Universitat Autònoma
de Barcelona

Ph.D. Thesis in Physics

Design and Optimization of Advanced Silicon Strip Detectors for High Energy Physics Experiments

Javier Fernández Tejero

Director **Dr. Miguel Ullán Comes**
Centro Nacional de Microelectrónica (IMB-CNM)
Consejo Superior de Investigaciones Científicas (CSIC)

Director **Dr. Celeste Fleta Corral**
Centro Nacional de Microelectrónica (IMB-CNM)
Consejo Superior de Investigaciones Científicas (CSIC)

Tutor **Dr. Lluís Font Guiteras**
Department of Physics
Universitat Autònoma de Barcelona (UAB)

Barcelona, July 2020

Centre Nacional de Microelectrònica IMB

CSIC
Consejo Superior de Investigaciones Científicas

Universitat Autònoma de Barcelona
Departament de Física

Centro Nacional de Microelectrónica (IMB-CNM)
Consejo Superior de Investigaciones Científicas (CSIC)

Design and Optimization of Advanced Silicon Strip Detectors for High Energy Physics Experiments

Memòria presentada per optar al títol de Doctor en Física

Autor: Javier Fernández Tejero
Directors: Dr. Miguel Ullán Comes i Dra. Celeste Fleta Corral
Tutor: Dr. Lluís Font Guiteras

CERTIFIQUEN:

que la memòria "Design and Optimization of Advanced Silicon Strip Detectors for High Energy Physics Experiments" que presenta Javier Fernández Tejero per optar al grau de Doctor en Física ha estat realitzada sota la seva direcció al Centro Nacional de Microelectrónica (IMB-CNM) del Consejo Superior de Investigaciones Científicas (CSIC) i tutoritzat al Departament de Física de la Universitat Autònoma de Barcelona (UAB).

Barcelona, juliol de 2020

Miguel Ullán Comes	Celeste Fleta Corral	Lluís Font Guiteras

A mis padres
y a mi hermana.

Acknowledgements

This work would not have been possible without the invaluable help of a large number of people, whom I have been fortunate to meet, and to whom I would like to thank and dedicate this thesis.

Primero dar las gracias a mis directores, Miguel Ullán y Celeste Fleta, por darme la oportunidad de empezar esta aventura. Desde el primer día he recibido su confianza y apoyo total. Han mostrado una paciencia infinita para ayudarme en todo lo que necesitara. De ellos he aprendido muchísimas cosas, en lo profesional y en lo personal.

M'agradaria agrair el suport rebut pel Departament de Física de la Universitat Autònoma de Barcelona (UAB), en especial al meu tutor Lluís Font, i a Jordi Mompart pel seus consells i per resoldre amablement qualsevol dubte, sempre en temps rècord.

Aquest treball també el vull dedicar als meus companys del Grup de Detectors de Radiació del Centro Nacional de Microelectrónica (IMB-CNM). He tingut la sort d'aprendre de tots/es ells/es. En especial, no puc deixar d'agrair tot el que he après de David Quirion, sempre disposat a ajudar-te amb un somriure, és una font inesgotable de coneixement. A Joan Marc Rafí pels seus consells sobre mesures i anàlisi. A Mar Carulla, Pablo Fernández, Daniela Bassignana, Javier Bravo, Rossella Zaffino, Maria Manna, Albert Doblas...i en general a tot el grup. És molt fàcil treballar amb gent tan professional, amable i positiva. Vull agrair també el bon ambient de treball que sempre han generat els meus companys de despatx. En especial a Laura Ortega, Dmitry Galyamin, Inci Dönmez, Perla Alday, Milena Tomic, (de nou) Mar Carulla, i tots/es els que en un moment o altre han passat temps al nostre despatx. Ha estat un plaer treballar amb vosaltres (i menjar les vostres delicioses galetes). Una especial menció també a tot l'equip de sala blanca del IMB-CNM, sense dubte, són la columna vertebral del centre. No puc deixar d'agrair a Maria Sánchez la seva paciència amb l'encapsulat de dispositius, i a Sergi Sánchez per l'ajuda amb les mesures a la taula semiautomàtica.

I would also like to acknowledge the staff of Deutsches Elektronen-Synchrotron (DESY) in Zeuthen, in particular to Ingo Bloch for the opportunity to work in the group, and for its constant support during these years. Special mention to Luise Poley, Laura Rehnisch, Sam Yanwing, Marko Milovanovic, Martin Stegler, Martin Renzmann and

Dennis Sperlich, for the help with the measurements and for making me feel part of the team. Thanks also to all the colleagues from the ATLAS ITk collaboration. Specially to Vitaliy Fadeyev, always ready to help. I have learnt a lot from him, and he has contributed directly or indirectly to most of the results presented in this thesis.

Muchísimas gracias a mi familia, en especial a mis padres Lucía Tejero y Jacinto Fernández, a mi querida hermana Carolina Fernández y a mis abuelos Ángeles Cardenas y Jacinto Fernández. Siempre me han apoyado a ciegas en todo lo que me he propuesto hacer. A mis queridas tías Rosa y Silvia Fernández, a David Sáez, Judit García, Jordi Sáez... Gracias a todos/as ellos/as he podido llegar hasta aquí. Quiero dar las gracias también al apoyo que he recibido de mis amigos/as. Gracias a Bruc por hacerme compañía cada día. Gracias a Maria Argudo por convencerme de que podía hacerlo. Gracias a Diego Sánchez por dejarme su monitor para escribir la tesis desde casa en época de confinamiento. Gracias a Francesc Sarrate por hacer más amenos los meses de escritura. A Paco Martínez, Laia Oller, Virginio Cepas, Víctor Caballero, Marta Estarán, Beatriz Corral, Marina Martínez, Albert Giménez, Pepe Lechón, Ana Ciscar, Javier Martínez, Rubén Llanas, Zaira Priego, Eduardo Artigas, Alejandra Allonca, Juanjo Fernández, Andrés Ramón, Jordi Verdú, Carlos Navarro, Eva Sánchez, Óscar Pavón...y en general a todos/as los/as amigos/as que me habéis apoyado durante todo este tiempo. Tengo la suerte de contar con un gran número de buenas personas a mi alrededor.

No me gustaría acabar esta dedicatoria sin volver a mencionar a mis directores Miguel Ullán y Celeste Fleta. Al empezar esta aventura nunca hubiese imaginado todo lo que iba a aprender de ellos. Siempre les estaré profundamente agradecido. Además de haber sido buenos mentores, puedo decir que han sido (son) buenos amigos.

A tots i totes, Gràcies! ¡Gracias! Thank you!

Abstract

The European Organization for Nuclear Research (CERN) is currently implementing a major upgrade of the 27-kilometre Large Hadron Collider (LHC), with the aim to expand the physics reach, increasing the luminosity and triggering the consequent multiplication of interactions per bunch crossing. The new High-Luminosity LHC (HL-LHC) operational conditions will have a direct impact in the silicon tracking sensors of the main detectors, the ATLAS and CMS experiments, causing a large increase of detector occupancy and radiation damage. This PhD thesis investigates the design and optimization of a new generation of silicon strip detectors able to withstand the severe operational conditions expected for the HL-LHC upgrade.

Firstly, the study tackles the development of the silicon strip detectors from a layout design point of view. Basic device elements are presented and its design is discussed based on performance considerations. A new python-based Automatic Layout Generation Tool (ALGT) is presented, with the aim to address the need for large area prototypes of strip detectors at the R&D stages of the ATLAS Inner-Tracker (ITk) upgrade. The ALGT is used to design a large area strip sensor prototype, several miniature sensors and diodes. These devices are generated, and arranged in a full 6-inch wafer layout design, for the participation of Infineon Technologies AG in the ATLAS ITk strip sensor Market Survey.

In addition, layout designs of a wide range of microelectronic test structures with different applications are presented. A set of test structures for the development of strip technologies is proposed, along with a test chip able to cover all the routine tests planned for the Quality Assurance (QA) works during the ATLAS strip sensor production. On the other hand, in order to improve the readout connection, several designs of Embedded Pitch Adaptors (EPA) are also proposed to minimize the possible drawbacks associated to the introduction of a second metal layer on the sensor structure.

An extensive characterization is performed in the frame of the ATLAS ITk strip sensor Market Survey. Devices fabricated by the candidate foundries, Infineon Technologies AG and Hamamatsu Photonics K.K., are evaluated before and after proton, neutron

and gamma irradiations, up to fluences expected at the end of the HL-LHC lifetime. Test structures and QA test chips designed are also characterized, with the objective to validate its design, expand the technology evaluation and provide reference values for the ATLAS production tests.

Additional studies and developments are presented with application in High Energy Physics (HEP) experiments in general. Hot topics, such as the humidity sensitivity of large area sensors or the effectiveness of the punch-through protection in a beam-loss scenario, are extensively investigated. A complete study of the new EPA structures proposed, and results of the first strip sensors fabricated in 6-inch wafers at Centro Nacional de Microelectrónica (IMB-CNM), are also shown.

The layout designs and characterizations presented, contribute to define the final design of the ATLAS strip sensors for the HL-LHC upgrade, and the additional investigations reveal conclusions of general interest that can lay the foundation for future developments.

Contents

1 Framework

The High Energy Physics (HEP) community is preparing a major upgrade of the Large Hadron Collider (LHC), increasing the luminosity of the current accelerator by an order of magnitude. Particle tracking detectors will be directly influenced by the severe operational conditions expected, specially in the layers closest to the collision point. This chapter presents the framework of this PhD thesis, introducing the High-Luminosity LHC upgrade (Section 1.1) and the improvements planned for the inner tracker of the ATLAS detector (Section 1.2), with special emphasis on the new strip detectors. Additionally, an introduction to silicon radiation detectors is presented (Section 1.3), with the objective to provide a general view of the structure and performance of the tracking sensors developed in this thesis.

1.1 The High-Luminosity Large Hadron Collider

The Large Hadron Collider (LHC) [1] is the main accelerator in The European Organization for Nuclear Research (CERN), located in France and Switzerland. It was built between 1998 and 2008 as the world's largest and most powerful particle collider. The 27-kilometre LHC ring, located 100 m underground, is the last element on a succession of accelerators (Figure 1.1), where each machine injects the particle beam into the next one, increasing the energy of the particles. The LHC consists of a ring of superconducting magnets and accelerating structures to boost the energy of the particles along the beam pipes. The particle beams are accelerated just below the speed of light before they are forced to collide with counter-circulating beams, reaching a total collision energy of 14 TeV. The beams into the LHC are made to collide at four locations around the ring, corresponding to the positions of four particle detectors: ATLAS (A Toroidal Large Hadron Collider Apparatus) [2], CMS (Compact Muon Solenoid) [3], LHCb (Large Hadron Collider beauty) [4] and ALICE (A Large Ion Collider Experiment) [5]. Figure 1.2 provides an overall view of the LHC and its four detectors and Table 1.1 lists the main parameters of the LHC experiment.

LHC has been spearheading the research on fundamental nature of matter since its operation start-up on September 2008, shedding light on hot topics such as the nature

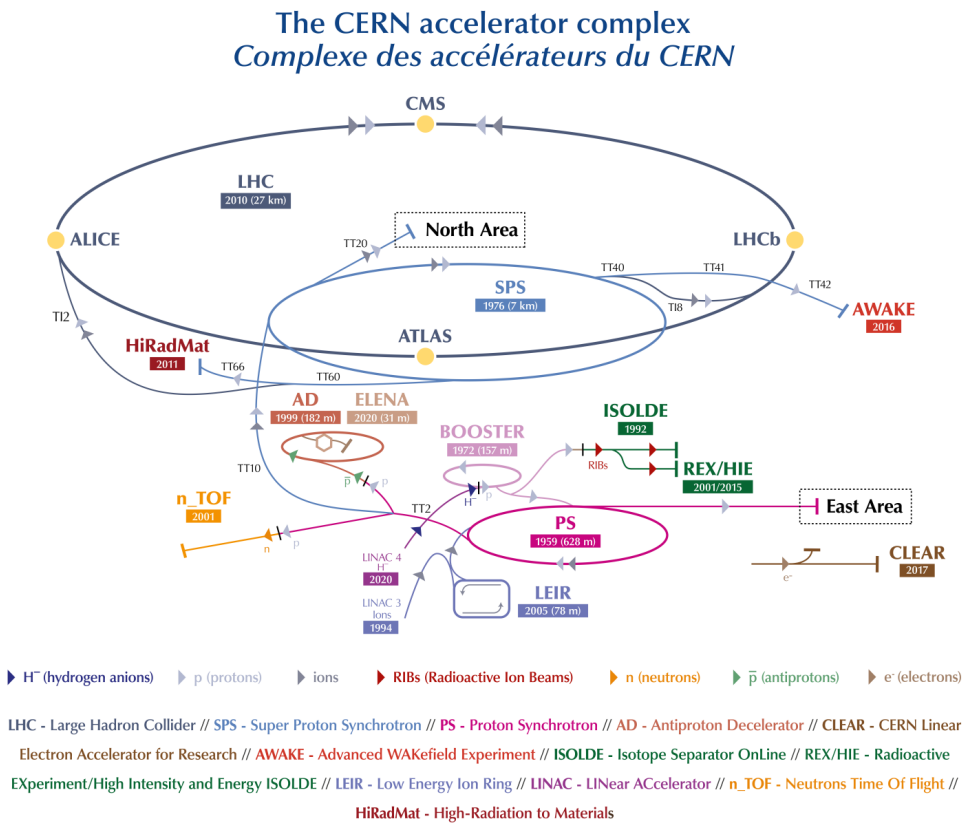


Fig. 1.1: The CERN accelerator complex. Figure from [1].

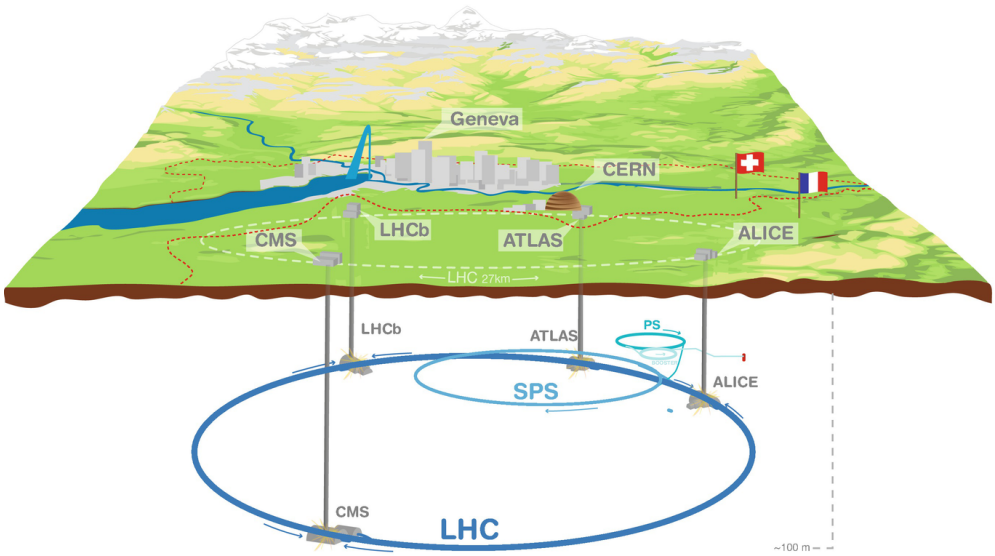


Fig. 1.2: Overall view of the Large Hadron Collider, including the ATLAS, CMS, ALICE and LHCb experiments. Figure from [1].

Parameter	Value
Beam energy	7 TeV
Dipole magnetic field	8.4 T
Peak Luminosity (protons)	$1.2{\cdot}10^{34}$ cm^{-2}s^{-1}
Injection energy	450 GeV
Circulating current/beam	0.53 A
Number of bunches	2835
Time between bunches	24.95 ns
Protons per bunch	1.05·1011
Stored beam energy	334 MJ
r.m.s. beam radius at intersection point	16 μm
Crossing angle	200 μrad
Beam lifetime	22 h
Luminosity lifetime	10 h

Tab. 1.1: Main parameters of the LHC experiment.

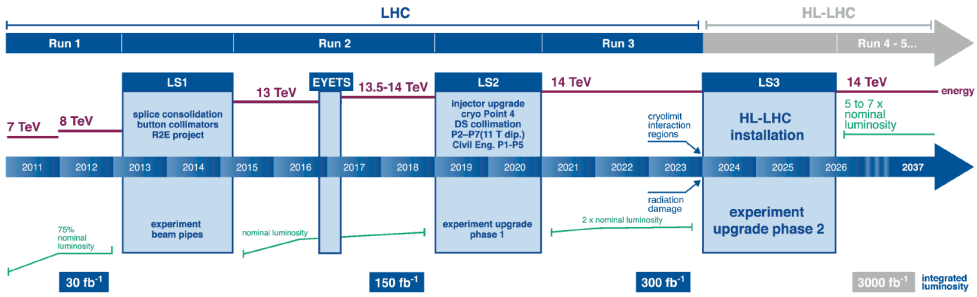


Fig. 1.3: LHC baseline programme including the HL-LHC run. Figure from [10].

of dark matter [6] or the origin of mass with the discovery of a new particle on August 2012: the Higgs boson ([7], [8]). To surpass the great contributions made during these years, CERN prepared an ambitious upgrade of the current collider, the High-Luminosity LHC (HL-LHC) [9], keeping the experiment at the forefront of the High Energy Physics (HEP) research. The upgraded collider will begin collisions in 2026 (Figure 1.3), operating at four times the nominal LHC luminosity, $5{\cdot}10^{34}$ cm^{-2}s^{-1}, and a total integrated luminosity of up to 3000 fb^{-1}, increasing the number of collisions that occur in a given amount of time. This represents an order of magnitude more data than what would be collected prior to the HL-LHC. To achieve this, the beam will be more intense and more concentrated than at present in the LHC. The HL-LHC upgrade will allow physicists to study in greater detail known mechanisms, such as the Higgs boson, and rare new phenomena.

The new HL-LHC working conditions require improved detectors able to operate after exposure to unprecedented large particle rates and fluences, increasing drastically the hit occupancy and the radiation doses received by the future tracking systems. This major upgrade represents a unique challenge for the design of a new generation of

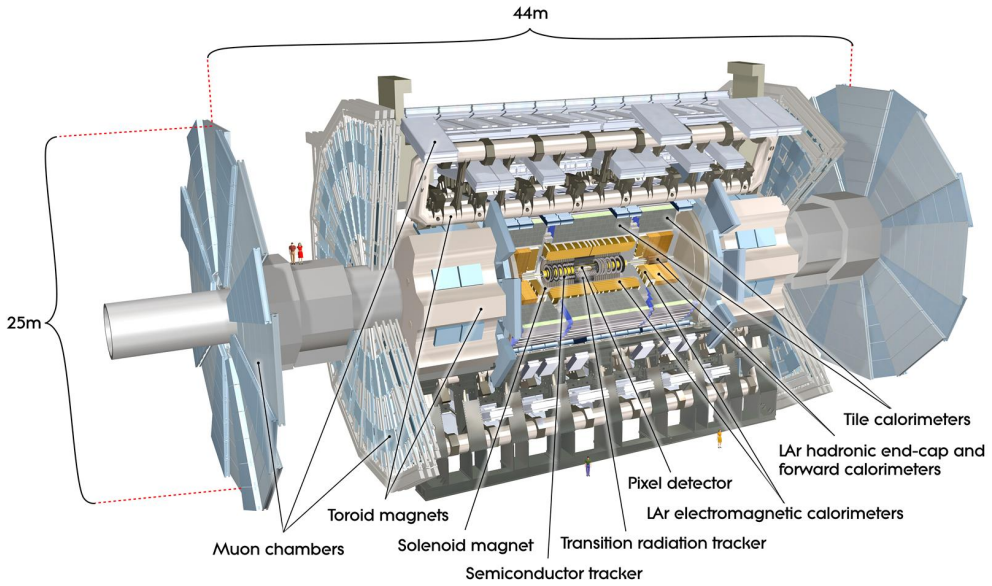


Fig. 1.4: Computer generated image of the whole ATLAS detector. Figure from [11].

tracking sensors, able to withstand severe operating conditions during the 10 years of lifetime of the experiment.

1.2 The ATLAS Experiment

ATLAS is one of the two general-purpose detectors at the LHC [2], with 46 m length, 25 m diameter, and a total weight of 7000-tonne (Figure 1.4). Particle beams collide at the centre of the ATLAS detector generating new particles flying out from the collision point in all directions. The tracks, momentum, and energy of the particles are recorded by six different concentric detecting subsystems arranged in layers around the collision point, using an advanced trigger system to discriminate the events to record.

1.2.1 Inner-Tracker Upgrade

The current ATLAS Inner Detector (ID) [12] consists of three concentric tracking systems. Pixel sensors are located at the innermost layers (Pixel Detector) [13], surrounded by the Semiconductor Tracker (SCT) ([14], [15]) composed of strip sensors, and a Transition Radiation Tracker (TRT) ([16], [17]) at the outermost layers of the ID (Figure 1.5(top)). The current ID was designed to withstand radiation doses[1] up to

[1] Radiation doses including a safety factor of 1.5.

1-MeV neutron equivalent fluences (n_{eq}) of $2{\cdot}10^{14}$ cm^{-2} at the SCT and 10^{15} cm^{-2} at the Pixel Detector, corresponding to the LHC conditions.

However, the current tracking system would not be able to withstand the radiation fluences expected for the HL-LHC, reaching accumulated doses of up to $2.1{\cdot}10^{16}$ n_{eq}/cm^{-2} at the inner layers. A new all-silicon tracker will be installed, known as the Inner-Tracker (ITk) (Figure 1.5(bottom)). Similarly to the current ID, the new ITk will consist of a pixel detector [18] in the region closest to the collision point, and a strip detector [10] at the highest radii. However, the new design of the ATLAS ITk, will be able to fulfil the challenging requirements of the HL-LHC, representing a major upgrade to withstand the severe working conditions. The top image on Figure 1.6 presents a schematic layout of the ATLAS ITk, showing a one-quadrant cross-section. The pixel sensors are represented in red and strip sensors in blue, and the vertical lines correspond to the *End-cap* devices and the horizontal ones to the *Barrel* sensors. Additionally, the bottom image on Figure 1.6 shows a simulation of the distribution of the maximum fluences expected at the different regions of the ITk.

1.2.2 Strip Tracker

The strip system of the new ITk ([10], [19]) extends from the outer layer of the pixel system (30 cm radius) to the inner surface of the calorimeter (1 m radius), with a total length of 6 m and representing a silicon area of around 165 m^2. The strip region planned consists of a four-layer Barrel section and one End-cap section on each side, composed of six disks per side (Figure 1.5(bottom)). All the strip sensors in the new ITk are planned to maximize the available area of 6-inch wafers, minimizing the sensor termination for cost-effectiveness and for the least dead space. The sensors will have n-type strip implants on p-type silicon substrates, in contrast to the p-on-n technology currently used in the ATLAS ID, as n-on-p detectors are more resistant to bulk damage[2]. The strips will be AC coupled to the strip (readout) metals, and biased with polysilicon resistors, with inter-strip isolation achieved by p-stop structures. The sensor termination, *Slim-edge*, has been optimized to cover the minimum area using a single guard ring and a p-type region at the very edge of the sensors, allowing biasing voltages up to 700 V without breakdown ([20], [21]).

Barrel Sensors:

The Barrel section of the ITk strip system will be composed of square-shaped sensors with a die area of around 10 x 10 cm^2. The strips in the Barrel sensors will be parallel with a constant pitch of 75.5 μm. Two Barrel sensor types are planned with different strip lengths, 2.4 cm for *Short-strip* (SS) sensors and 4.8 cm for the *Long-strip* (LS)

[2]Radiation effects on silicon detectors are discussed in Section 2.3.

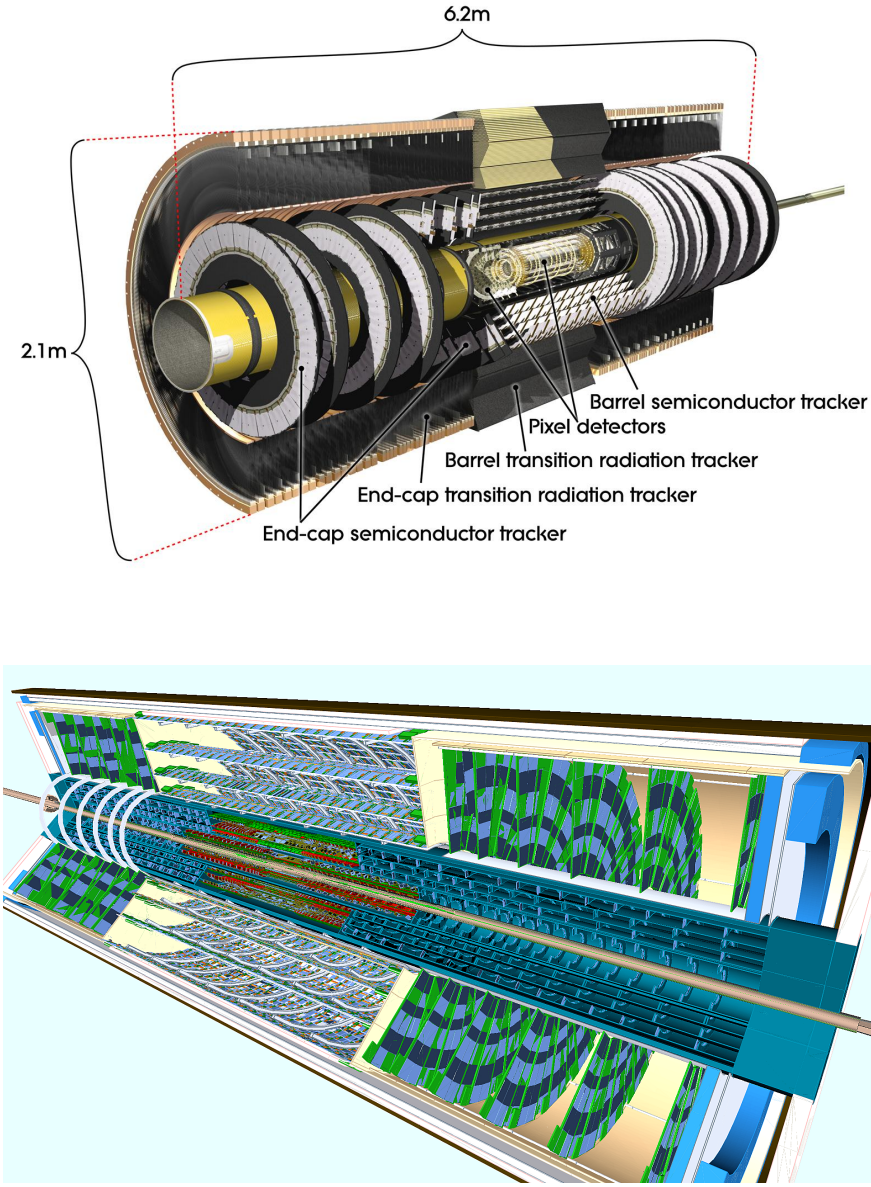


Fig. 1.5: Computer generated images of the current ATLAS Inner Detector (ID) (top) and the planned Inner-Tracker (ITk) upgrade (bottom) for the forthcoming HL-LHC. Figures from [11].

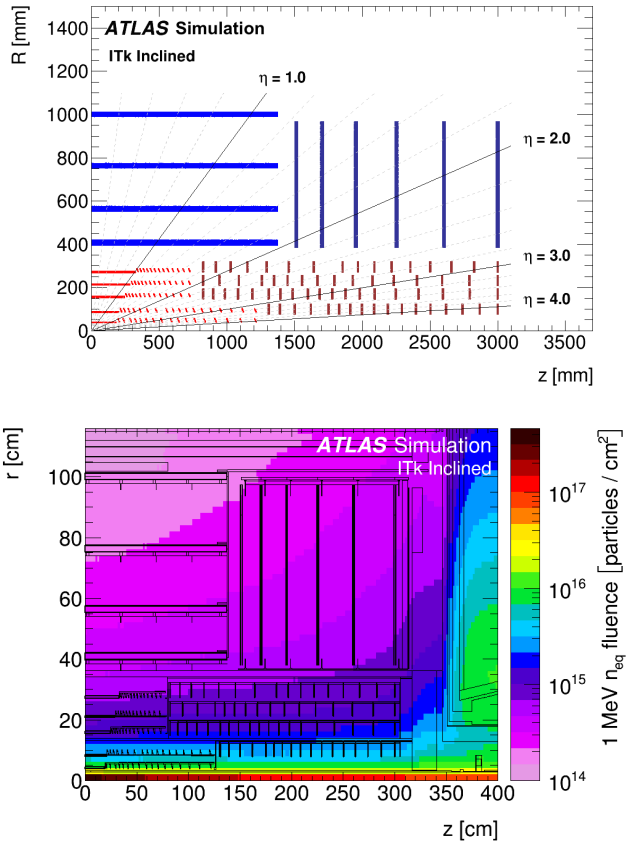


Fig. 1.6: (top) Schematic layout of the ATLAS ITk for the HL-LHC upgrade. Horizontal axis corresponds to the beam line axis, with the particle collision point at zero. Pixel sensors are represented by red lines, strip sensors by blue lines, Barrel sensors correspond to the horizontal lines and End-cap sensors to the vertical ones. (bottom) Simulation of the 1-MeV neutron equivalent fluence distribution for the ITk layout. Figure from [10].

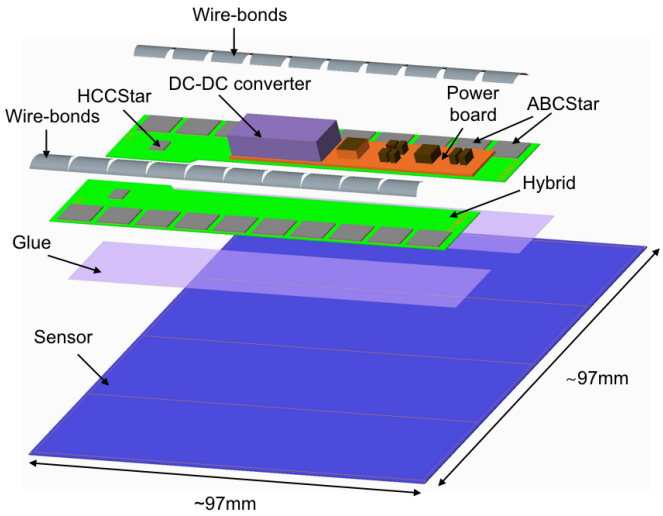


Fig. 1.7: Exploded view of a SS Barrel module with all relevant components. Figure from [10].

design, with the aim to balance the strip occupancy [10] with the shortest strips closest to the beam region. The strips will be arranged in strip rows with 1282 strips/row, resulting in 4 strip rows for the SS design and 2 strip rows for the LS. The readout will be done by ASICs with 256 channels, using 10 chips per 2 strip rows (128 channels x 10 ASICs = 1280 channels/row) and leaving one strip per sensor side to shape the electric field. Figure 1.7 shows an exploded view of a Barrel SS module with all relevant components, such as the hybrid, the power board or the ASICs. Barrel modules are arranged in *Stave* structures (Figure 1.8). Each Barrel Stave is populated with 28 modules (14 per Stave side), representing a total of 392 Staves on the four concentric Barrel layers. Barrel modules on both sides are rotated by 26 mrad to allow a total stereo angle of 52 mrad with the objective to determine the radius (R) by correlating the hits on both sides.

Table 1.2 provides an overview of the total number of strip sensors needed for the ATLAS ITk, also detailing the number of channels and rows per sensor. Further details of the characteristics and specifications of the ATLAS ITk Barrel sensors will be presented in Chapter 4.

End-cap Sensors:

The sensors in the End-cap region are planned to have strips oriented radially to the beam axis to give a measurement of the azimuthal angle (ϕ). The End-cap region will be composed by *Petal* structures arranged in wheels (Figure 1.9). Each wheel is populated with 32 identical Petals, and each Petal is planned to contain nine modules

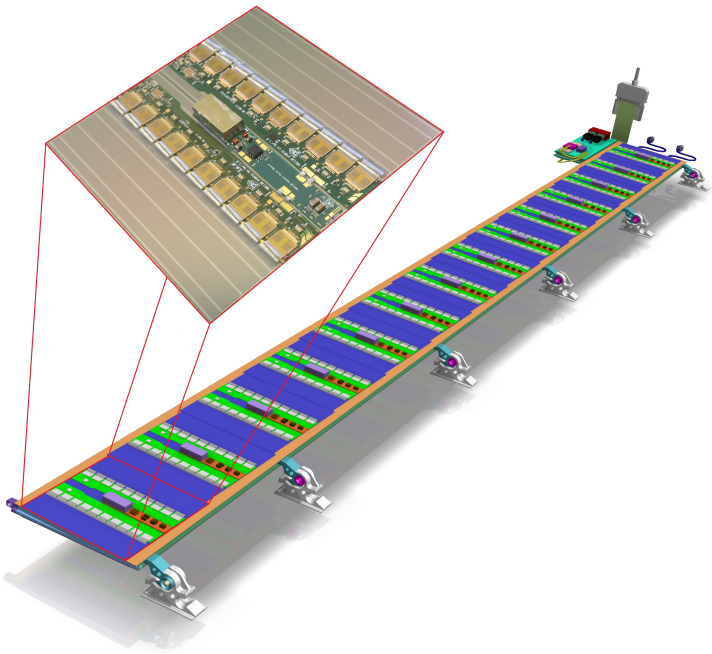
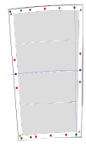
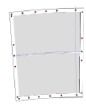


Fig. 1.8: Computer generated image of a Barrel Stave, showing a picture of a single LS module. Figure from [22].

Sensor type	Number of sensors	Shape	Number of rows	Channels per sensor	Min/max pitch (μm)
Short-strips	3808	Square	4	5128	75.5
Long-strips	7168	Square	2	2564	75.5
EC Ring 0	768		4	4360	73.5/84
EC Ring 1	768		4	5640	69/81
EC Ring 2	768		2	3076	73.5/84
EC Ring 3	1536		4	3592	70.6/83.5
EC Ring 4	1536		2	2052	73.4/83.9
EC Ring 5	1536		2	2308	74.8/83.6

Tab. 1.2: Overview of the total number of silicon strip sensors per shape and channels per sensor. Table from [10].

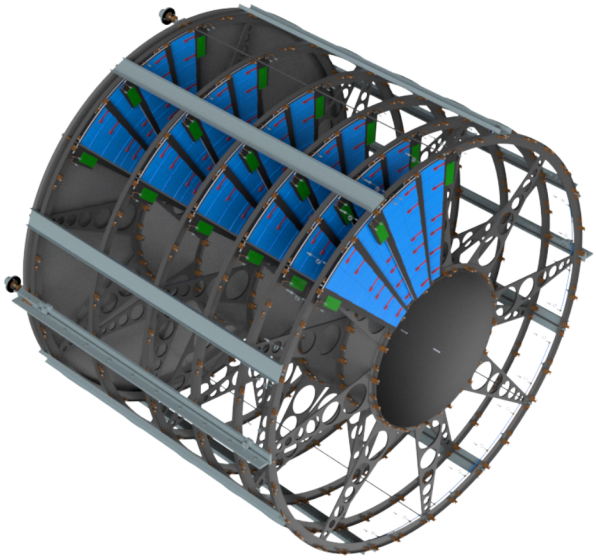


Fig. 1.9: Schematic representation of one of the End-cap systems containing six wheels housing a total of 32 identical petals (only four petals shown in this representation). Figure from [10].

on each side, corresponding to nine sensors with six different End-cap sensor designs (Figure 1.10), i.e. from Ring 0 (R0) to Ring 5 (R5), with the radial strips adapted to the distance (radius) to the beam pipe. In contrast to the Barrel sensors, strips in End-cap designs are laid out with a built-in stereo angle of 20 mrad with the aim to determine the z-position correlating the hits on both sides of the Petal, that will compose a strip sensor system with a total stereo angle of 40 mrad. The stereo angle is built into the End-cap sensors due to the complexity of achieving a physical rotation of sensors with varying geometries and variable strip pitch.

To achieve the built-in stereo angle, the End-cap sensors will have a wedge shape with curved edges that represents a major challenge from a design point of view. As depicted in Figure 1.11, the inner and outer edges of the sensor are concentric arcs centred at the beam axis (point O). On the other hand, the two sides of the sensor are straight lines, with the origin rotated away from the beam axis (point F) to have a built-in stereo angle (φ_s) of 20 mrad. In consequence, the sensor sides are laid out parallel to the first and last strips of the sensor in order to avoid the presence of truncated (orphan) strips that introduce undesired limitations on the sensor performance ([23], [24]). Similarly to the Barrel sensors, the strips in the End-cap sensors are arranged in 2 or 4 strip rows, depending on the ring, with a number of strips multiple of 128 to match the readout chip channels (which "serve" two strip rows), and with an angular pitch constant within the same strip row. Table 1.2 also provides an overview of the total number of strip sensors needed for the ATLAS ITk End-cap system with number of channels and rows per sensor type.

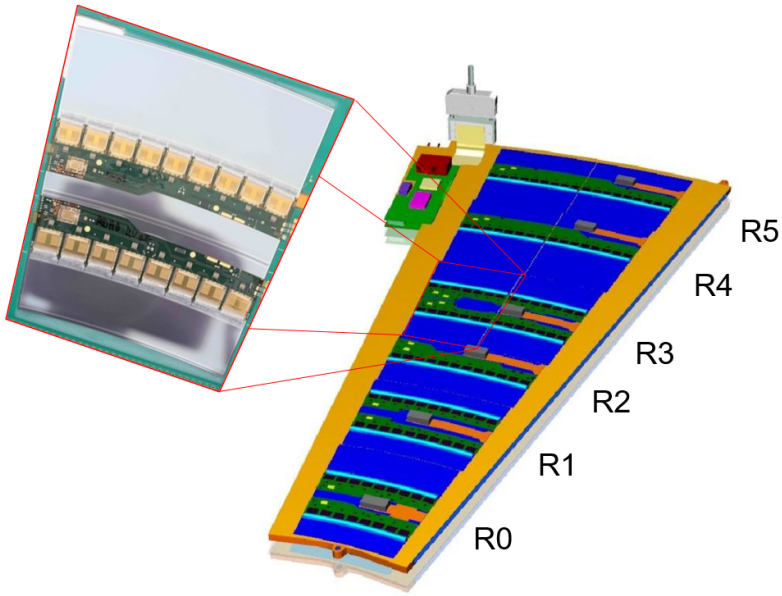


Fig. 1.10: Computer generated image of an End-cap Petal, housing six different End-cap strip sensors, and showing a picture of a single R3 module. Figure adapted from [10].

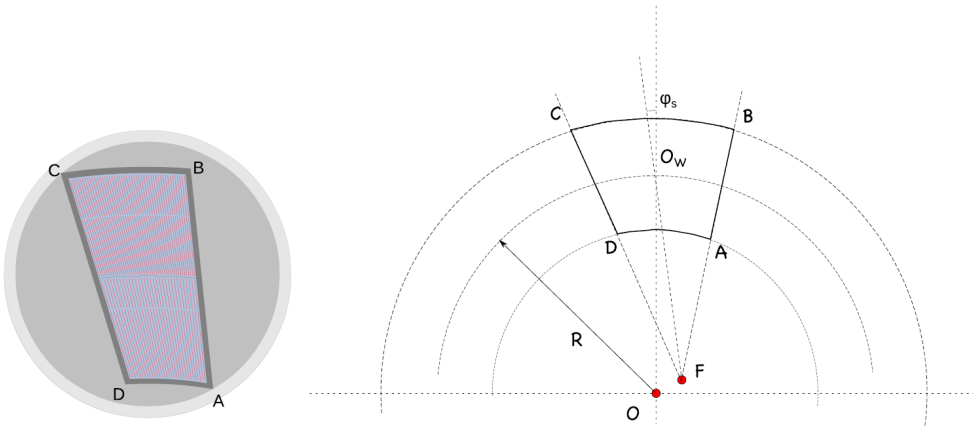


Fig. 1.11: Schematic representation of the End-cap sensor geometry. O corresponds to the center of the beam pipe, strips are radially oriented to the point F to have implemented a built-in stereo angle φ_s and A, B, C and D are the corners of the sensor in the ring R. Figure from [25].

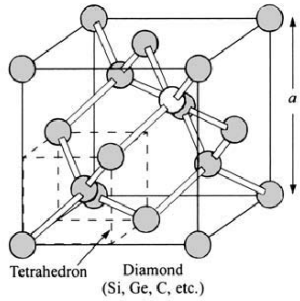


Fig. 1.12: Silicon crystal structure. Figure from [26].

1.3 Silicon Radiation Detectors

1.3.1 Silicon Properties

Silicon is a semiconductor with a diamond crystal structure. The simplest repeating unit (*unit cell*) has two interleaved face-centered cubic (FCC) lattices with their origins at (0, 0, 0) and (1/4, 1/4, 1/4), as shown in Figure 1.12. The silicon atom is tetravalent and shares each of the four valence electrons (silicon is a group IV material) with its neighbours forming covalent bonds in its crystalline structure.

Semiconductors have a forbidden region in the energy band structure, known as *band gap*, that separates the *conduction band* and the *valence band*. For a theoretical temperature of 0 K, and in the absence of impurities (*intrinsic silicon*), all the valence band levels in the crystal structure are filled by electrons, whilst the conduction band remains empty, behaving as an insulator material. If the temperature increases, the energy provided to the material can excite some electrons from the valence band to the conduction band, allowing their migration through the crystal lattice, and thus increasing the conductivity of the material. The energy difference between the highest level of the valence band and the lowest level of the conduction band is known as the *band gap energy* (E_g). It represents the minimum energy needed to promote an electron from the valence band to the conduction band. The energy where exactly half of the available levels are occupied is defined as the *Fermi level* (E_F). In particular, silicon has an indirect band gap, which means that an increase in energy and momentum is needed to excite an electron. The vacancy generated in the valence band is called *hole* and, from a conduction point of view, it is treated as a carrier of electricity comparable with the free electron but with the opposite electric charge. Figure 1.13 shows a representation of the energy levels in an intrinsic semiconductor and the electron promotion between energy levels in terms of covalent bonds.

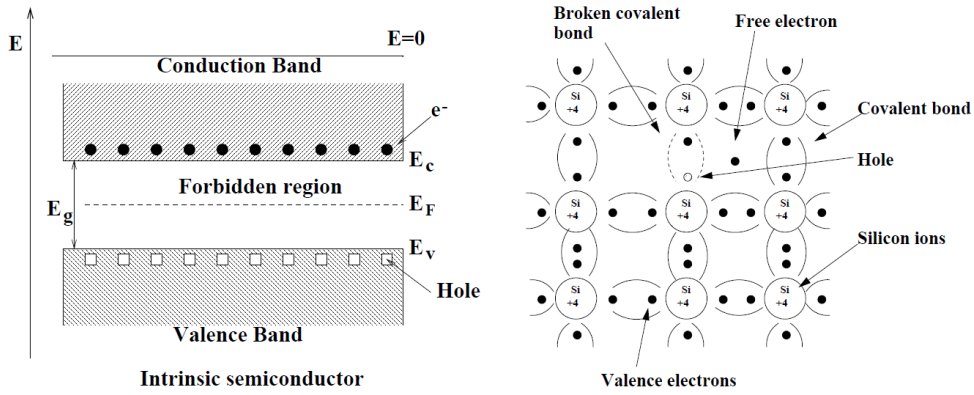


Fig. 1.13: Band structure for outer shell electron energies in silicon (left) and silicon crystal with a broken covalent bond (right).

The thermally produced hole and electron densities are equal in intrinsic silicon. However, this conductivity behaviour can be altered introducing impurities, forming an *extrinsic* (*doped*) semiconductor. The presence of impurities in the silicon lattice introduces energy levels in the forbidden gap, increasing the thermally produced carriers. The introduction of impurities with five electrons in the valence band (group V), such as phosphorus or arsenic, in a silicon crystal (group IV), leaves one electron per impurity atom available in the crystal lattice (*donor*). The net result is an excess of electron carriers, and a reduction of holes caused by a higher recombination ratio, turning the silicon into a *n-type* material. Similarly, the introduction of impurities with three electrons in the valence band (group III), such as boron, gallium or indium, results in an excess of holes (*acceptor*), generating a *p-type* material. Figure 1.14 illustrates the mechanisms responsible for the electrical changes induced by phosphorus and boron implantations, typically used in the fabrication of silicon radiation detectors. Figure 1.15 also shows the energy levels introduced in the forbidden gap by other elements.

Specifically, the resistivity (ρ) and conductivity (σ) are related to the carrier density and mobility by

$$\rho = \frac{1}{e(\mu_n n + \mu_p p)} = \frac{1}{\sigma} \tag{1.1}$$

where e is the electron charge, n is the concentration of electrons in the conduction band, p is the concentration of holes in the valence band, μ_n is the mobility of the electrons, and μ_p is the mobility of the holes. Mobility is defined as

$$\mu = \frac{v}{E} \tag{1.2}$$

where E is the electric field and v the drift velocity that, at room temperature, has a value of 1350 cm^2/V·s for electrons and 480 cm^2/V·s for holes.

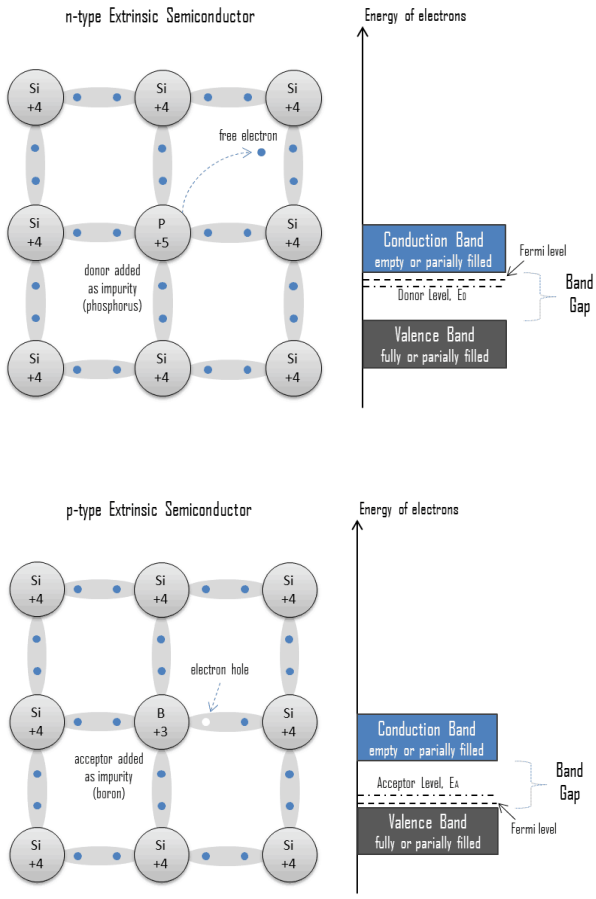


Fig. 1.14: Schematic representation of n-type (top) and p-type (bottom) silicon generated through the introduction of phosphorus and boron impurities, respectively.

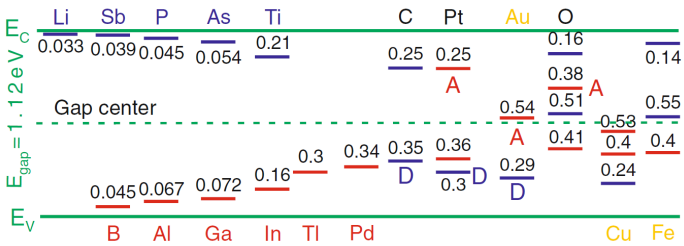


Fig. 1.15: Examples of additional energy levels introduced in the silicon forbidden region by impurities. Figure from [27].

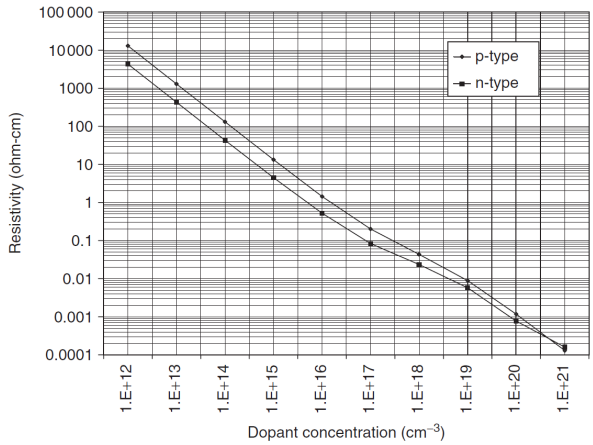


Fig. 1.16: Silicon resistivity can be varied over eight orders of magnitude by doping. Figure from [28].

The controlled introduction of dopants in silicon is a basic and powerful technique in microfabrication. It allows to control with a high accuracy the electrical properties of silicon, reaching resistivity ranges of eight orders of magnitude (Figure 1.16).

1.3.2 Silicon pn-Junction

A pn-junction is formed when a semiconductor is doped with acceptors (p-type) on one side and donors (n-type) on the other. In this situation, free electrons in the n-type region diffuse to the p-type side to recombine with the holes. Similarly, but in the opposite direction, the excess of holes in the p-type region will also move to recombine with the electrons in the n-type region. The recombination of the diffusing charges generates a region around the pn-junction where free charges are neutralized, known as *depletion region* also known as *space-charge region* because the charge equilibrium is decompensated, generating charged ions in this region. In this situation, an electric field is generated between the positive and negative ions that opposes the diffusion, which increases until it equals the diffusion, reaching a dynamic equilibrium (Figure 1.17). This *built-in voltage* (V_{bi}) is described by

$$V_{bi} = \frac{k_B T}{e} log(\frac{N_a N_d}{n_i^2}) \tag{1.3}$$

where k_B is the Boltzmann constant, T is the temperature, n_i is the intrinsic carrier concentration, N_a and N_d are the acceptor and donor concentrations, respectively. The built-in voltage is of the order of a few hundred millivolts at room temperature, for typical doping densities of $N_a \approx 10^{17}$ cm^{-3} and $N_d \approx 10^{15}$ cm^{-3}.

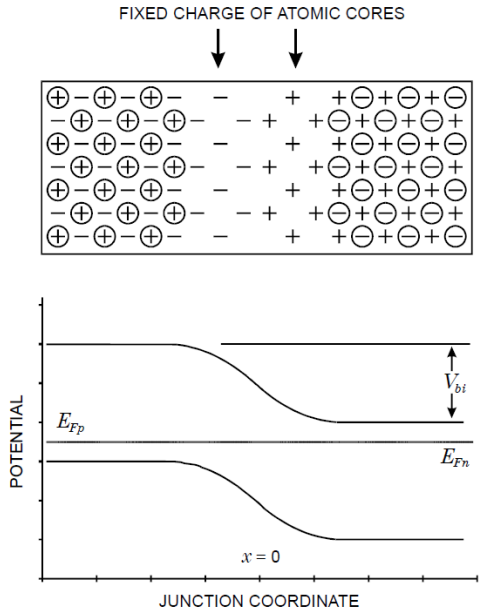


Fig. 1.17: Charge distribution in a pn-junction in thermal equilibrium (top) and electric potential as a function of the position within the junction (bottom). Figure from [29].

This dynamic equilibrium remains unless an external voltage is applied on the junction. If a direct voltage (*forward bias*) is applied to the pn-junction the potential barrier is reduced, whilst if a reverse voltage (*reverse bias*) is used the potential barrier and the depleted region increases. In reverse bias mode, the depletion region will extend mainly on the side with the lower doping concentration. If we assume a highly doped region on a lowly doped substrate, the expression for the width of the depleted zone (W) can be approximated by

$$W = \sqrt{\frac{2\epsilon(V_{bias} + V_{bi})}{eN_x}} \tag{1.4}$$

where ϵ is the silicon dielectric constant, V_{bias} is the external reverse bias and N_x is the doping density of the lowly doped region. Alternatively, using Equation 1.1, the width of the depleted zone can be also expressed in terms of the material resistivity (ρ) and of the majority carriers mobility (μ) as

$$W = \sqrt{2\epsilon\rho\mu(V_{bias} + V_{bi})} \tag{1.5}$$

Then, as the applied V_{bias} increases, the depleted region extends until the free carriers are removed from the whole silicon substrate. The bias voltage at which the depleted zone reaches its maximum depth (d), is known as the *full depletion voltage* (V_{fd}).

Assuming that the contribution of the V_{bi} is negligible, as V_{fd} is usually more than one order of magnitude higher, the full depletion voltage can be defined as

$$V_{fd} = \frac{d^2}{2\epsilon\rho\mu} - V_{bi} \approx \frac{d^2}{2\epsilon\rho\mu} \tag{1.6}$$

that can be alternatively expressed as

$$V_{fd} = \frac{ed^2}{2\epsilon}|N_{eff}| \tag{1.7}$$

where N_{eff} is the effective doping concentration, defined as the difference between the donor and acceptor concentrations.

Thus, the resistivity of the substrate is a very important parameter that has to be carefully considered for the design and characterization of devices based on the pn-junction mechanisms, as the silicon radiation detectors. The resistivity of the substrate will directly affect the mobility of the carriers and, in consequence, the voltage needed to deplete the active area of the detector.

1.3.3 Radiation Detectors

Radiation detectors are composed, in the simplest configuration, by pairs of electrodes placed in an absorbing medium. A charged particle passing through the detector deposits part of its energy resulting, directly or indirectly, in the creation of electric charge. Radiation detectors with direct generation of charge can be classified into *gaseous detectors* and *solid-state detectors*, depending on the composition of the absorbing medium used. In both cases, the electrodes collect the electric charge generated by a crossing particle, normally by applying an electric field, to generate an output electrical signal that can be read and interpreted, although normally the gaseous detectors use multiplication mechanisms to increase the primary charge generated. The third major radiation detector technology is the *scintillation detectors*, which use materials with the property of luminescence to re-emit the energy absorbed from radiation in the form of light (photons). Scintillators make use of a photomultiplier to transform the energy of the photons generated by radiation into electrons (photoelectric effect), resulting in an electrical pulse that can be analysed. Thus, scintillators are a type of radiation detector that creates electric charges indirectly, making use of the luminescence effect.

In particular, solid-state radiation detectors with a silicon substrate are extensively used for particle tracking purposes in HEP experiments. The silicon bulk is depleted from free carriers through a reverse biased pn-junction. Then, the charge deposited within its volume drifts towards the junction and is collected by the electrodes, whilst the charge released in the non-depleted zone is lost as it quickly recombines with the free carriers.

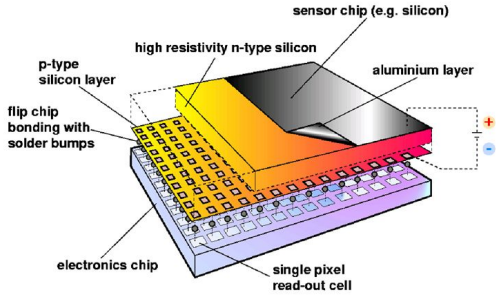


Fig. 1.18: Schematic representation of pixel detector (Medipix2). Figure from [30].

In consequence, silicon detectors should operate with an applied voltage sufficient to deplete the maximum volume, preferably the whole substrate (full depletion).

Silicon radiation detectors can be position sensitive if one of the electrodes is segmented in an array of pn-junctions, or if several detectors with single pn-junctions are arranged to provide information of the position of the crossing particle. Two position-detector configurations are commonly used in HEP experiments: strip detectors and pixel detectors.

Silicon strip detectors have one of the electrodes divided into multiple (independent) pn-junctions forming long and thin strips, separated by few tens to few hundreds microns, usually isolated from the closest neighbours, and each one connected to its own readout electronics stage. This segmentation provides good two-dimensional position information of the point where the impinging particle is crossing the detector, since the electric charge generated quickly drifts to the closest strips. Positioning two of these detectors together with some misalignment angle provides accurate 3D information of the position of the crossing particle. Strip detectors represent the baseline of the work presented in this thesis, and extensive details of their design, fabrication and performance will be provided in the following chapters.

On the other hand, silicon pixel detectors are small diodes with a pixel cell of a few square microns, usually arranged in a bigger detector. The reduced dimensions of each pixel directly provide an accurate 3D positioning of the crossing particle. The pixels need to be individually connected to the readout electronics through bump bonding (Figure 1.18). Pixel detectors are particularly useful when the hit ratio is very high, as their small size avoids ambiguities in the determination of the hit position, in contrast to the strip detectors. However, the number of readout channels per pixel detector is much higher than the channels needed in a strip detector, making more complex the assembly and readout. In consequence, pixel detectors are usually positioned at the innermost layers of the particle tracking detectors, whilst strip detectors are used in the outer layers.

2 Silicon Strip Detectors

Silicon strip detectors, along with pixel detectors, are extensively used in High Energy Physics (HEP) experiments for particle tracking purposes. For the forthcoming High-Luminosity Large Hadron Collider (HL-LHC) upgrade, the ATLAS collaboration decided to replace the current p-on-n strip sensors as p-type silicon is more resistant to bulk damage and, besides, it does not undergo type inversion like n-type silicon. This chapter provides a general overview of the features and technology of n-on-p silicon strip detectors. The different device components and basic performance are detailed in Section 2.1, the generalities of the fabrication process introduced in Section 2.2 and the radiation effects discussed in Section 2.3. Additionally, the key parameters and testing methods used to evaluate the performance of the silicon strip sensors are presented in Section 2.4.

2.1 Device Description

Silicon strip detectors are diodes with one of the electrodes segmented to provide information of the position where an ionizing particle has crossed the device. In n-on-p technology, a p-type bulk is used as substrate and an array of long and narrow n^+ segments (*strips*) are implanted on the frontside, generating multiple p-n junctions. The signal is AC-coupled, through a coupling dielectric, to metal lines on top of the strip implants to drive the signal to the readout electronics. Strips are individually isolated using p-type implants. A n^+ ring (*bias ring*) is implemented surrounding all the strips, that are connected to it through a polysilicon resistor (*bias resistor*), keeping all the strips at the same potential. Additional n^+ rings (*guard rings*) are included surrounding the bias ring with the objective to shape the electric field outside the sensitive area. A p^{++} layer is implanted in the backplane of the substrate, with a metal layer on top, to ensure a good ohmic contact. At the very edge of the detector, in the frontside, a p^{++} ring is also implemented (*edge structure*) to avoid the appearance of an inversion region at the edge of the device that could short-circuit the n-implants at the frontside with the backplane of the sensor through the conductive silicon edge. Then, each strip behaves as a reverse biased diode. Figure 2.1 presents a schematic representation of a n-on-p silicon strip detector.

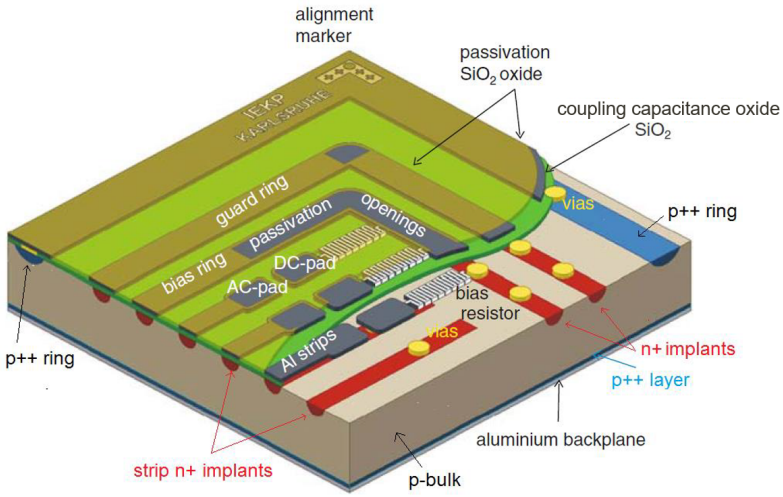


Fig. 2.1: Schematic representation of a n-on-p AC-coupled silicon strip detector. Figure adapted from [27].

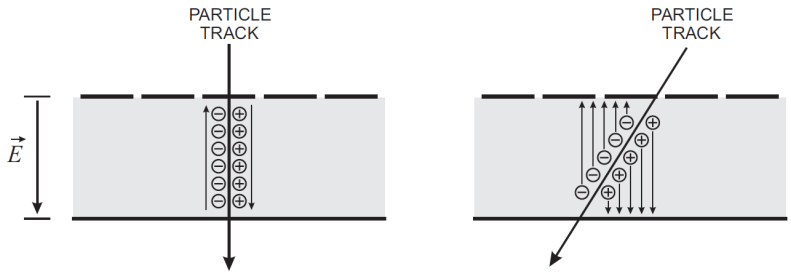


Fig. 2.2: Schematic representation of signal formation and collection in a silicon strip detector. Particles crossing the detector perpendicularly will deposit charge on one strip (left), whilst particles crossing with a certain angle will deposit charge in multiple strips (right). Figure from [31].

In operation, the bulk is fully depleted due to the reverse bias applied between the upper (n-type) and lower (p-type) sides of the device. In this situation, electron-hole pairs are generated in the bulk when an ionizing particle crosses the device, and the electrons drift towards the closer strips (Figure 2.2). The charge collected by the strip is AC-coupled to the readout channel and provides information about the coordinate of the crossing particle. For charged particles, the collected signal is proportional to the thickness of the detector. However, since the strip detectors are usually installed very close to the interaction point, their thickness should be ideally as low as possible so as not to perturb the pass of particles without compromising the signal-to-noise ratio.

2.2 Fabrication

This section presents a general view of the fabrication process of silicon strip detectors, based on the steps performed at the cleanroom of Centro Nacional de Microelectrónica (IMB-CNM). No detailed information is provided on the fabrication processes of the other sensors tested in this thesis and fabricated by other foundries, due to intellectual property and non-disclosure agreements, but the description of the different steps is enough to understand the overall fabrication process.

Substrates normally used for the fabrication of silicon strip detectors are p-type (in case of n-on-p technologies) high-resistivity Float Zone (FZ) silicon wafers with <100> orientation with diameters of 4 or 6-inch. Typical substrate thickness used for HEP applications is around 300 μm. Firstly, each wafer is labelled at the backside, usually indicating the fabrication batch number, the wafer number and other information used to easily identify the characteristics of the device fabricated. In particular, IMB-CNM uses the code XXXXX-DET-YY for the fabrication of silicon strip detectors, where XXXXX is the fabrication batch, YY is the wafer number and the label DET indicates that it will be used to fabricate silicon radiation detectors.

In order to remove possible surface residues, native thin oxides, and to improve the crystallographic properties of the silicon surface, the wafers are firstly cleaned using Hydrofluoric and Hydrochloric acids, and a thick oxide is grown in all the surfaces and then etched completely. Next, a new 0.8 μm thick wet oxide is grown to isolate the different active areas of the future device.

2.2.1 P-stops and Sensor Edge Isolation

The next step in the fabrication process is the formation of p-type regions (*p-stops*) at the frontside of the device to isolate the different strips, and to avoid the appearance of an inversion region at the very edge of the device that could short-circuit the n-implants at the frontside with the backplane of the sensor. Depending on the sensor design, p-stops can be also included in the guard ring, e.g. isolating the different rings in a multi-guard ring configuration.

In order to define the different regions to be implanted, a first photolithographic step is done using the mask level called P-DIFF, where all the regions to be implanted are open, while the rest are masked, in order to expose only the selected patterns with ultraviolet (UV) light. The photolithographic process starts with the deposition of a photo-resist at the frontside, followed by a soft bake to drive out the solvent that can still be present in the resist. Typical resist thicknesses are about 1 μm when contact/proximity

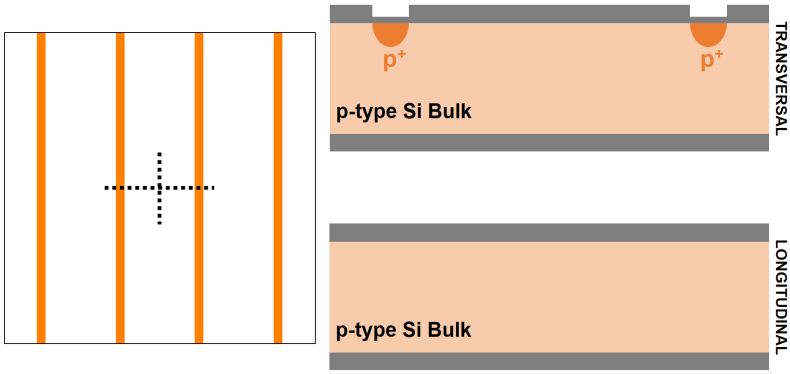


Fig. 2.3: First photolithographic step (P-DIFF): formation of p-type regions (p-stops) for inter-strip isolation and sensor edge isolation. Layout image (left) indicating the position of cross-sections transversal (top) and longitudinal (bottom) to strips.

lithography[1] is used. Then, the wafer and the mask P-DIFF are introduced into the mask aligner, where they are aligned and the photo-resist is illuminated with UV light in the regions to be implanted. After the UV exposure, the resist is baked in order to diffuse the photogenerated molecules, that can change its solubility when the wafer is introduced in the developer to remove the resist in the exposed regions. At this point, the field oxide in the illuminated regions is etched, together with the backside silicon oxide, and the residual resist is removed and a cleaning step is performed. A thin silicon oxide of 40 nm, is grown to protect the silicon surface during implantation, to optimize the doping profile and to avoid the *channeling* of the implanted ions. Finally, the wafer is introduced into the ion implanter and Boron impurities are introduced, with an implantation dose of 10^{13} cm^{-2} at an energy of 50 keV, to generate the p$^+$ regions. Figure 2.3 shows schematic cross-sections, parallel and perpendicular to the future strips, at this point of the fabrication process.

The wafers are cleaned after the ion implantation and a new wet oxidation is performed so the oxide on top of the p-stop is 0.8 μm thick. The high temperatures used in this oxidation process (1100ºC) also diffuse the implanted Boron into the silicon and activate the doping impurities by making them occupy substitutional positions in the silicon lattice.

2.2.2 Strip Implants, Coupling Oxides and Backplane Implant

The formation of the p-stops is followed by the implantation of n-type regions to define the implants of the strips, bias ring and guard rings. In order to define the patterns to be implanted, a second photolithographic step is done using the mask level called N-

[1] Photolithography technique is explained in Section 3.1.1.

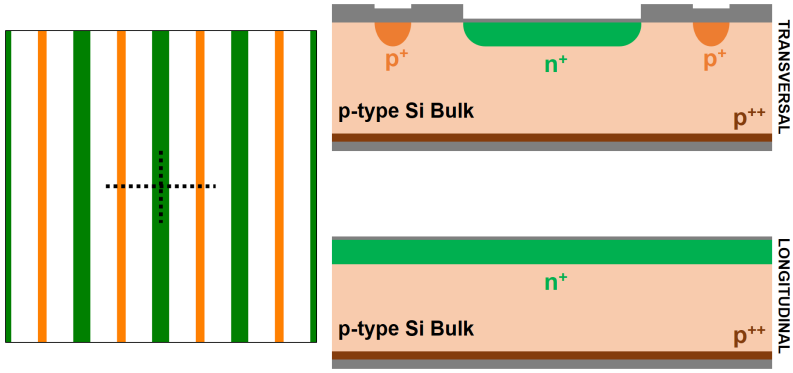


Fig. 2.4: Second photolithographic step (N-DIFF): formation of n-type strip implants. Layout image (left) indicating the position of cross-sections transversal (top) and longitudinal (bottom) to strips.

DIFF. Similarly to the previous photolithographic process, the resist is deposited on the frontside of the wafer, the regions to be implanted are exposed to the UV light, and the resist and the oxide in these areas are etched. Prior to the implantation process, a thin silicon oxide layer of 40 nm is grown to protect the silicon surface during implantation and to avoid channeling, similarly to the previous p-type implantation. Then, the wafer is introduced into the ion implanter and Phosphorus impurities are introduced, with an implantation dose of 10^{15} cm^{-2} at an energy of 100 keV, to generate the n^+ diffusions. Next, Boron impurities are introduced in the backside of the wafer with an implantation dose of 10^{15} cm^{-2}, at an energy of 50 keV to create the ohmic contact.

A dry oxidation is performed after the implantations, with the objective to create the coupling oxide on top of the strip implants. Figure 2.4 presents schematics cross-sections at this point of the fabrication, showing the strip implant, the coupling oxide and the backplane implant, together with the p-stops.

2.2.3 Bias Resistors and Contacts

The next step in the fabrication process is the formation of the polysilicon bias resistors to connect each strip with the bias ring. Firstly, a 0.6 μm thick polysilicon layer is deposited on both sides of the wafer using the Low Pressure Chemical Vapor Deposition (LPCVD) technique. The resistivity of the polysilicon layer is adjusted to meet the bias resistance requirements performing a Boron implantation at the frontside of the wafer, with a dose of 10^{14} cm^{-2} and an energy of 100 keV.

Then, with the aim to define the contacts between the bias resistor and the future metal layer, a third photolithographic step is performed using the mask level called RES-CON. A resist layer is deposited at the frontside, and the contact regions are exposed to

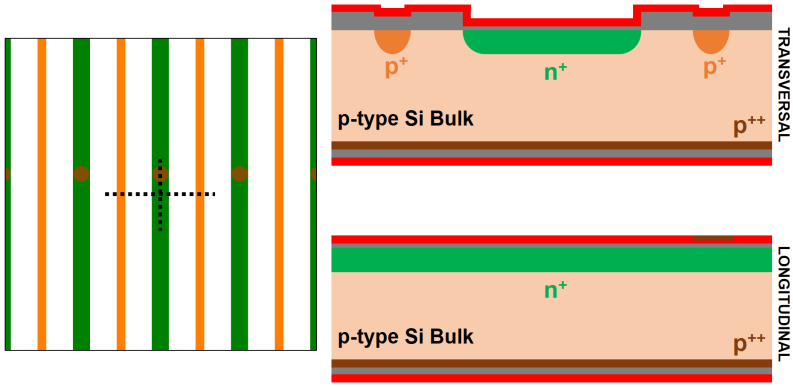


Fig. 2.5: Third photolithographic step (RES-CON): formation of contacts between polysilicon bias resistors and strip metal. Layout image (left) indicating the position of cross-sections transversal (top) and longitudinal (bottom) to strips.

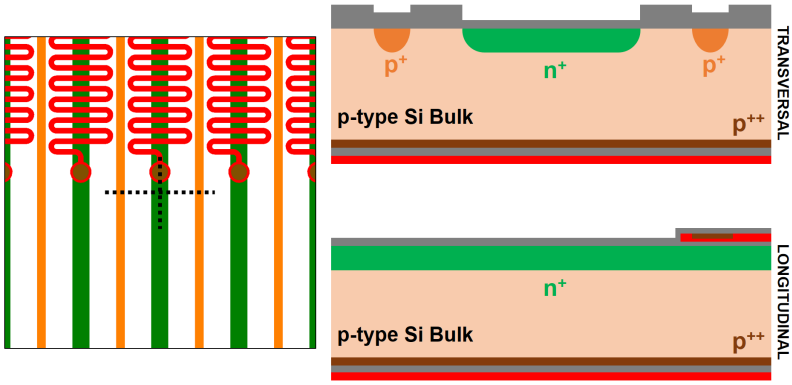


Fig. 2.6: Fourth photolithographic step (POLY): formation of polysilicon bias resistors. Layout image (left) indicating the position of cross-sections transversal (top) and longitudinal (bottom) to strips.

the UV light. The wafer is introduced in the ion implanter, and Boron impurities are implanted with a dose of 10^{15} cm^{-2} at an energy of 50 keV, generating low resistivity p-type regions where the metal will be contacted, and the resist is removed. The bias resistor contact is illustrated in the longitudinal cross-section in Figure 2.5.

Now that the contacts between polysilicon and metal are created, a fourth photolithographic step is needed to define the polysilicon bias resistors. The resist is deposited at the frontside, and the wafer is illuminated through the mask level called POLY. Then, the resist in the exposed regions is developed, and the underlaying polysilicon etched, forming the polysilicon bias resistors that connect the strip implants with the bias ring. The wafer is cleaned, and a wet oxidation is performed with the double purpose to create a thin oxide that will isolate the bias resistors from the metal layer and to activate the doping impurities by the thermal process (Figure 2.6).

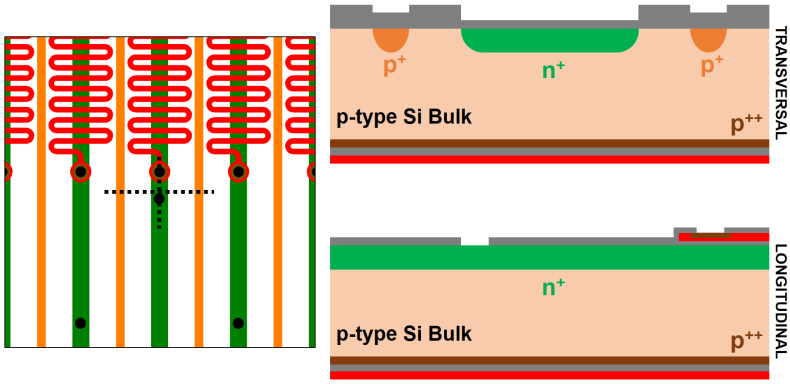


Fig. 2.7: Fifth photolithographic step (WINDOW): formation of contacts between polysilicon bias resistors and strip metals, and also between strip implants and strip metals. Layout image (left) indicating the position of cross-sections transversal (top) and longitudinal (bottom) to strips.

2.2.4 Readout Metals

Now that the bias resistors for each strip are formed, and the metal-polysilicon contact regions created, the next step is the formation of the metal readout lines along with the metal layers present in the bias ring, guard rings and edge structure. A new photolithographic step needs to be done at this point. It will be used to generate contact windows in the silicon oxide where the polysilicon and metal should be contacted, and also where the n-implants and the metal layer should be contacted, e.g. DC pads or bias ring.

For the formation of the windows in the silicon oxide, a fifth mask level called WINDOW is used to expose the photo-resist in the regions to be contacted. The illuminated resist is removed and the underlying silicon oxide is etched in order to ensure the oxide opening on top of the polysilicon layer and n-implants (Figure 2.7).

Since thin native oxide layers can be grown in short periods of time, deteriorating the contact, a preventive removal of silicon oxide is performed immediately before the metal layer deposition (less than 10 minutes). Then, a layer of 0.5 μm thick metal alloy, made of Aluminum (99.5%) and Copper (0.5%), is sputtered on the frontside of the wafer.

A sixth photolithographic process is then performed, using the mask level called METAL. In this case a thicker resist layer is deposited (2 μm) on top of the metal, the exposed resist is removed and the metal in these regions etched to form the metal patterns over the strips, bias ring, guard rings and edge structure (Figure 2.8). Finally, the wafer is cleaned and the resist residues removed.

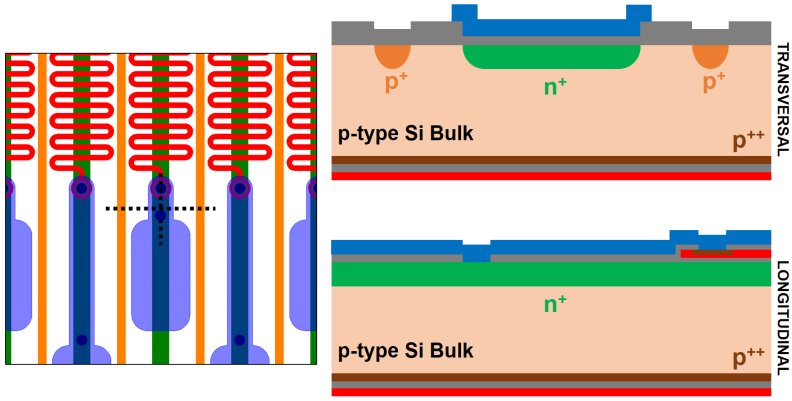


Fig. 2.8: Sixth photolithographic step (METAL): formation of strip metals. Layout image (left) indicating the position of cross-sections transversal (top) and longitudinal (bottom) to strips.

Optionally[2], if a second metal is needed in the sensor structure, an isolator oxide layer should be grown on top of the readout metal, in order to avoid their electrical contact (*inter-metal oxide*). In this case, a multi-layer oxide, with a total thickness of 1.5 μm, is used in order to minimize the appearance of *pinholes* short-circuiting both metals, and 0.5 μm of this multi-layer is etched to avoid sharp-edges in the structures of the future second metal layer.

Then, a new photolithographic step is needed to define the contacts between both metals, using the mask level called VIA. Firstly, a 2 μm thick resist layer is deposited on top of the inter-metal oxide. The regions where the contacts will be located are illuminated, and the underlying oxide etched, leaving the readout metal uncovered. Next, a 1.5 μm thick Al/Cu layer is sputtered on top of the inter-metal oxide, completely filling the contacts opened with the VIA mask level, and connecting both metals in these regions. Finally, another photolithographic process is performed using the mask level called METAL2, to define the structures in the second metal layer. Similarly to the previous photolithographic step, a 2 μm thick resist layer is deposited on top of the deposited metal, and the wafer is illuminated through the METAL2 photomask. In this case, the regions outside of the future structures are illuminated, and the underlying metal etched to form the second metal structures.

[2]For standard silicon strip sensors, with only one (readout) metal, skip the following fabrication steps and continue in Section 2.2.5. Silicon strip detectors with a second metal routing the readout metal, known as *Embedded Pitch Adaptors* (EPA) are proposed and characterized in this thesis. Objectives and designs of the EPA structures are detailed in Section 3.2.8.

2.2.5 Backplane Metal, Surface Passivation and Contact Pads

At this point of the fabrication, the backside of the wafer is still protected by a polysilicon layer, deposited during the formation of the bias resistors. The frontside of the wafer is protected with a thick resist layer (2 μm), and the polysilicon layer at the backside is etched, exposing the p-implant region. Then, a 1.5 μm thick Al/Cu layer is sputtered on the backside of the wafer, forming the backplane electrode. Similarly to the frontside metal layer, the deposition of the backside metal should be done minimizing the time between the polysilicon etching and the metal deposition to avoid the appearance of native oxides that could deteriorate the ohmic contact. Finally, the wafer is cleaned and baked (350ºC) to prepare the metal for the final fabrication step.

The next step of the fabrication process is the passivation of the surface with the objective to protect the different structures from the influence of the environment, such as contaminants or humidity-induced ions. At IMB-CNM, two different layers are used to passivate the surface, a 0.4 μm thick silicon oxide layer and a 0.2 μm thick silicon nitride layer on top. Both layers are deposited using the Plasma-Enhanced Chemical Vapor Deposition (PECVD) technique, followed by a cleaning process and a last photolithographic step.

The seventh mask level[3], called PASSIV, is used for the formation of passivation openings for contact pads, such as AC, DC and bias pads. A thick resist layer (2 μm) is deposited on top of the passivation layers, and the resist in the contact pad regions are illuminated and removed. Finally, the silicon nitride layer is etched, the resist is baked again to ensure its proper adhesion, and the silicon oxide layer is etched in a second step, exposing the metal of the sensor pads. Figure 2.9 presents cross-sections, longitudinal and transversal to the strip direction, of a silicon strip detector at the end of the fabrication process.

2.3 Radiation Effects

In HEP experiments, the aim of the silicon tracking detectors is the detection of particles traversing the device, making use of the radiation-matter interactions. However, these interactions can also significantly alter the characteristics of the detector when its exposition is prolonged. Permanent radiation damage in silicon devices can be divided in two categories: *ionization damage* and *displacement damage*, affecting the surface and bulk differently. Ionization damage creates electron-hole pairs at the silicon bulk and the silicon oxide surface layers. In the bulk, the charges generated are rapidly

[3]It will be the ninth mask level in case a second metal layer has been included.

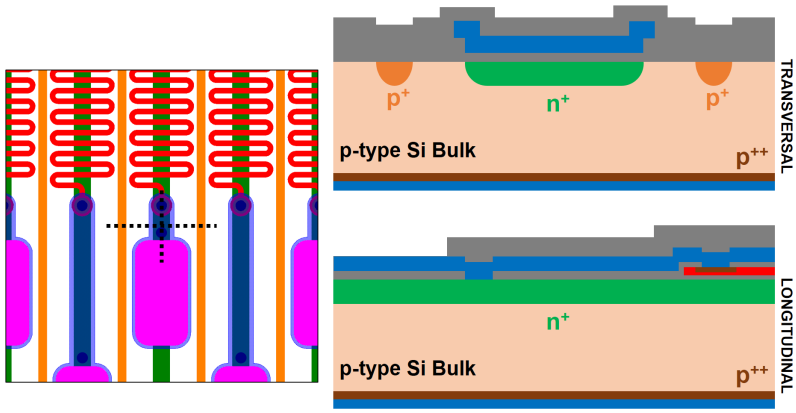


Fig. 2.9: Seventh (and last) photolithographic step (PASSIV): formation of passivation openings for AC and DC contact pads. Layout image (left) indicating the position of cross-sections transversal (top) and longitudinal (bottom) to strips.

driven to the electrodes causing no damage. In contrast, at the surface layers and their interfaces with silicon, radiation creates positive trapped charges and interface traps that modify the electric field, creating surface generation currents and, in silicon strip detectors, affecting the inter-strip characteristics. On the other hand, the effect of displacement damage on the surface layers is negligible, but permanent damages can be created at the silicon bulk through the dislocation of atoms from their position in the crystal lattice, that deteriorate basic detector properties such as the leakage current, the full depletion voltage or the charge collection efficiency. This section provides a general view of the mechanisms responsible for the radiation damages induced on the silicon bulk and surface layers, and their consequences on the performance of silicon strip detectors.

2.3.1 Surface Damage

The insulating oxide layers present at the surface of the silicon strip detectors can be electrically altered by ionizing radiation. The effects mainly depend on the total energy absorbed, and are independent from the radiation type. However, the ionization produced depends on the material, as it depends on the number of electron-hole pairs generated per absorbed energy unit, expressed in rad or Gy[4]. Incident ionizing particles generate electron-hole pairs at the surface layers of the silicon strip detector (usually SiO_2). Since electrons have higher mobility ($\mu_e \approx 20$ cm^2/Vs) than holes ($\mu_h \approx 2{\cdot}10^{-5}$ cm^2/Vs) in SiO_2, electrons are rapidly collected by the electrode, while holes slowly move towards the SiO_2/Si interface. Some of these holes can be trapped at the oxide or the interface generating relatively fixed positive charges that attract electrons from the bulk. In consequence, electron accumulation layers can form conducting channels at the

[4] 1 Gy = 1 J/kg = 100 rad.

silicon surface between the strip implants, deteriorating the inter-strip characteristics, such as inter-strip resistance and capacitance, directly affecting the signal of the device. Additionally, energy levels created in the SiO_2/Si interface can increase the surface generation current, modifying the leakage current of the device. However, it is worth mentioning that the ionization damage induced in the surface layers can be minimized to an acceptable level optimizing the fabrication processes (better oxide quality) and adapting the design of the detector (surface isolation elements: p-stop, p-spray).

2.3.2 Bulk Damage

Silicon bulk properties are mainly influenced by the displacement damage originated in the interaction between the impinging particles and the lattice atoms. While the electron-hole pairs generated by the ionizing radiation are rapidly collected by the electrodes, the interaction with the lattice may lead to permanent material changes that could significantly alter the performance of the device. Neutral particles scatter elastically with the nucleus in the silicon lattice, whilst charged particles can interact electrostatically with the partially screened nucleus. Consequently, the energy transfer and kinematics of the interaction, and the subsequent modifications of the crystallographic structure, are directly related to the radiation type ($\beta^{+/-}$, pions, neutrons, ions, γ) and energy.

In the recoil path traveled by an impinging particle in the silicon bulk, several lattice atoms can be displaced, generating *point defects*, whilst most of the energy is deposited at the end of the path, forming *cluster defects*. Recoil energies above 25 eV will create point defects; energies between 2 keV and 12 keV will be able to generate a cluster defect and additional point defects; and higher energies will result in several clusters and point defects. As an example, Figure 2.10 shows a Monte Carlo simulation of the point and cluster defects generated by an incident particle with a recoil energy of 50 keV [32], approximately the average kinetic energy that 1 MeV neutron can impart to the lattice.

Point defects can be classified in four groups (Figure 2.11), depending if an atom is located at an unexpected lattice site (*substitutional defects*), if it is located at a normally unoccupied site (*interstitial defects*), if a lattice site is empty (*vacancies*) or if it is a combination of an interstitial next to a vacancy (*Frenkel defects*).

The total damage produced is proportional to the Non-Ionizing Energy Loss (NIEL), which gives the portion of energy lost by a traversing particle which does not go into ionization and eventually leads to displacement damage. The value of the NIEL depends on the type and energy of the impinging particle and its value is scaled to the reference value of 1 MeV neutrons, through the use of the hardness factor (κ).

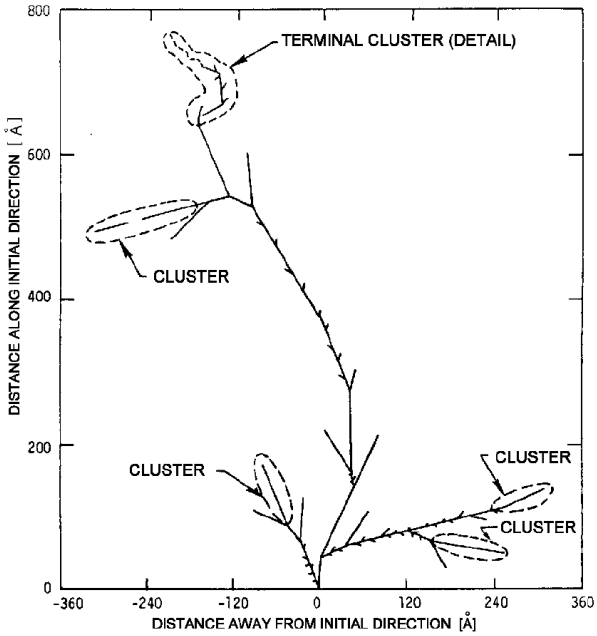


Fig. 2.10: Monte Carlo simulation of the path and defects originated by an impinging particle with 50 keV. Figure from [32].

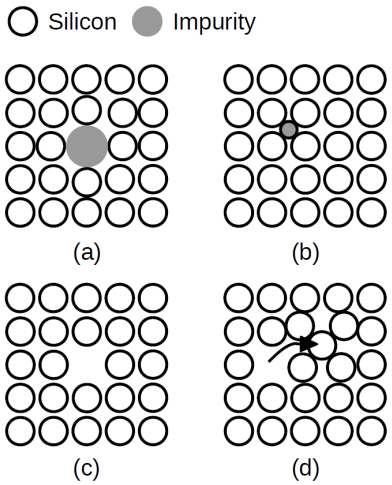


Fig. 2.11: Radiation induced point defects: (a) substitutional defect, (b) interstitial defect, (c) lattice vacancy, and (d) Frenkel defect (interstitial + vacancy). Figure from [26].

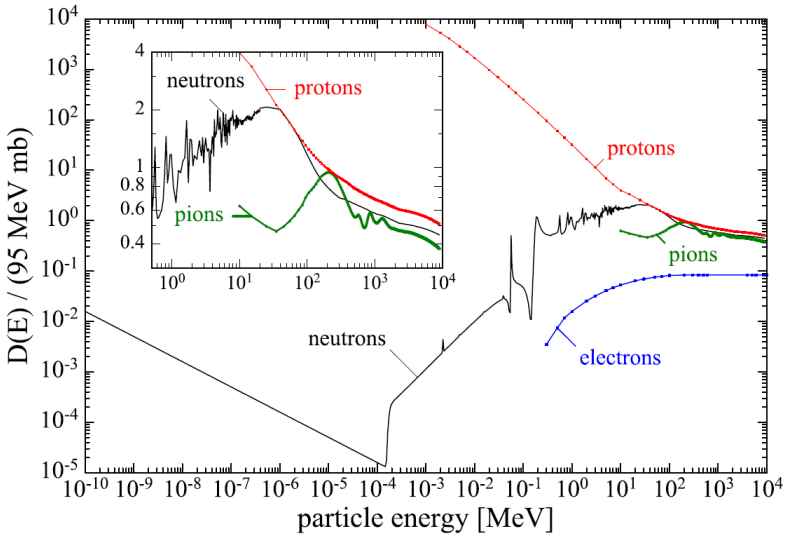


Fig. 2.12: Calculated values of NIEL cross-sections for different particles normalized to 95 MeV mb (1-MeV neutron equivalent). Figure from [33].

This factor compares the damage efficiency of a specific irradiation to the damage which would have been produced by the same fluence of 1 MeV neutrons. Consequently, the displacement damage of a particle fluence (Φ) can be expressed as the *1-MeV neutron equivalent fluence* (Φ_{eq}) as

$$\Phi_{eq} = \kappa\Phi \tag{2.1}$$

The NIEL cross-section, or displacement damage function D, is defined in units of MeV mb[5], and the 1-MeV neutron equivalent (n_{eq}) has been fixed to 95 MeV mb. Figure 2.12 shows calculated values of NIEL cross-sections for different particles normalized to 95 MeV mb. A detailed discussion of the NIEL-scaling hypothesis can be found in [33] and a compilation of hardness factor values for different particles and energies in [34].

The most notable manifestation of displacement damage can be classified in three groups:

- Formation of mid-gap states. Electron-hole generation and recombination is affected, increasing the leakage current on reverse-biased pn-junctions, where the conduction band is underpopulated and the generation dominates.

- Formation of defect energy levels close to a band gap, phenomenon known as *trapping*. If the emission times of the trapped charges are longer than the

[5] A *barn* (b) is a non-SI metric unit of area equal to 10^{-28} m^2, or 100 fm^2, approximately the cross-section area of an uranium nucleus.

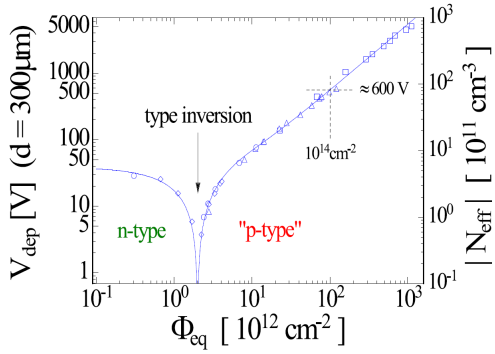


Fig. 2.13: Effective doping concentration, and full depletion voltage, as a function of 1-MeV neutron equivalent fluence for a standard FZ n-type silicon detector, illustrating the type inversion phenomena. Figure from [33].

acquisition time of the detector, the collected charge is reduced affecting the *Charge Collection Efficiency* (CCE).

- Changes in the effective doping characteristics. Defects can act as donors, acceptors or be neutral, affecting the effective doping concentration (N_{eff}). In particular, it was found that n-type silicon converts to p-type silicon (*type inversion*) when exposed to high radiation fluences [33], due to the creation of acceptor states. Figure 2.13 shows the evolution of the effective doping concentration, as a function of the radiation fluence, illustrating the type inversion phenomena.

Figure 2.14 illustrates the mechanisms induced by the creation of energy levels in the forbidden gap, and its influence on different macroscopic characteristics of the silicon detector. In particular, the changes in the effective doping concentration lead to a variation on the device full depletion voltage (V_{fd}), as they are directly proportional, as discussed in Section 1.3.2 (see Equation 1.7).

In consequence, as n-type silicon exposed to high radiation fluences will undergo dopant compensation and further type inversion, the V_{fd} of a p-on-n sensor will reach a minimum and then increase again, triggering an increase of the voltage needed to deplete the sensor bulk that eventually could lead to its operation in under-depletion. In addition, in an inverted p-on-n silicon sensor the onset of the depletion region and the maximum electric field is no longer at the segmented readout electrode which causes a degradation of the signal collected. In contrast, an n-on-p silicon sensor will not suffer type inversion and only increase steadily its operational voltage.

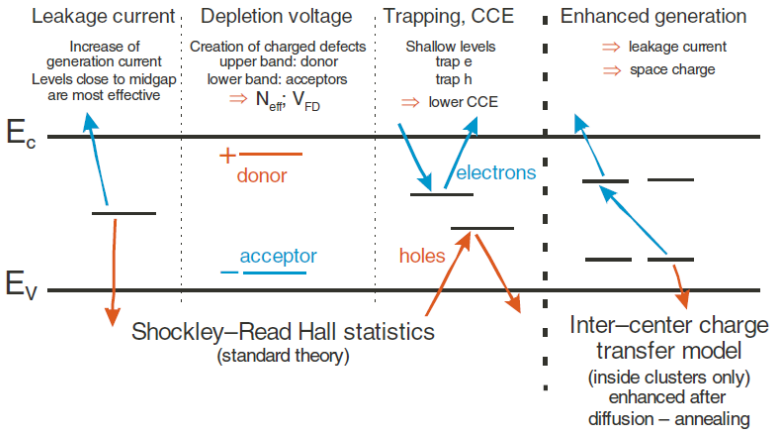


Fig. 2.14: Mechanisms induced by the creation of energy levels at the forbidden band, and its effect on the silicon detector performance [27].

On the other hand, the creation of mid-gap states after irradiation also increases the device leakage current proportionally to the fluence, and has been found experimentally [35] that its relation can be expressed as

$$\Delta I = \alpha \Phi V \tag{2.2}$$

where ΔI is the difference between the leakage current after and before irradiation, V is the active volume of the detector, and α is a proportionality factor called *current related damage rate*. The increase in leakage current caused by radiation has a direct influence on the detector performance, as the device will have a higher power consumption, leading also in some cases to the induction of thermal runaway.

At the current LHC fluences, around 10^{14}-10^{15} n_{eq}/cm^2, α is independent of the silicon type and doping concentration and its value is in the range 4-5$\cdot 10^{-17}$ A/cm ([36], [37]). However, for very high fluences (>10^{16}), similar to the expected in the HL-LHC upgrade, a saturation of α has been observed [38], as shown in Figure 2.15.

2.3.3 Annealing Effects

The detector damage is influenced by the temperature at which the device is kept. Radiation-induced defects might recombine, e.g. an interstitial impurity can fill a lattice vacancy if the temperature provides enough energy to surpass a certain activation energy barrier, and even complexes may dissociate into their components. This effect is called *short term* or *beneficial annealing*, and may significantly improve the detector characteristics after irradiation. However, in the long term, defects electrically inactive can interact and become active, inducing what is known as *reverse annealing* effect [33].

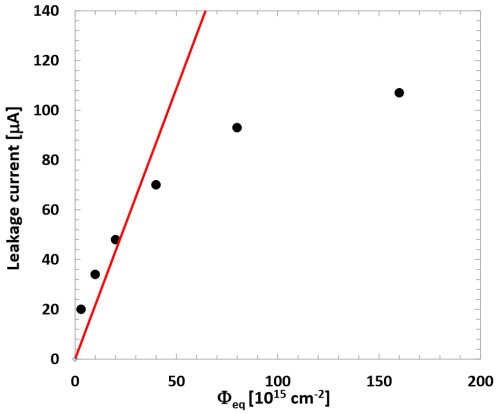


Fig. 2.15: Saturation of leakage current at very high fluence. Figure from [38].

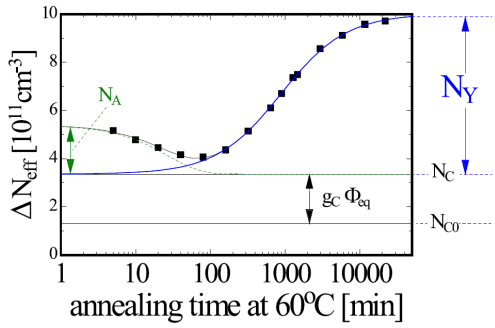


Fig. 2.16: Effective doping concentration, of a PiN diode irradiated up to $1.4{\cdot}10^{13}$ cm^{-2}, as a function of the annealing time at 60°C. Figure from [33].

In consequence, the time dependence of N_{eff} can be parametrized as

$$\Delta N_{eff}(t) = N_C + N_A(t) + N_Y(t) \tag{2.3}$$

where the component N_C is the *stable damage*, not dependent of time, and the N_A and N_Y are the time-dependent beneficial and reverse annealing effects, respectively. Figure 2.16 presents the evolution of the effective doping concentration as a function of the annealing time at 60°C, showing a reduction of the change in space charge at times below 100 min, and the later reverse annealing effect. Consequently, given the temperature dependence of the processes, HEP silicon detectors are kept at low temperatures to delay the reverse annealing effect. Additionally, as the space charge change reaches a minimum after the short-term annealing, the main HEP experiments have established a standard annealing of 80 min at 60°C for tests performed on irradiated silicon sensors. All the post-irradiation measurements presented in this thesis were performed after the sensors were exposed to this standard annealing.

2.4 Test Methods

This section describes the basic test methods used in this thesis to evaluate the characteristics of the silicon strip detectors. Detailed information is provided on how to test fundamental parameters, such as the leakage current or the full depletion voltage, and to assess the inter-strip characteristics and the performance of single strips, measuring key parameters such as the coupling capacitance, strip implant/metal resistance, bias resistance, etc. Particularly, for the ATLAS Inner-Tracker (ITk) strip sensors, all the tests before irradiation should be performed at 20ºC, and after irradiation at -20ºC, with the sensors in a dry environment (<10%). The aim of this section is to provide a general view of the test methods to be used for a complete characterization of silicon strip detectors. Specific values for each test method and parameter limits will be provided in Chapter 5, where ATLAS strip sensors will be characterized, and the results compared with the specifications.

2.4.1 Leakage Current and Bulk Capacitance Characteristics

The characterization of the device leakage current and bulk capacitance is fundamental for the evaluation of the quality and performance of the silicon detector. Current-Voltage (IV) curves provide valuable information of the breakdown voltage and current, which is directly related to power consumption and noise of the detector. The leakage current is generated in the bulk and it is directly related to the existing electric field and defects, caused by radiation or production issues, and its magnitude should be kept as low as possible. On the other hand, Capacitance-Voltage (CV) measurements provide information about the effective doping concentration and full depletion voltage apart from full capacitance at operating voltage which affects the detector noise.

In n-on-p silicon strip sensors, the leakage current measurement is performed connecting the bias rail and the backplane of the detector to the low and high outputs of a Source-Measure Unit (SMU), respectively. Then, a reverse bias voltage sweep (V_{bias}) is applied and the current is measured. Alternatively, the voltage sweep can be also performed in the guard ring with the objective to evacuate surface currents, leading to a higher accuracy on the measurement of the bulk leakage current. Figure 2.17 shows a schematic representation of the test configuration and typical IV curve obtained. When the voltage starts to increase, the silicon bulk is being depleted and the leakage current increases accordingly until the full depletion voltage (V_{fd}) is reached. Additionally, a steady increase in the leakage current may occur around the full depletion voltage depending on the amount of defects present on the surface layers. Voltages higher than V_{fd} will generate only a low increase of the leakage current until the avalanche

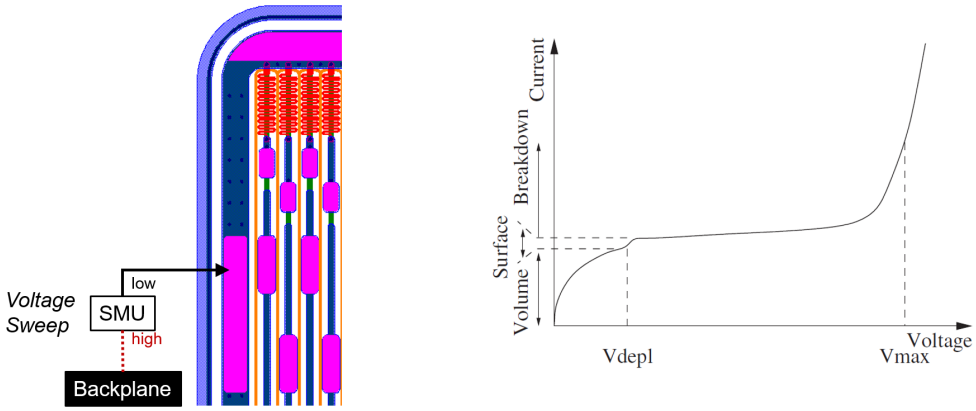


Fig. 2.17: Current as a function of the reverse bias voltage (IV). Test method (left) and typical IV curve [40] (right).

breakdown is produced at the breakdown voltage (V_{bd}). The breakdown is usually due to charge multiplication in charge collisions with the lattice under the high electric field, or by *Zener breakdown*, caused by *tunnel effect* [39]. Silicon strip detectors should be designed and fabricated to fulfil the condition $V_{bd} \gg V_{fd}$, since they need to be operated with their active volume fully depleted and, as explained in Section 2.3, the radiation-induced bulk damages will increase the V_{fd}.

Similarly to the IV test, the bulk capacitance measurement is performed using the same configuration, but connecting an LCR meter to measure the evolution of the capacitance as a function of the applied voltage. Additionally, as the LCR meter needs to apply a small AC signal to measure the capacitance, and most LCR meters are not able to provide the high voltages needed, a decoupling box is normally used to isolate the voltages applied by both sources, allowing the acquisition of the bulk capacitance values. An *open correction* measurement should be done prior to the CV measurement in order to avoid the introduction of parasitic capacitances from the setup circuitry. An RC-series configuration is used for this measurement. According to the requirements of the ATLAS ITk collaboration, the frequency of the measurement should be 1 kHz before irradiation, and lower frequencies should be used if the test is performed on irradiated devices at lower temperatures, e.g. 400 Hz at -10ºC and 200 Hz at -20ºC. Then, a reverse bias voltage sweep is applied to the silicon strip detector and the depletion zone increases in volume, with the consequent increase in capacitance, until the full depletion voltage is reached and the capacitance remains constant for all voltages. Alternatively, the CV measurement can be also performed applying the voltage sweep at the same time in the guard ring. As for the IV test, the accuracy of the measurement will be higher, since it will enhance the definition of the electric field in the depleted region. Figure 2.18 shows a schematic representation of the test configuration method

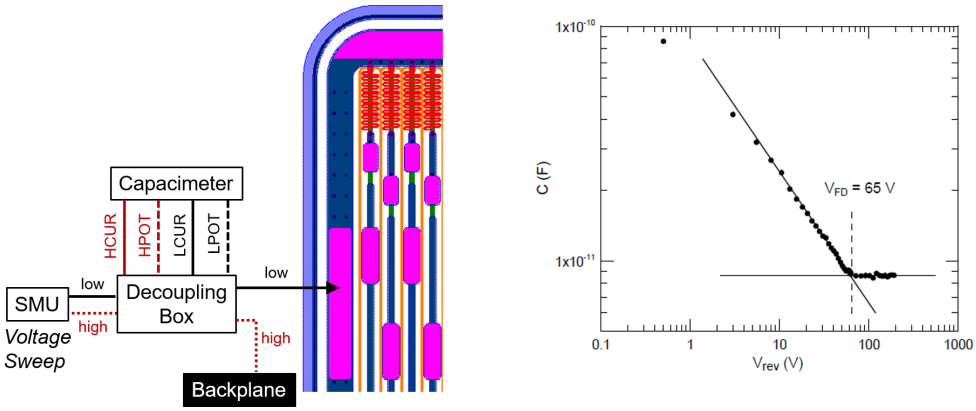


Fig. 2.18: Bulk capacitance as a function of the reverse bias voltage (CV). Test method (left) and example of full depletion voltage extraction [42] (right).

and an example of the typical CV curve obtained. This behaviour can be modelled as a parallel plate capacitor, where the capacitance can be expressed as

$$C_{bulk} = \begin{cases} A\sqrt{\frac{q\epsilon|N_{eff}|}{2V_{bias}}} & V_{bias} \leq V_{fd} \\ A\frac{\epsilon}{W} & V_{bias} > V_{fd} \end{cases} \tag{2.4}$$

where A is the area of the pn-junction, ϵ is the permittivity of the silicon bulk and W is the depletion depth. An example of the full depletion voltage extraction is presented in Figure 2.18, where the values are represented as log(C) vs. log(V), although C^{-2} vs. V plots are also used. The capacitance behaviour before and after the full depletion is reached can be described with two linear fits. Then, the full depletion voltage can be obtained experimentally at which these two fits intersect [41]. The full depletion voltage is directly related to the resistivity of the wafer substrate, as discussed in Section 1.3.2, so the effective doping concentration of the silicon bulk can be obtained from Equation 1.7.

As reference, ATLAS silicon strip detectors for the HL-LHC upgrade[6] are intended to have leakage currents in the order of tens of nA/cm^2, with a depletion voltage around 350 V, and breakdown voltage above 700 V.

2.4.2 Inter-strip Characteristics

In segmented tracking detectors, such as silicon strip sensors, the resistance and capacitance between neighbouring electrodes play a key role in the final performance of the device. High inter-strip resistance (R_{int}) values will be an indication of good strip isolation, that avoids unwanted effects such as signal sharing. The signal quality

[6] ATLAS Specifications for the HL-LHC upgrade are detailed in Section 5.1.

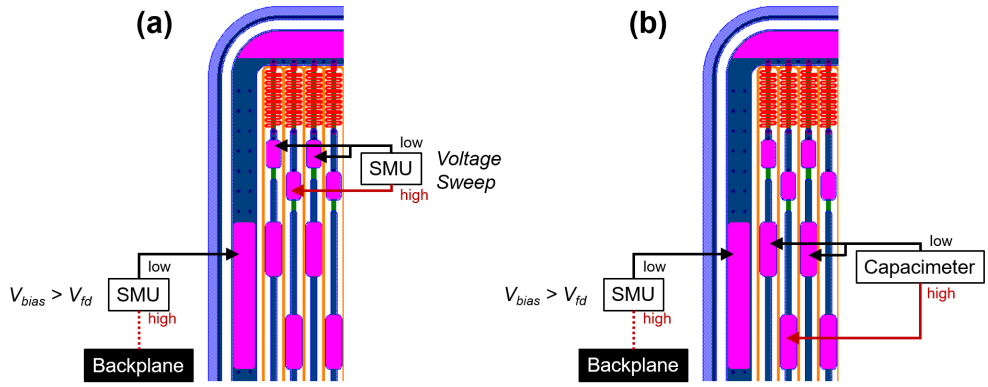


Fig. 2.19: Inter-strip resistance (a) and inter-strip capacitance (b) test methods.

can be also compromised by the inter-strip capacitance (C_{int}), since it will directly affect the signal-to-noise ratio in the readout electronics. In order to get the most of the signal into the readout preamplifier, the capacitance between neighbouring strips should be much smaller than the coupling capacitance. Inter-strip considerations should be carefully addressed adapting the sensor layout, i.e. p-stop and strip pitch, and fabrication processes, i.e. quality and thickness of the oxides, to optimize the performance of the silicon strip detectors, especially after high radiation fluences.

Schematic representations of the inter-strip resistance and inter-strip capacitance test setups are shown in Figure 2.19. Both measurements are performed considering the first neighbouring strips at both sides of the strip under test, using the DC pads (contacting the strip implant) for the resistance measurement[7], and the AC pads (contacting the strip metal) for the capacitance. The silicon bulk should be fully depleted prior to these measurements, so a second voltage supply is needed using the configuration shown in Figure 2.17. Then, for the inter-strip resistance test, a voltage sweep is applied to the strip implant under test and the leakage current is measured in the neighbouring implants, obtaining the resistance from the inverse slope of the IV curve. Similarly, for the inter-strip capacitance, a voltage sweep is applied to the central strip metal but this time an LCR meter, in RC-parallel configuration and a test frequency of 100 kHz, is used to measure the capacitance between the readout metals.

Inter-strip resistance values in the order of GΩ/cm and inter-strip capacitance below 1 pF/cm are recommended by the ATLAS collaboration to ensure a proper performance of the silicon strip detector.

[7]The inter-strip resistance set-up can be also used to test the bias resistance if the leakage current is also measured in the strip under tests. Bias resistance measurement is explained in Section 2.4.3.

2.4.3 Single Strip Characteristics

Single strips are the basic units of silicon strip detectors, so their individual performance has a direct impact on the tracking efficiency of the device. As shown previously, on AC-coupled strip detectors there is a thin oxide layer between the strip implant and the readout metal. Ideally, the coupling capacitance should be large to collect and drive to the readout as much signal as possible. To achieve this, the isolation oxide layer should be thin, without compromising the fabrication reliability, and of high quality to prevent the appearance of conducting channels between the implant and the metal, so-called pinholes. Moreover, the resistance of the strip implant and strip (readout) metal should be also carefully controlled so it does not exceed a certain threshold that could affect the mobility of the signal charges. Similarly, the total resistance of the polysilicon bias resistor should be also within a range to keep the strips at the same potential but, at the same time, prevent the signal discharge through the grounded bias ring. Additionally, the silicon strip detectors designed and characterized in the framework of this thesis are equipped with a beam-loss protection based on the punch-through effect. The *Punch-Through Protection* (PTP) is achieved by reducing the distance between the strip implant and the bias rail implant at the bias resistor side of the strip. In an hypothetical beam-loss scenario, the large amount of charge accumulated in the silicon bulk will be evacuated through the bias implant when a certain voltage threshold (punch-through voltage) is reached, preventing the appearance of irreversible damages on the coupling capacitor[8]. Consequently, this protection should be also carefully evaluated measuring its punch-through effective resistance and voltage.

Figure 2.20 shows a schematic representation of the test method to measure the coupling capacitance (C_{coupl}) of a single strip. The high and low outputs of an LCR meter are connected to the DC pad (strip implant) and the AC pad (strip metal) of the strip under test. The capacitance is measured at 1 kHz with RC-parallel configuration, and for an ATLAS ITk strip sensor, its value should be in the order of 20 pF/cm or above.

In order to test the resistance of the strip implant ($R_{implant}$), the high and low outputs of a SMU should be connected to the DC pads of the same strip. A voltage sweep is applied and the leakage current is measured, extracting the resistance value from the inverse slope of the IV curve. Similarly, the strip (readout) metal resistance (R_{metal}) can be measured with an identical configuration and procedure, but connecting the AC pads of the strip, instead of the DC pads. Figure 2.21 shows a schematic representation of both measurements. Acceptable resistance values are in the range of kΩ/cm for the strip implant, and Ω/cm for the readout metal.

[8] Details of *Punch-Through Protection* (PTP) structure are presented in Section 3.2.7.

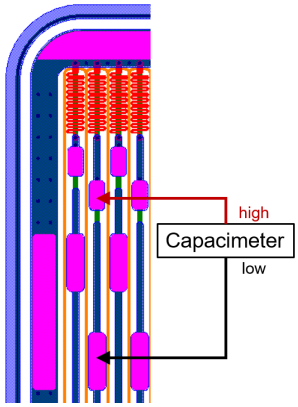


Fig. 2.20: Coupling capacitance test method.

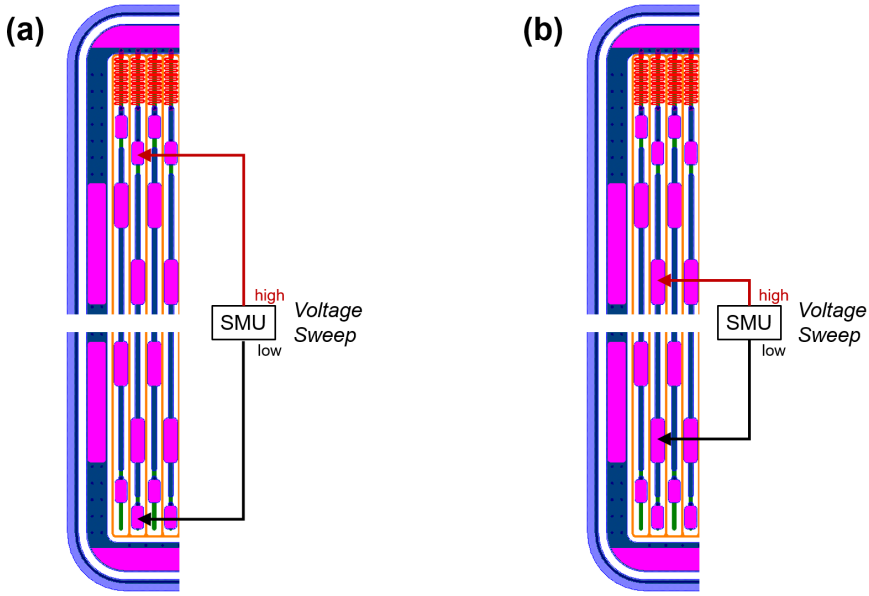


Fig. 2.21: Strip implant resistance (a) and strip metal resistance (b) test methods.

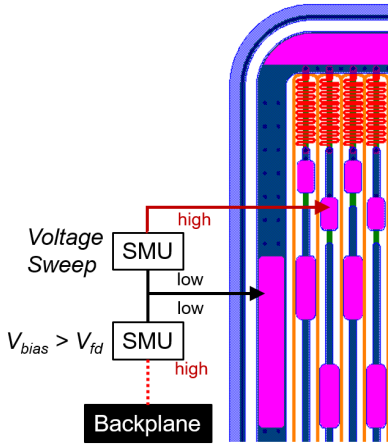


Fig. 2.22: Punch-through voltage test method.

On the other hand, the inter-strip resistance test method shown above (Figure 2.19(a)) can also be used to measure the polysilicon bias resistance. Besides the leakage current induced in the neighbouring strips, the voltage sweep applied to the strip under test will also induce a leakage current in the same strip. Then the IV curve obtained can be used to calculate the bias resistance from its inverse slope, with recommended values in the order of a few MΩ.

Finally, the effectiveness of the Punch-Through Protection (PTP) structure can be evaluated measuring the evolution of the resistance between the strip implant and the grounded bias rail when a voltage is applied to the strip implant (Figure 2.22). The strip sensor should be fully depleted applying a reverse bias voltage to the backplane and leaving the bias ring grounded. A test voltage V_{test} is applied to the DC pad (strip implant), and the induced current I_{test} is measured between the strip implant and the bias ring. The effective resistance R_{eff} can be calculated from the equivalent circuit composed by the bias resistance in parallel with the punch-through resistance [43], and consequently is given by

$$R_{eff} = \frac{V_{test}}{I_{test}} = \left(\frac{1}{R_{bias}} + \frac{1}{R_{PT}} \right)^{-1} \tag{2.5}$$

where R_{PT} is the punch-through resistance between the strip implant and the bias rail. From there we can extract the punch-through voltage (V_{PT}) for the condition $R_{PT} = R_{bias}$, i.e. $R_{eff} = R_{bias}/2$ [44].

3 Design of Silicon Strip Detectors

The particle tracking detectors in the forthcoming High-Luminosity Large Hadron Collider (HL-LHC) will be exposed to unprecedented adverse conditions, especially at the inner trackers of the main experiments. With the first layers at a radius of just 30 cm from the particle beam, the new strip sensors should be designed with the objective to operate at high performance over the lifetime of the experiment. Simulations of the accumulated radiation fluences expected in the HL-LHC (Figure 1.6) revealed the necessity to replace the p-on-n technology currently used by a new generation of n-on-p strip sensors with a higher radiation hardness. Moreover, the planned increase of the instantaneous luminosity in the HL-LHC will also require a higher segmentation, i.e. higher number of strips per sensor, in order to reduce the high occupancy (*pile-up*) expected. The hermeticity of the new ATLAS sensors will also be optimized minimizing the inactive regions at the edge of the sensors and fabricating the devices in 6-inch substrates, instead of 4-inch, and making use of the maximum area available. In addition, the new ATLAS strip modules will be arranged in *Staves* and *Petals* in the *Barrel* and *End-cap* regions, respectively, in contrast to the use of individual modules currently installed in the detector. In consequence, the design of the new generation of strip sensors should be carefully reformulated to optimize its characteristics and performance to meet the novel requirements.

This chapter introduces the basic concepts used for the layout design of microelectronic devices (Section 3.1), and presents a detailed study of the different components of the n-on-p silicon strip sensors (Section 3.2), discussing the improvements that can be achieved optimizing the layout design.

3.1 Layout Design

Layout concepts and design rules are directly related to the characteristics and limitations of the photolithography technique. A general view of this fabrication process, the use of photomasks and the different parameters involved is firstly introduced, with the objective to understand the layout design of single device structures and integrated circuits.

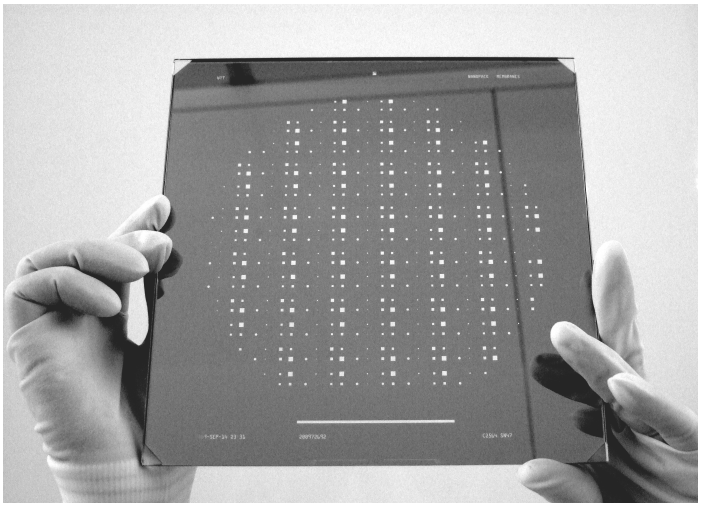


Fig. 3.1: Photomask fabricated on a glass plate with patterns on a chromium layer of 100 nm thick. Figure from [28].

3.1.1 Photolithography and Masks

Photolithography (or *optical lithography*) is a microfabrication process which uses ultraviolet (UV) light to expose photosensitive film (called *photoresist*) through photomasks to define patterns. One particular mask is used for each photolithographic step. Masks contain chromium patterns of around 100 nm thickness on a glass plate to block UV light in selected areas (Figure 3.1), forming all the patterns in the photoresist simultaneously, with typical exposure times in the order of a few seconds. If the regions corresponding to the elements to be defined are transparent (exposure areas), with the rest covered by chromium, it is said that it is a *dark-field* mask. On the other hand, if the regions to be defined in the device are masked, with the other regions exposed, it is called *bright-field* mask. Then, the UV light generates photochemical reactions in the resist, making the exposed areas soluble for *positive resists* or hardening the exposed areas if a *negative resist* is used[1]. Then, a selective removal of the photoresist (*development*) can be performed, and the areas of the underlying material can be processed differently, e.g. implanted, etched, etc. Finally, the resist covering the underlying material not processed is removed. Figure 3.2 shows an example of oxide pattern generation using the photolithography technique.

The first photomasks were hand-drafted using graphical black crepe tape on mylar media for photo imaging, originally calling the overall process *tapeout* (Figure 3.3). For historical reasons, the term *tapeout* is still used to describe the photomask fabrication process using the electronic file provided by the layout designers.

[1] It is worth noting that, when negative resist is used, dark-field masks will act as bright-field masks, and vice versa.

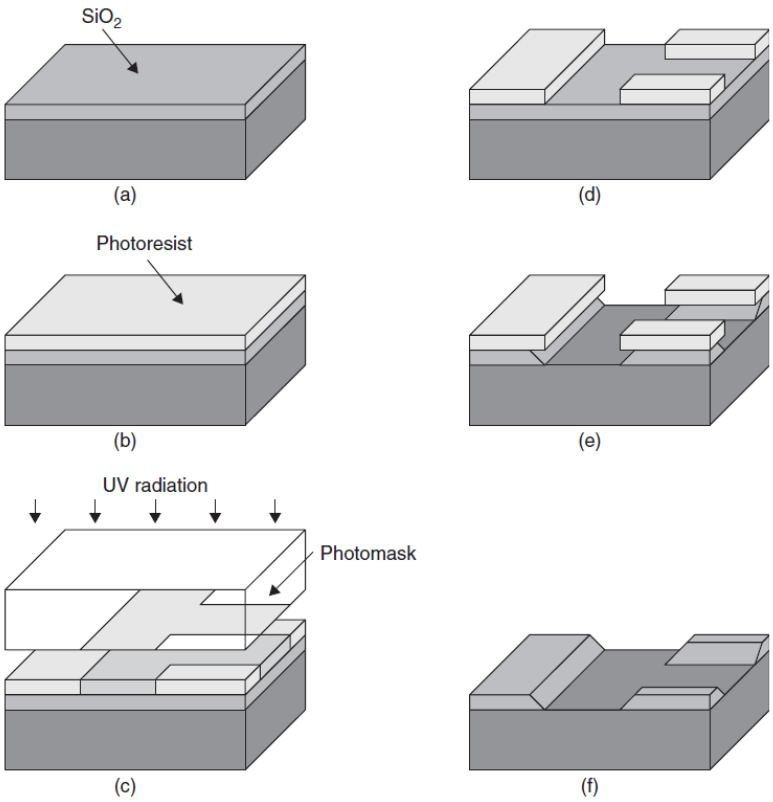


Fig. 3.2: Example of oxide pattern generation using photolithography technique: (a) oxide film deposition; (b) resin film application; (c) UV exposure through a photomask; (d) development of resin patterns; (e) oxide etching; and (f) resin removal. Figure from [28].

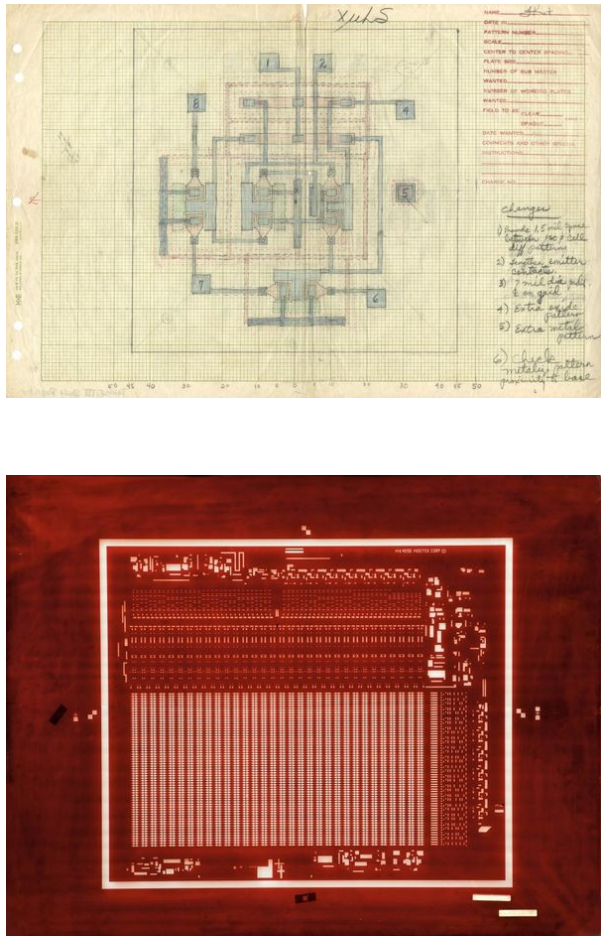


Fig. 3.3: (top) Example of an electrical schematic that is translated into geometric shapes that create equivalent physical circuits on the wafer (Fairchild Micrologic "S", 1960) [45]. (bottom) Example of a mask layer prepared for photographic reduction onto a glass plate. The design was transferred to the Rubylith film and selected areas cut and stripped by hand to create the pattern (Mostek MK4096 4K DRAM, 1976) [46].

Fig. 3.4: Photomask (left) is translated and rotated below the photomask (middle) to match the alignment marks (right). Figure from [28].

The fabrication of integrated circuits usually requires several photolithographic steps, each one requiring one mask level. The patterns already present on the wafer should be accurately aligned to the patterns of the new mask level, representing one of the most critical steps in the fabrication. For this purpose, alignment marks are usually included in each of the mask levels. The alignment is performed introducing the wafer and the mask into the mask aligner, where the wafer is translated and rotated below the mask to match the alignment marks and therefore, the previous patterns present in the wafer (Figure 3.4).

Besides the alignment step, the resolution of the photolithography process will be also highly influenced by the exposure step [47]. The wavelengths and energy of the light used will require considerations on the photoresist thickness and exposure times needed to trigger the photochemical reactions and obtain resist walls as vertical as possible after the development step. The exposure can be performed with the mask in contact with the resist (*contact lithography*) or with a small gap in-between (*proximity lithography*), typically in the order of a few microns. Then, the distance between the wafer and the mask will also influence the resolution of the final patterns, as reflection and diffraction effects will expose the resist underneath the opaque parts of the mask and will generate resist walls with a certain slope, positive or negative depending on the photoresist type used (Figure 3.5). In addition, equipment vibrations during the exposure process will affect the exposition of the photoresist in the edge of the masked regions, deteriorating the resolution of the patterns defined. The minimum resolvable linewidth [48] can be calculated from Fresnel diffraction and approximated by

$$linewidth \approx \sqrt{\lambda(g + \frac{d}{2})} \tag{3.1}$$

where λ is the wavelength of the exposing radiation, g is the gap between the resin and the mask, and d is the photoresist thickness.

Consequently, the mechanics, the optics, the chemistry of the resist and the mask alignment will play a key role in the resolution achieved by the photolithographic process. This is one of the main drivers of the “minimum feature size”, which is one

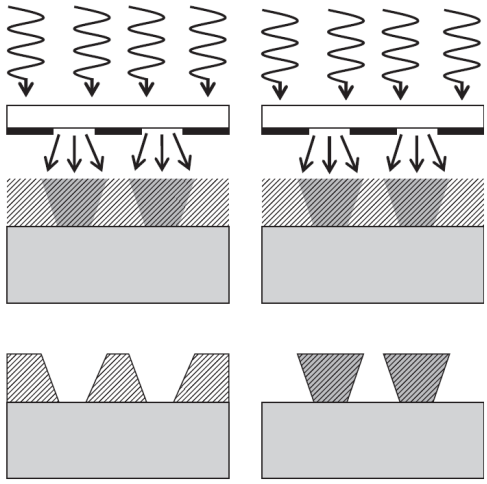


Fig. 3.5: Influence of light diffraction at the pattern edges of the mask on the profile of the positive (left) and negative (right) photoresists. Figure from [28].

of the key parameters of any technology or process. The limitations introduced by these elements will directly influence the design of the masks (the layout) used for the photolithographic process, establishing the design rules.

3.1.2 Layout Concept

The layout of an integrated circuit is the bidimensional projection of the tridimensional device configuration using planar geometric shapes to define the elements of the different layers that conforms the device. Each layer corresponds with one photomask level used in a photolithographic step, where the geometric shapes are used to define patterns on the wafer that can be selectively processed, e.g. doped or etched, to generate different device elements and their interconnections, as discussed in the previous section.

In CMOS technology, four basic layer types can be distinguished: conductors (e.g. metal, polysilicon), isolators (e.g. oxides), contacts/vias and doped layers (e.g. n-type or p-type). Isolation layers, such as grown or deposited oxides, are used to isolate the conducting layers. These conducting layers are connected through the isolation layers using contacts or vias. Doped layers, on the other hand, change locally the conductivity properties introducing donor (p-type) or acceptor (n-type) ions into the layer. The number of layers designed is usually minimized in order to reduce the mask-making cost and the errors associated with the mask manipulation.

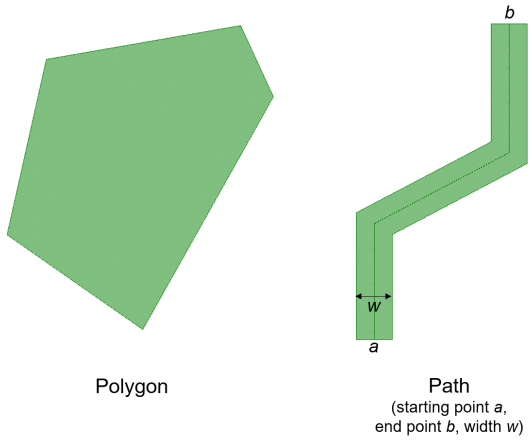


Fig. 3.6: Example of a polygon shape with six vertices and a path shape. Paths have associated a starting point (a), an end point (b) and a path width (w).

3.1.3 Design Approaches and Tools

Two different approaches can be used for the layout design: *semi-custom* or *full-custom*. In the semi-custom approach, the layout design is made using predefined building blocks (cells) containing basic common elements from libraries. This approach speeds-up the design phase, reducing also the cost, but allowing less control over the different device elements. In contrast, in full-custom design, all circuits are hand-crafted by the designer allowing the use of special circuit styles and arbitrary sizing of the different elements, but considerably increasing the design cost and time. A full-custom approach is used in this thesis to design silicon strip detectors, since the characteristics of the devices should be accurately adapted and controlled to fulfil the specifications established by the collaboration, in order to achieve the expected performance for the lifetime of the HL-LHC.

Computer-aided design (CAD) tools [49] are commonly used to draw the mask layouts, and the Graphics Database System (GDS) [50] format is widely used by semiconductor industries to digitally store the layouts. The electrical schematic of the circuit and the different device elements are translated into geometrical shapes using polygons and paths (Figure 3.6) to define areas and connections, respectively. Depending on the objective, the use of polygons or paths can be more appropriate to facilitate the design process. Polygons can have multiple different shapes and can enclose complex areas, whilst paths are limited by a given starting point, an end point and a path width. However, paths are usually easier to manipulate, changing the different characteristics, while modifications on complex polygons trend to be tedious. Paths also have an attribute to control the shape of the start/end terminations, that can be square or round with different variants (Figure 3.7).

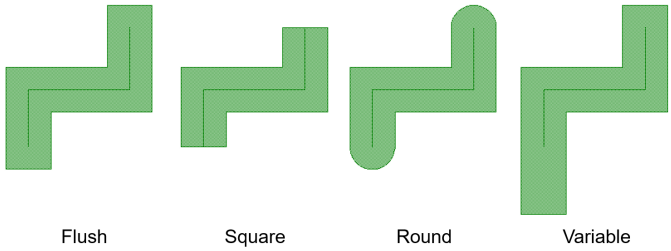


Fig. 3.7: Example of a different path terminations.

3.1.4 Design Rules

In the process of designing a layout there is a set of rules that have to be respected by all the layout objects. Two groups of design rules can be distinguished: *technological rules* and *device rules*. Technological rules are usually defined by the foundry in charge of the fabrication, and are directly related to the physical limits of the manufacturing process, such as the photolithographic resolution or the dopant lateral diffusion. On the other hand, the aim of the device rules is the definition of the different device elements needed to achieve the performance requirements, such as the pad dimensions or the length/width of the isolation structures. In contrast to the technological rules, the device rules are usually established by the customer, e.g. ATLAS or CMS collaborations, since they are related to the characteristics of the device elements needed to achieve the expected performance (specifications).

Technological Rules:

Technological design rules are a direct consequence of the physical limits of the different fabrication steps needed for a certain technology, and thus depend on the manufacturer equipment and processes. The limitations established are the result of a deep knowledge of the possible variations that can be produced during the fabrication.

As previously discussed, the dimensions of the elements (patterns) defined in the wafer surface by the photolithographic process have a strong dependence on the wavelength/energy of the exposure light, the photochemical reactions induced in the resist, the gap between the wafer and the mask, and in general the mechanics and optics used. Small variations on these parameters can induce deviations on the dimensions of the transferred patterns, since areas that should not be processed will not be properly protected due to diffraction effects (Figure 3.5) or defective resist developments. In addition, the mask alignment is a critical step in the photolithographic process, especially in technologies such as the strip detectors with a high number of mask levels. Technological design rules should consider the expected misalignments, and

their statistical propagation throughout several photolithographic steps, to take into account the possible deviations in the relative position between elements.

Beside the physical limitations associated with the photolithographic steps, other fabrication processes can introduce variations on the final device elements that should be controlled to establish safety technological design rules. The high temperatures usually used during the fabrication will induce a lateral diffusion of the dopants used to create the different doped areas. The etching processes, on the other hand, have a strong dependence on the layer material and thickness, that can result on elements with higher or lower dimensions, if an over- or under-etch is produced.

Consequently, minimum layer dimensions, separations between layers and mask alignment sequences should be established by the manufacturer in the technological design rules to avoid major deviations that can become critical for the device performance. Each layer and each combination of layers have its own rules, that can be classified in three general groups:

Width Rule: Minimum width of an individual layer. The width rule is usually defined considering the maximum resolution that can be achieved by the photolithographic steps and the precision of the etching processes. A violation of the width rule usually results in an open circuit in the corresponding layer, showing breaks or shapes with undesired narrowed parts. Similarly, the width rule has to be applied also for the length of an object, normally detailed in the design rules as the minimum area that a shape can have in a particular layer.

Separation Rule: Minimum separation between different layout objects. In this case, beside the photolithography resolution and the etching precision, the separation rules should take into account also the dopant lateral diffusion. A violation of this rule may result in a short circuit caused by the union of different objects. The separation rule has to be defined for objects from the same layer, but a minimum separation can also be defined for objects from different layers if they are technologically related (for instance, p- and n- dopings of the same substrate).

Overlap Rule: Minimum overlap of one object by another from a different layer. This rule always involves objects from different layers, and is defined to compensate for possible misalignments between layers or variations on the element dimensions caused by defective resin coverages or over-/under-etching of the processed material, that can induce technological errors (for instance que metal coverage of a via to an underlying metal).

Figure 3.8 illustrates the width (w), the separation (s) and the overlap (o) rules, showing also some examples of rule violation that should be avoided. On the other

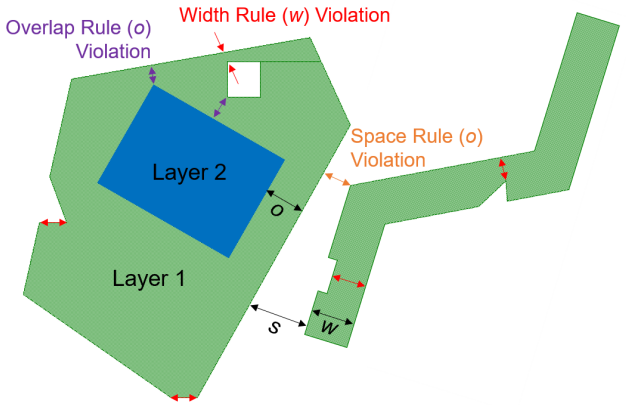


Fig. 3.8: Three objects from two different layers (green and blue) showing different examples of width (red), space (orange) and overlap (purple) rule violation.

hand, it is worth noting that objects with angles below 90º infringe the width and/or the separation rules and, consequently, are usually not allowed.

Most of the design rules presented above, especially the ones involving different layers, are a direct consequence of the minimum misalignment expected and its propagation after several consecutive photolithographic steps. The alignment sequence is also defined in the technological design rules and determines which layers are aligned to each other. Layers are not necessarily always aligned to the previous layer, but to some technologically-related previous layer, e.g. contact layer will be aligned to the n-implant layer, even if other layers were implemented after the n-implant layer.

Device Rules:

Device design rules establish the shape, the dimensions and the position of the different device elements. In this case, the customer, e.g. ATLAS or CMS, is in charge of their definition considering the device required performance, and maybe also other aspects such as the assembly, the operation and the lifetime intended for the device. These requirements are usually included in a specifications document that should be evaluated by the manufacturer to find possible incompatibilities with the technological design rules.

Typical device design rules include the definition and location of the pads, the active and die areas, the isolation structures, the dicing streets or the identification labels, among others. Additionally, test structures and diodes can be defined in the device rules and their distribution along the wafer.

It is worth mentioning that the device rules are usually defined as the final dimensions and position of the fabricated devices, not of the layout objects. Due to the possible deviations discussed above (e.g. metal overetch, dopant lateral diffusion, etc), the manufacturer can introduce modifications in the layout in order to compensate for these deviations and obtain devices which fulfil the requirements established in the device rules.

3.2 Advanced Design of Silicon Strip Detectors

The general layout design concepts discussed above can be applied now to the design of silicon strip detectors for High Energy Physics (HEP) experiments. Silicon strip detectors are widely used for particle tracking purposes at the inner sections of the main detector experiments, as discussed in Chapter 2. The most basic elements in these devices are the strips, which are long and narrow diodes. Typical silicon strip detectors contain several hundreds (even thousands) of strips, usually arranged in parallel and isolated from their neighbours, within a concentric biasing ring that keeps all the strips at the same potential using dedicated biasing structures, such as polysilicon resistors. The bias ring defines the active area of the device, and its volume is depleted applying a reverse bias voltage between the frontside bias ring and the backplane electrode. Additional structures, such as guard rings and edge implants, are usually included at the detector edge region to shape the electric field between the bias ring and the sensor physical edge in order to increase the breakdown voltage of the device.

The layout design carried out in this thesis for the silicon strip detectors is based on the *full-custom* approach, previously introduced in Section 3.1.3. The high-performance expected for HEP detectors requires an optimization of the sensor characteristics at the highest possible level, only accessible through the full-custom design approach. The characteristics of the different device elements are established by the sensor collaboration, in order to achieve the desired performance during the lifetime of the experiment. On the other hand, the technological design rules are defined by the foundry in charge of the massive production, depending on the limitations of the different fabrication processes. Thus, both design rules should be carefully assessed and balanced during the layout design stage to obtain the best possible device performance. However, it is worth noting that due to the large size of the silicon strip detectors used in HEP experiments, the technological design rules do not reach the limits currently used for the last generation of microelectronic technologies. In this case, the main limitations and requirements are addressed to optimize the yield of the massive fabrication, since, in contrast to the standard microelectronics, each wafer contains only one device and several thousands of devices should be fabricated to cover areas of several m^2 at the detector inner trackers.

This section details the layout design process of the new generation of ATLAS silicon strip detectors. With the aim to meet the strict requirements of the forthcoming HL-LHC, the new sensors are designed using the n-on-p technology, to avoid the radiation induced inversion of the n-type bulk, with larger dimensions, also including improvements on the sensor edge termination (to improve the hermeticity) and protections against beam-loss accidents. Firstly, the different layers and alignment sequence are introduced, followed by a discussion of the different elements of the sensor with the aim to understand their influence on the device performance to optimize the layout design.

3.2.1 Layers and Alignment Sequence

Silicon strip detectors are fabricated layer by layer mainly using conductors, isolators, contact/vias and implant layers, over a low doped silicon substrate. The objects/patterns in each of these layers are transferred to the wafers by a photolithography process using a single photomask. Depending on the manufacturer and the characteristics of the silicon strip detectors, its fabrication usually requires between 7 and 9 photomask levels:

P-implant layer: Definition of p-type regions (*p-stops*) to isolate each strip from the neighbouring strips and bias ring (Figure 2.3). P-type regions can be also included in the guard ring and/or in the sensor edge to improve the control over the electric field. P-implant mask is usually the first photolithographic level in strip sensor technology.

N-implant layer: Definition of n-type regions (Figure 2.4). In n-on-p technology it is used to create the strip implants and the bias ring and guard ring implants.

Polysilicon layer: Definition of polysilicon bias resistors that will be used to connect the strip implants and the bias ring (Figure 2.6). This photomask level is usually aligned to the n-implant level, even if previous levels are used, in order to reduce de misalignment between the strip implant and the bias resistor.

Metal contact layer: Definition of areas where the oxide between the polysilicon bias resistor (and/or the n-implant) and the future metal will be etched, with the aim to fill it with metal and ensure their contact (Figure 2.7). Similarly to the *polysilicon layer*, this layer is also usually aligned to the n-implant level, instead of the previous level, with the objective to minimize critical misalignments between the strip implant and the readout metal contact.

Metal layer: Definition of metal objects, that will form the readout metal in each strip, the metal over the bias ring, guard rings and edge structure, and the final contacts and pads (Figure 2.8).

Second metal contact layer (*via*): Optional photomask level. Definition of areas where the oxide between the readout metal and the future second metal will be etched. Similarly to the *metal contact layer*, the regions without oxide will be filled with the second metal layer, ensuring the contact between the readout metal and the second metal. Thus, this level is only needed if a second metal layer will be included.

Second metal layer: Optional photomask level. Definition of second metal objects. In this thesis, this layer is used to incorporate (second) metal tracks routing the (first) readout metals to a new set of wire-bonding pads, as will be discussed in Section 3.2.8.

Passivation opening layer: Definition of areas where the passivation oxide will be etched, with the aim to have external access to the silicon strip detector through the AC, DC and bias metal pads (Figure 2.9).

Figure 3.9 shows, as an example, a diagram of the mask alignment sequence used for the fabrication of strip sensors in the cleanroom of Centro Nacional de Microelectrónica (IMB-CNM). In particular, the IMB-CNM design rules are formulated considering a maximum misalignment between layers of 1.25 μm, that represents 3 times the standard deviation (σ) or, in other words, the misalignment will be less than 1.25 μm with a probability of 99.7%. The propagation of the misalignment for consecutive layers is then calculated to be within 3σ, obtaining a maximum misalignment of 1.75, 2.25 and 2.50 μm for two, three and four consecutive mask alignments [51], respectively. In consequence, overlap rules can be extracted from the mask alignment sequence, establishing minimum overlaps between each pair of layers.

3.2.2 Strip Implant

In strip sensor technologies, the most fundamental element is the strip implant. It is the component that creates the basic diode in the bulk, and it is responsible to collect the charge induced by a particle crossing the sensor. In n-on-p sensors, the strip implants are highly-doped n-type regions on a low doped p-type silicon bulk, forming a p-n junction. The breakdown voltage is inversely proportional to the doping concentration of the bulk, with a maximum electric field per unit length of 30 V/μm [27]. The strip implant is usually designed using paths rounded at the start/end terminations (Figure 3.7), in order to minimize the electric field at the p-n junction that is directly influenced by sharp edges.

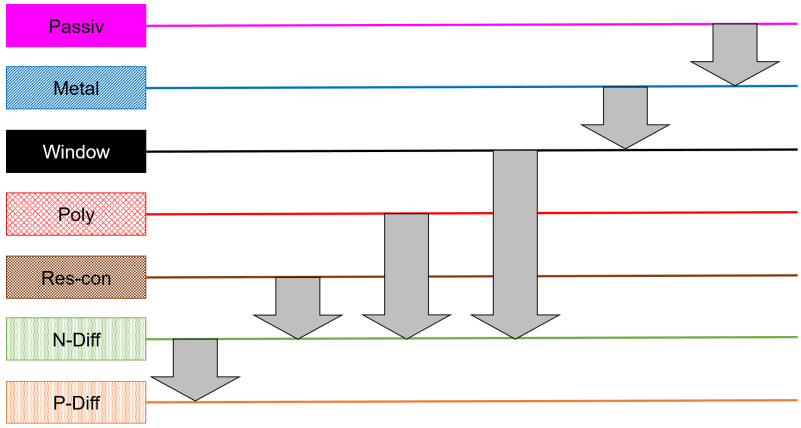


Fig. 3.9: Mask alignment sequence for the fabrication of strip sensors at IMB-CNM.

As will be discussed in Section 3.2.4, strip implants with larger width increase the coupling capacitance and, on the other hand, a high number of strips per sensor increase the spatial resolution of the tracking detector (highly-segmented sensors). Then, as the active area in each sensor is limited, both considerations should be balanced to find the optimal strip implant width. Similarly, the length of the strip implant should be balanced to have the maximum efficiency depending on the working conditions: longer strips will increase the collection ratio in the implant, but will increase the hit density (*occupancy*) per strip, reducing the efficiency of the tracking recognition and saturating the readout. In particular, ATLAS have balanced these effects defining strip implant lengths able to work in a pile-up scenario of up to 200 inelastic proton-proton collisions per beam crossing. On the other hand, the strip *pitch*, defined as the distance between the centres of two neighbour strips, will define the degree of segmentation of the sensor. A lower strip pitch (higher segmentation) will provide the sensor with a higher spatial resolution, but also the number of channels will be increased, hindering the assembly and the readout. In addition, in the extreme case, the minimum strip pitch that can be used will be influenced by the separation rule, as discussed in Section 3.1.4, since the lateral diffusion of the dopants in the strip implant can induce a short-circuit between neighbouring implants.

Typical values for the strip implant width and length used in HEP experiments are around 15-20 μm and 10-15 cm, respectively, with a strip pitch below 100 μm.

3.2.3 Inter-strip Isolation: P-stop and P-spray

The presence of fixed positive charges in the SiO_2 layers induce the appearance of an electron inversion layer in the Si-SiO_2 interface in p-type silicon substrates (Figure 3.10(a)). On n-on-p devices, the presence of an electron layer between the strip n-implants can increase drastically the inter-strip capacitance and reduce the inter-strip

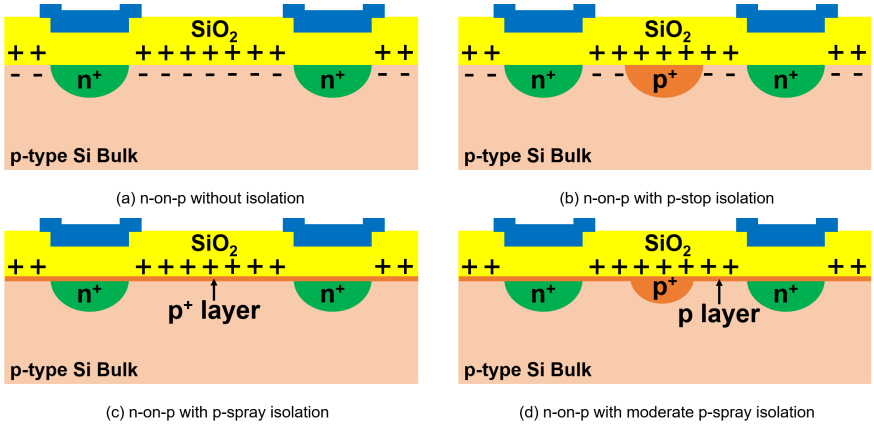


Fig. 3.10: Schematic cross-section of a n-on-p strip detector without isolation (a), with p-stop isolation (b), with p-spray isolation (c) and with moderate p-spray isolation (d).

resistance, or even can short-circuit neighbouring strips. As explained in Section 2.3, the positive charge density in the oxide increases with radiation [52], compromising the lifetime of the devices in HEP experiments. Consequently, the silicon surface of the n-on-p devices are usually isolated introducing p-type dopants to compensate the appearance of the electron inversion layer. For this purpose, two different approaches are commonly used on n-on-p technologies, so-called *p-stop* and *p-spray* [42].

The p-stop technique is based on the introduction of p-type floating regions in-between the n-implants to interrupt the inversion layer and isolate the neighbouring strips (Figure 3.10(b)). P-stops are usually designed as narrow paths that surround each n-implant, maximizing their separation from strip n-implants to avoid the induction of high electric fields. The use of p-stops to isolate strip implants introduces a new photolithographic step dedicated to the p-type implantation (p-implant layer in Section 3.2.1), increasing the cost of the overall fabrication process.

On the other hand, the p-spray technique introduces an uniform p-type layer in the whole silicon surface at the beginning of the fabrication process to compensate the inversion layer, covering completely the gap between n-implants without the introduction of new mask levels (Figure 3.10(c)). This technique allows the reduction of the gap between strips, and thus the strip pitch, increasing the spatial resolution of the tracking detector. However, it was observed that the dopant profile should be carefully calibrated to ensure a proper isolation and to avoid early breakdowns ([42], [53]). A third option to isolate the strips is a combination of p-stop and p-spray, so-called *moderate p-spray*. It consists in the introduction of a soft p-spray layer combined with a p-stop with a reduced width (Figure 3.10(d)).

Currently, the isolation of strips in n-on-p detectors for HEP experiments is done using p-stops, mainly due to the complexity to define doping profiles for the p-spray layer

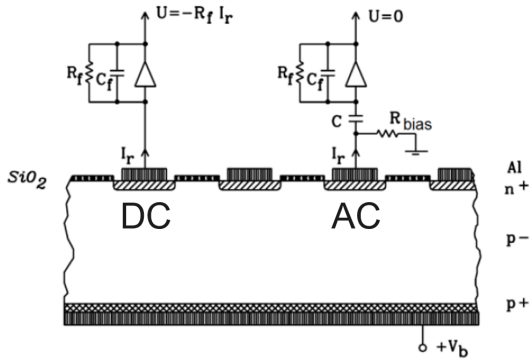


Fig. 3.11: Schematic representation of the AC and DC coupling modes. Figure from [54].

able to achieve high breakdown voltages on the strip detectors. Consequently, the strip isolation used for all the devices presented in this PhD thesis is done using the p-stop technique. In particular, the specifications of the strip detectors for the HL-LHC ATLAS upgrade establish that p-stops should have a width between 6 and 8 μm with an implant surface dose of approximately $4{\cdot}10^{12}$ ions/cm^2.

3.2.4 Readout Coupling

The signal generated by a particle crossing the strip detector is collected by the strip implant, that should drive it to the readout electronics. Two different approaches can be used to take out the signal to the readout chip: the direct coupling (DC) and the capacitive coupling (AC). In DC mode, the signal is taken directly from the strip implant, with the advantage to be technologically simple and cheap. On the other hand, in AC mode a dielectric material, e.g. SiO_2, is used between the strip implant and strip metal to create a parallel plate capacitor, transfering the signal to the readout electronics through a coupling capacitance.

As can be seen in Figure 3.11, in DC mode all the reverse leakage current (I_r) is driven directly to the readout, while in AC mode only the AC part of the I_r goes to the readout, and the DC part is evacuated through the bias circuit. In addition, a clear advantage of the AC mode respect to the DC mode, is that the dielectric layer shields the readout system from dark currents, that can lead to pedestal shifts, reduction of the dynamic range and may even saturate the electronics [54]. Thus, DC mode is simpler and cheaper than AC, but the readout electronics are more exposed.

Strip detectors usually have implemented both AC and DC pads (Figure 3.13), where the AC pads are used for the readout of the detectors assembled in modules, whilst the DC pads can be used to contact the strip implant and test some particular parameters of the strip, such as the inter-strip resistance or the strip implant resistance.

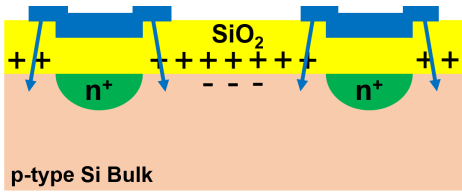


Fig. 3.12: Schematic representation of the influence of strip metal overlap in the electron accumulation layer near the strip implants.

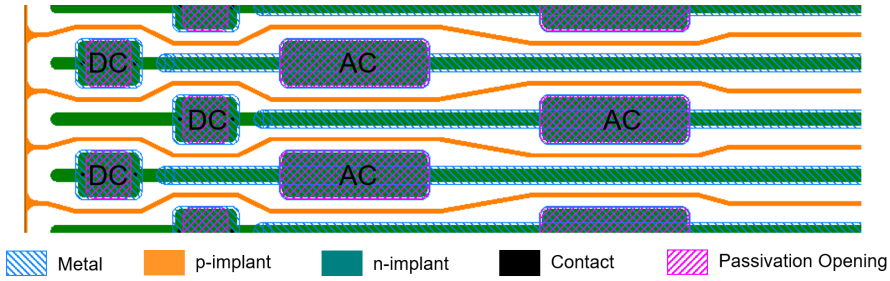


Fig. 3.13: Layout image of a particular area of a strip sensor where AC and DC pads are located, showing also zigzag-shaped p-stops to optimize the separation between p- and n-implants.

From a layout design point of view, the strip implant and metal should be wide, and the coupling oxide thin, to increase the coupling capacitance of the strip. The overlap of the metal respect to the implant can be enlarged, in order to draw the high electric fields from the electrodes to the coupling oxide. Additionally, a large metal overlap acts as an electron repellent field plate that prevents electron accumulation near the strip implants (Figure 3.12). Figure 3.13 shows a layout image of a particular area of a strip sensor, where a set of DC and AC pads are placed. Besides the width, separation and overlap rules, limitations for the shape and dimensions of the DC and AC pads can be also defined in the design rules, in order to meet the testing and assembling requirements. In particular, in Figure 3.13, the strip implant is widened below the pads in order to reduce the topology induced by the different layers. Consequently, the pads are designed staggered, with the p-stop in zigzag shape, with the aim to maximize the distance between p- and n-implants.

3.2.5 Biasing Structures: Bias Ring and Bias Resistor

In order to have the same potential in each individual strip, an n-implant ring, so-called *bias ring* is implemented surrounding and contacting all the strips, and delimiting the active area of the tracking sensor. Three different biasing structures are commonly used to contact the strip implants with the bias ring implant: *gate bias*, *punch-through bias* and *bias resistor*.

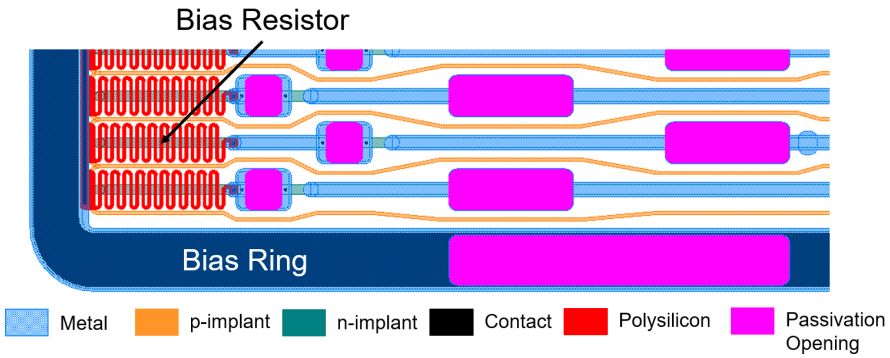


Fig. 3.14: Layout image of one of the strip sensor corners, showing several strips connected with polysilicon bias resistors to a bias ring surrounding all the strips.

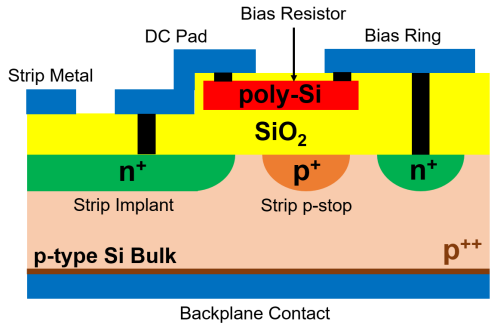


Fig. 3.15: Schematic cross-section, parallel to the strips, of the strip implant bias using a polysilicon bias resistor.

In the gate bias structure, a metal layer acts as a gate contacting the strip implant and the bias implant, similar to a MOS transistor. The metal gate should be activated with an external signal to create an electrical path between the implants, keeping the strips and the bias ring at the same potential. On the other hand, for the punch-through bias, the distance between the strip implant and the bias ring implant is reduced. When a voltage is applied to the bias ring, the depletion area below the n-implant ring grows and, when a certain threshold is exceeded, it reaches the small depletion area below the strip implant and both implants are put at the same potential. Finally, the third biasing structure is the bias resistor, which uses a polysilicon line to connect the strip implant and the bias ring implant (Figure 3.14). The polysilicon resistor is implemented over a thick oxide on top of the strip and the bias ring, contacting the strip implant through the DC pad and the bias ring through the metal on top of the bias ring implant (Figure 3.15). The total resistance of the polysilicon structure is usually established in a safety range, in the order of few MΩ, with the aim to ensure the strip biasing but also to limit the current in case of strip breakdown.

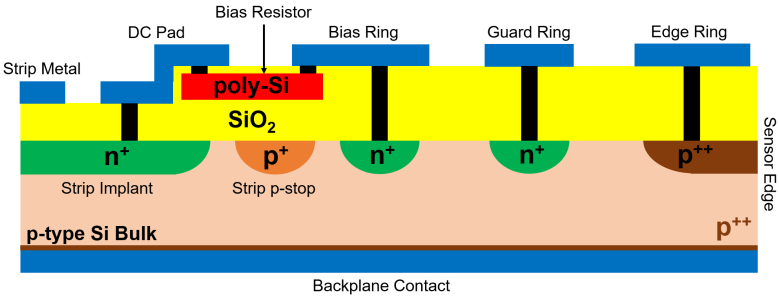


Fig. 3.16: Schematic cross-section, parallel to the strips, of the sensor edge termination.

The use of bias resistors requires a new mask level to implement the polysilicon resistor (polysilicon layer in Section 3.2.1), but the total bias resistance can be easily tuned adapting the length and width of the resistor and the sheet resistance of the deposited polysilicon layer. Besides its adaptability, the bias resistor is more radiation hard than the other biasing structures [55]. Therefore, the polysilicon resistor is widely used in strip sensor technology and is the biasing structure used for all the strip sensors presented in this thesis.

3.2.6 Sensor Termination: Guard Ring and Edge Structure

With the aim to improve the voltage performance of the strip sensor, two ring-shaped structures, concentric to the bias ring, are implemented conforming the sensor termination: the *guard ring* and the *edge structure*.

The first structure is the guard ring, placed next to the bias ring and composed of an n-type region connected to a metal layer on top (Figure 3.16). The doped region in the guard ring is used to shape the electric field originated in the bias ring, reducing the rapid decrease of potential in the lateral of the active area that can produce an electric field peak, inducing a low voltage breakdown. Two different connection schemes are usually employed with the guard ring structure, applying a certain potential, i.e. 0 V, or leaving the guard ring floating. Additionally, depending on the working bias needed and the proximity of the active area to the edge region, a multi-guard ring structure can be used, composed of several concentric rings, including in some cases alternated p-type regions, to enhance the control of the electric field. Figure 3.17 shows two examples of guard ring structures, one with a single ring and a second one with six rings with p-stops. The separation between implant rings and the width of the rings are the key parameters to be chosen, in terms of the substrate doping and voltage needs, in order to obtain an optimal termination structure.

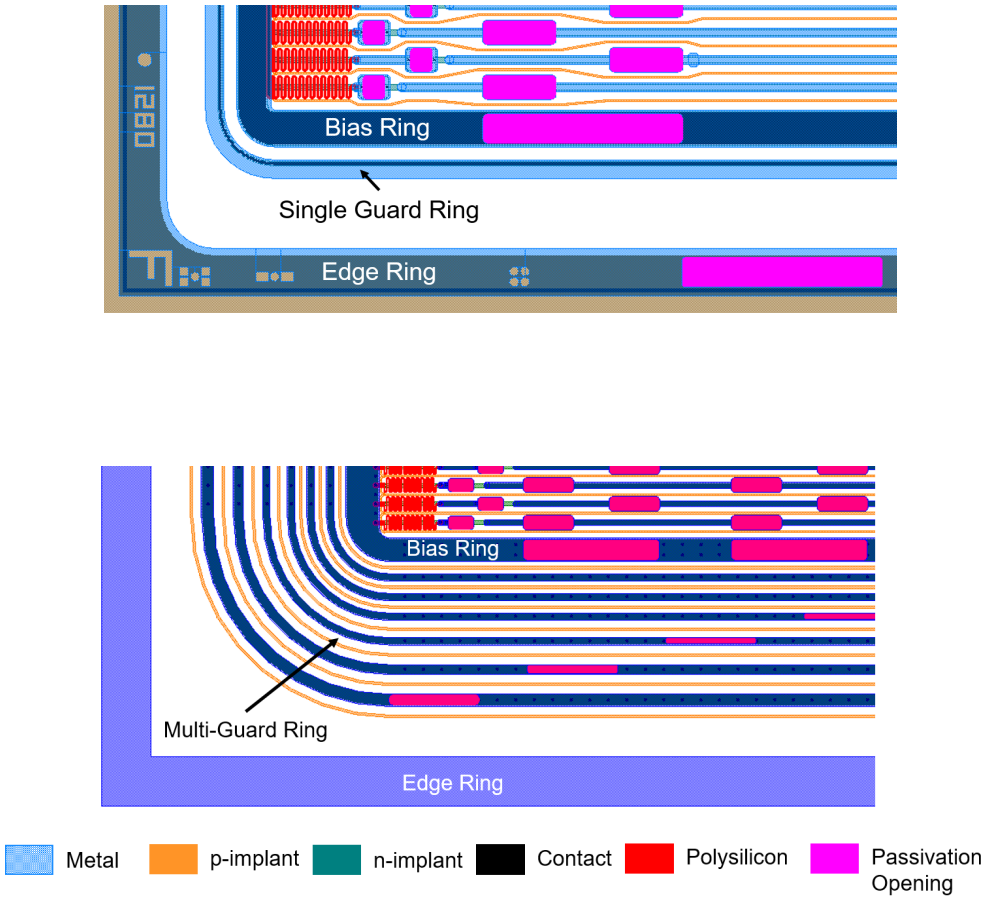


Fig. 3.17: Layout images of one of the strip sensor corners, showing two examples of sensor edge termination, with a single guard ring (top) and with a multi-guard ring (bottom).

The second, and outermost, structure used in current strip technologies is the edge structure. In this case, a p-type region is implemented at the periphery of the sensor, contacted to a metal layer on top (Figure 3.16). The doped region of the edge structure usually reaches the sensor dicing streets to ensure the presence of the p-type implant at the very edge of the sensor. Then, the possible appearance of an inversion region in the edge, able to short-circuit the n-implants with the sensor edge and backplane, is compensated by the introduction of p-impurities. In consequence, with this sensor termination, including the edge structure and the guard ring, the voltage drops from the physical edge of the sensor towards the active area enclosed by the bias ring.

The dimensions of the sensor termination are also a key aspect of the sensor design, since it introduces dead regions in the detector. Then, the number of guard rings and their separation with the edge structures should be minimized (*slim-edge*), without compromising the breakdown voltage, in order to optimize the inactive regions in the sensor.

3.2.7 Beam-loss Protection: Punch-through Protection

In a beam-loss accident, silicon strip sensors could generate a large amount of charge in the bulk, which can collapse the electric field, short-circuiting the sensor backplane and the strip implants. In AC-coupled strip technology, large voltage differences through the dielectric between the implant and the readout metal could produce irreversible damage to the coupling capacitor [43].

In order to prevent this situation, the new n-on-p strip sensors can be equipped with a *punch-through protection* (PTP) for each strip, where the distance between the strip implant and the bias ring implant is reduced at one end of the strips (Figure 3.18). Additionally, the PTP can be equipped with a *full gate* structure consisting of a polysilicon layer covering the PTP structure, which has shown to increase the effectiveness of the punch-through effect [56]. Then, when an intense particle beam hits the sensor, the PTP acts shorting the strip implant to the grounded bias ring when a certain voltage threshold is reached, evacuating the large amount of charge through the bias circuit and protecting the coupling capacitor [57].

3.2.8 Readout Connectivity

The connection of the readout chips with the strip sensor, usually made with wire-bonds, is another key aspect that should be carefully evaluated when a new sensor is designed. The rapid evolution of microelectronics allows the design of sensors with larger dimensions, e.g. using 6 or even 8-inch wafer substrates, while the density of the readout ASICs is increased, also increasing the number of channels. With

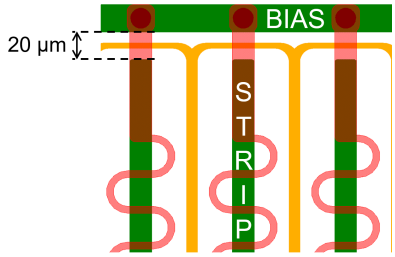


Fig. 3.18: Layout image of a strip sensor with punch-through protection. Figure adapted from [57].

the current tendency, the sensor-readout connection through wire-bonds can become challenging, especially when the pitch of the readout channels is considerably lower than the pitch of the strips, or even when the strips are not parallel and the pitch is variable. Consequently, the wire-bonding has to be done with a certain angle that in some cases can be high enough to compromise the process reliability. This issue was solved by the ATLAS collaboration for the sensors currently installed in the LHC, using *external pitch adaptors* consisting of metal tracks on a glass substrate, glued on top of the sensor, to adapt the strip pitch to the pitch of the readout electronics. However, as will be discussed in Section 4.4, the use of external pitch adaptors increases the cost and doubles the number of wire-bonds during the assembly process.

Readout connectivity issues in HEP experiments have been a hot topic in the last decades. In the 90s, double-sided detectors were developed by DELPHI[2] [58] and Collider Detector at Fermilab (CDF) [59] collaborations, facing the challenge of connecting both sensor sides to the readout electronics. In this case, the solution applied was the use of (second) metal tracks to route the (first) readout metals from one sensor side to make the readout connection through a unique access point ([60], [61]). A similar solution was implemented by the LHCb collaboration for sensors currently installed in the VErtex LOcator (VELO) system [62].

The use of second metal tracks, implemented (embedded) in the sensor itself, have also been considered by the ATLAS[63], CMS [64] and LHCb ([65], [66]) collaborations to adapt the pitch of the strips to the pitch of the readout channels, known as *Embedded Pitch Adaptor*, in the new strip sensors developed for the HL-LHC upgrade. For this purpose, a second metal should be included on top of the first (strip) metal, with a SiO_2 layer in-between and creating new *via* contacts to connect both metals (Figure 3.19). Thus, two new photolithographic mask levels should be included in the fabrication process, corresponding to the *via* and *second metal* layers in Section 3.2.1). However, besides the introduction of new photolithographic steps, it should be noted that an additional metal layer represents an additional parasitic capacitance, which can affect the inter-strip characteristics and the signal coupling. Possible adverse effects should

[2]One of the four main detectors of the Large Electron-Positron (LEP) collider at CERN.

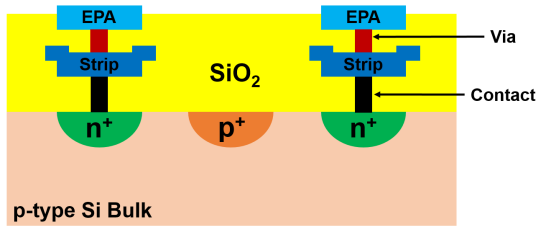


Fig. 3.19: Schematic cross-section of a n-on-p strip detector with an EPA implemented.

be carefully evaluated when designing the EPA structure used, in order to minimize their impact in the sensor performance and module assembly[3].

3.2.9 Other Elements: Fiducials, Labels and Scratch Pads

In general terms, the layout of a sensor includes a set of elements that are dedicated to facilitate the device identification and assembly, without influence on the device performance. These elements are usually included in a layer that can be easily observed with a microscope, e.g. metal layer, and are placed outside of the sensitive area. As these elements are part of the layout, they should fulfil the design rules, that usually include additional structures useful during the fabrication and assembly processes.

As an example, the strip sensors for the ATLAS upgrade are planned to include a wide variety of these elements to be implemented in the metal layer [67]. The new sensors will include seven different fiducial marks (Figure 3.20), six open-in-metal and one metal-in-open, to facilitate the sensor assembly process. Some of these fiducial marks indicate the location of certain parts of the sensor, such as *Mark I* that indicates the end of the strips, and others help to identify the orientation of the sensor, such as *Mark F* that is asymmetric in x and y coordinates. The strips are also numbered including a label to facilitate its identification, this being especially useful for sensors with several hundreds of strips. Examples of use of *Marks F*, *G*, *I* and strip labels can be seen in Figure 3.17(top). Moreover, in massive productions, such as the planned for the HL-LHC detectors upgrade, each device includes a sensor label and a set of scratch pads, to assign a unique binary code to each sensor after fabrication, with the objective to facilitate the identification of the sensor type, wafer number and fabrication batch (Figure 3.21).

[3] Several EPA designs will be discussed and evaluated in detail in Section 4.4.

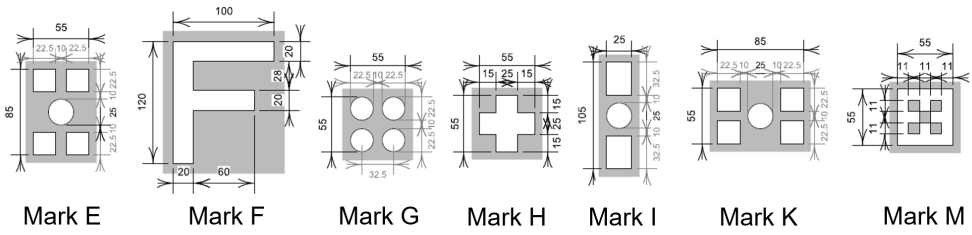


Fig. 3.20: Fiducial marks used for the ATLAS ITk strip sensors. Figure from [67].

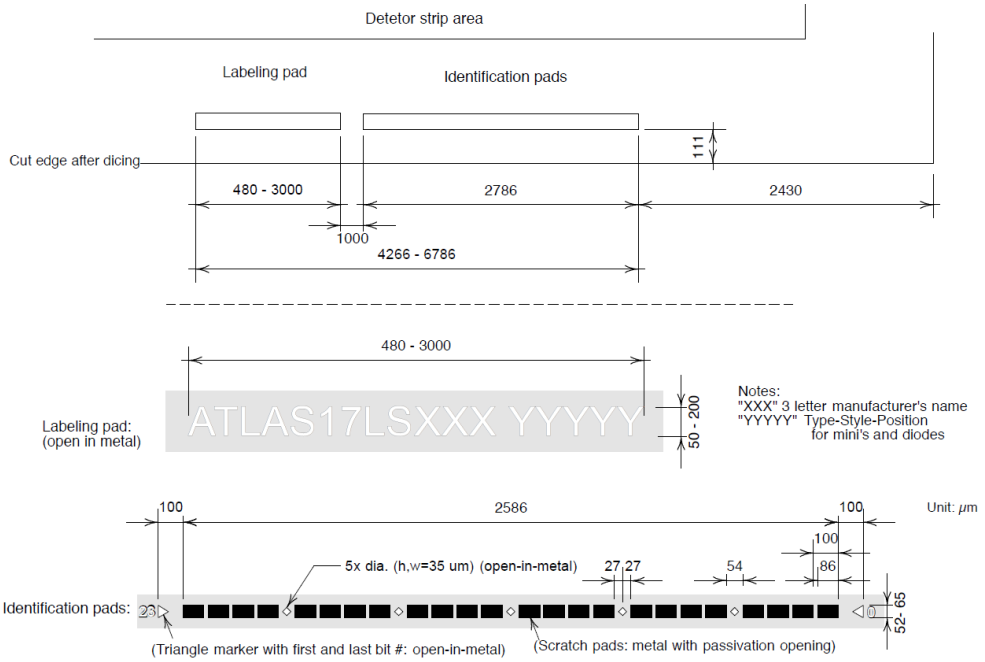


Fig. 3.21: Example of labels and scratch pads used for the ATLAS17LS prototype. Figure from [68].

4

Design of Silicon Strip Detectors for the ATLAS Inner-Tracker Upgrade

This chapter presents the contributions made during this PhD thesis on the layout design of prototypes, test structures and new solutions for the upgrade of the ATLAS Inner-Tracker (ITk) strip detector system. In this framework, a novel layout design tool based on python scripting, developed to facilitate the automatic generation of prototypes, is shown in the first Section 4.1. This new tool was applied for the first time during the ATLAS strip sensor Market Survey to design a full-size Barrel prototype, and a set of miniature sensors and diodes, for the candidature of Infineon Technologies AG to produce the new sensors. Section 4.2 details the layout design process, and demonstrates the usefulness of the python-based layout tool with a practical case. Section 4.3 introduces the importance of the use of microelectronic test structures in the technological development of new strip sensors and additionally applies the concepts in the design of Quality Assurance test chips, that will be used to monitor the ITk strip sensor production in the next 5 years. Moreover, a solution to improve the interconnection between the new radially-oriented strip sensors (End-cap) and the readout electronics is presented in Section 4.4, consisting of integrated (embedded) metal strip pitch adapters. The section shows a wide set of layout designs with the aim to optimize the electro-mechanical implications in the final devices. Finally, Section 4.5 faces, for the first time, the challenge to set-up the Centro Nacional de Microelectrónica (IMB-CNM) cleanroom to fabricate large area strip sensors in 6-inch wafers, studying some of the critical microfabrication steps and laying the foundations to design the first large area prototype adapted to the IMB-CNM design rules, making use of the programmable layout tool introduced at the beginning of the chapter.

Figure 4.1 shows the colour code used for the different layers of the layout images presented in this chapter.

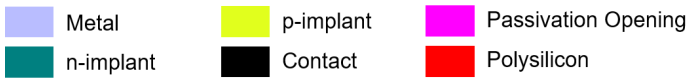


Fig. 4.1: Colour code used for the different layers of the layout images.

4.1 Automatic Layout Generation Tool

A new python-based layout design tool was developed during this PhD thesis to address the need for prototypes of strip tracking sensors for future HEP experiments. This versatile tool, called *Automatic Layout Generation Tool* (ALGT) ([69], [70]), can be used to easily layout sensors adapted to different wafer sizes (e.g. 4, 6, 8-inch or even larger wafer formats), characteristics, or technologies, introducing variations in their layers or even generating test structures, such as miniaturized sensors or monitor diodes.

The software used for the layout design is Glade [71], a freeware integrated circuit (IC) editor extendible using python scripting, developed by Peardrop Design Systems. By compiling a python script in Glade, a parameterised *programmable-Cell* (PCell) is generated, called *SuperMaster* cell. This primary cell is used to create instances, called *SubMaster* cells, using the unique properties defined for the instance. PCells can have multiple input parameters (or arguments), and must have default values specified for each one in order to build the SuperMaster cell.

PCells already created are instantiated by other PCells, generating more complex layout structures, arranged in different hierarchy levels. Figure 4.2 shows the PCell hierarchy created for the ALGT, with the aim to generate a wide variety of strip sensor prototypes. Each box represents a single PCell, showing the python script name and the input parameters that can be modified through its instantiation. PCells from the lower level create basic elements of the sensor layout, e.g. AC or DC pads, and cells located at the higher levels instantiate one or multiple PCells from the lower levels to compose more complex structures, e.g. bias resistors or strips. Besides the input parameters, each ALGT PCell is programmed by defining internally two types of variables, not accessible through their instantiation:

Device Variables: Parameters associated with the common configuration of the final devices, e.g. implant width or strip pitch. These parameters should remain constant within the same prototype project, in order to ensure the expected performance of the fabricated sensors. In particular, device variables are defined by the High Energy Physics (HEP) experiment collaboration, e.g. ATLAS or CMS.

Technological Variables: Parameters established by the manufacturer, associated to their fabrication process, e.g. minimum size of layers or overlaps between them. In particular, the values for the technological variables are defined in the *technological design rules*[1] of the foundry in charge of the fabrication, e.g. Hamamatsu or Infineon.

[1] General design rules concepts previously explained in Section 3.1.4.

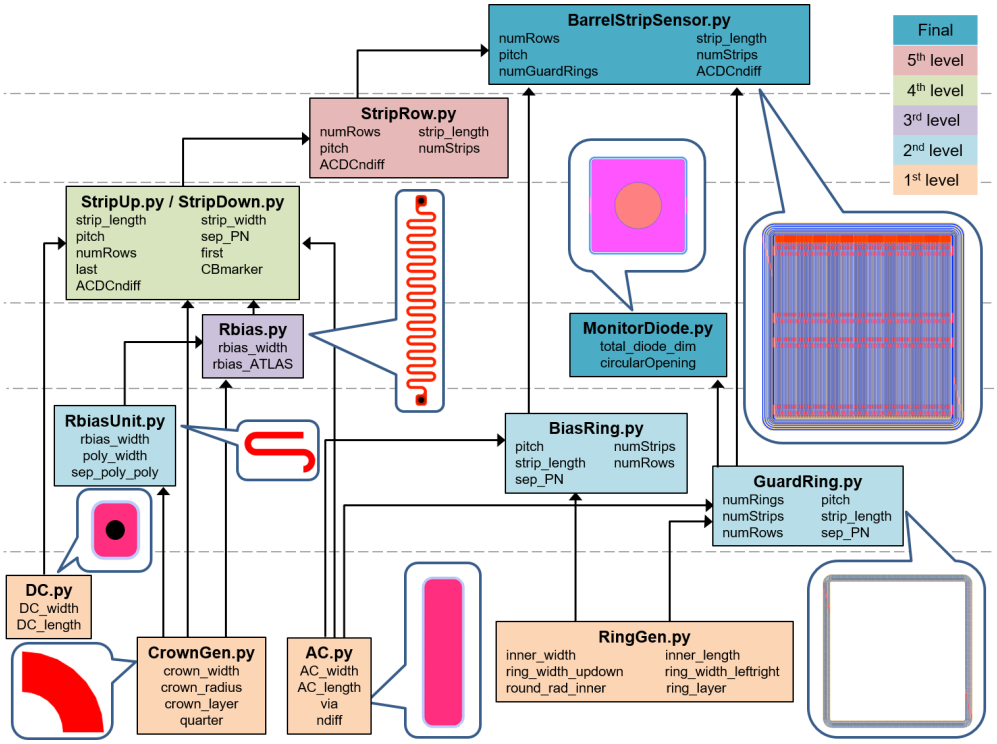


Fig. 4.2: PCell hierarchy to design prototype strip sensors using the Automatic Layout Generation Tool. PCells represented by boxes, indicating the python script name and the input parameters.

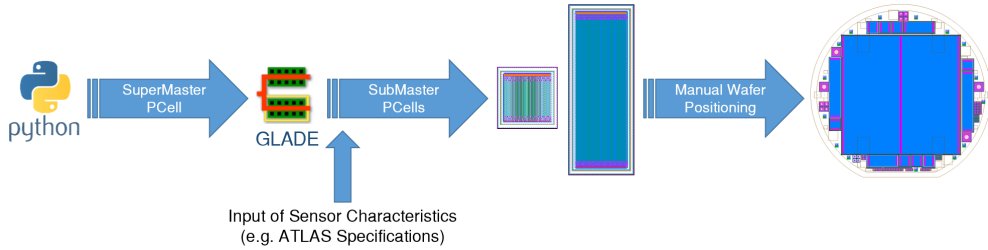


Fig. 4.3: Wafer layout design workflow using the Automatic Layout Generation Tool.

Hence, when designing a programmable strip sensor, devices with different dimensions and features can be easily generated adapting the values of the corresponding PCell variables, e.g. p- and n-implant width, strip length, pitch, number of strips and strip rows, polysilicon resistor geometry, etc. Figure 4.3 shows a schematic representation of the general layout design workflow using the ALGT technique.

4.2 Layout Design of Infineon Prototype for the ATLAS Strip Sensor Market Survey

In 2016, the ATLAS collaboration entered the Market Survey [72] phase in the search of foundries to fabricate the ITk strip sensors for the High-Luminosity Large Hadron Collider (HL-LHC) upgrade. Two vendor candidates, Infineon Technologies A.G. (IFX) [73] and Hamamatsu Photonics K.K. (HPK) [74], were pre-selected in the step-1 of the survey. For the step-2, ATLAS requested the different companies to supply fully functional sensors previously fabricated, representative of the quality the companies were able to achieve. The sensor samples were tested in different ATLAS institutes, before and after irradiation, fulfilling most of the requirements established by ATLAS, fulfilling most of the requirements established by the ATLAS sensor community, therefore both companies passed the step-2 evaluation. For the final qualification phase of the Market Survey, the step-3, the vendors were requested to provide full-size and fully featured prototype sensors according to the specifications[2] [72] stated by ATLAS.

For this final step of the survey, the ATLAS collaboration was in charge of the full wafer layout design for Infineon, the so-called ATLAS17LS-IFX, containing a full-sized Barrel Long-Strip sensor and a wide variety of miniature sensors, diodes and test structures. This work involved a complex challenge and a fruitful collaboration between ATLAS, IMB-CNM and Infineon, reconciling the ATLAS requirements and the technological and design rules of the vendor. For the design of the devices included in the ATLAS17LS-IFX wafer layout, the ALGT described above was used for the first time, proving

[2] ATLAS ITk specifications detailed in Section 5.1.

Sensor Mechanical Properties	
Silicon wafer diameter	6 inches (150 mm)
Thickness (uniformity)	300 μm (20 μm)
Length	97637 μm (slim-edge) / 98937 μm (standard-edge)
Width	97966.5 μm (slim-edge) / 99066.5 μm (standard-edge)
Sensor Electrical Properties	
Wafer type	p-type FZ
Crystal orientation	<100>
Resistivity	> 3 $k\Omega$cm
Full depletion voltage (V_{fd})	< 330 V
Maximum operating voltage	700 V

Tab. 4.1: Electro-mechanical properties of the n^+-on-p Barrel Long-Strip prototype sensor ATLAS17LS-IFX for the HL-LHC upgrade.

the usefulness of the tool to generate prototypes adapted to the design rules of the manufacturer and at the same time fulfilling the client requirements.

4.2.1 Main Sensor

The maximum fluence expected in the inner layers of the ATLAS ITk strip system in the HL-LHC will be 1.6x10^{15} 1-MeV neutron equivalent (n_{eq})/cm^2, and a total ionizing dose (TID) of 66 Mrad(Si), for its ten years of lifetime, including a 1.5 safety factor ([10], [18]). In order to increase the radiation hardness relative to the p^+-on-n strip sensors currently installed in the ATLAS SCT, the more robust n^+-on-p technology [75] was proposed for the ITk. However, n^+-on-p technologies have different design requirements than p^+-on-n, and they include characteristic structures such as p-stops [76]. Additionally, and in contrast to the current LHC sensors fabricated on 4-inch wafers, the new ATLAS strip sensors are designed to maximize the use of 6-inch substrates currently used by the leading radiation sensor foundries. The new devices, designed with larger dimensions, reduce the number of wafers needed to cover a particular tracking area and therefore the cost of the final system and the hermeticity, but this requires the development and validation of the new large area strip sensor technologies. Table 4.1 summarizes the electro-mechanical properties of the ATLAS strip sensors for the HL-LHC upgrade [67].

The new strip Barrel system will be composed of Long-Strip (LS) and Short-Strip (SS) sensors. In the frame of the participation of Infineon in the Market Survey, a prototype LS sensor (hereinafter referred as *Main sensor*) was designed using the ALGT software presented above. The input parameters used in the ALGT were extracted from the ATLAS17LS technical specifications document [67] defined by the ATLAS Collaboration. Table 4.2 presents some of the Main sensor layout requirements, and the corresponding input parameters used to generate the device with the ALGT. Figure 4.4 shows an

	ALGT Input Parameters	ATLAS17LS-IFX Design Requirements
Number of strip segments	`numRows`	2
Number of strips per segment	`numStrips`	1280+2
Strip pitch	`pitch`	75.5 μm
Strip length	`strip_length`	48289.5 μm
Strip width	`strip_width`	16 μm
Polysilicon bias resistance	`rbias_ATLAS`	1.5 ± 0.5 $M\Omega$

Tab. 4.2: Design specifications for the ATLAS17LS-IFX Main sensor, indicating also the associated ALGT input parameters.

image of the ATLAS17LS-IFX Main sensor layout generated with the ALGT with some of the design characteristics of the prototype.

Punch-Through Protection (PTP): The sensor implements a Punch-Through Protection (PTP) structure for each strip, with an optimum separation [20] of 20 μm between the n-implant of the strip and the n-implant of the bias rail. As explained in Section 3.2.7, the PTP acts shorting the strip implant to the grounded bias rail when a certain voltage threshold is reached, protecting the coupling capacitor [57]. In addition, the PTP structure is equipped with a *full-gate* structure consisting of a polysilicon layer covering the PTP structure, which has shown to increase the effectiveness of the punch-through effect [56].

Staggered Pads: The strip implant below the AC and DC pads is widened to have similar dimensions to the pads. This increase in the strip implant is included with aim to avoid the topology induced by the different layers in the metal of the pad, which could lead to needle contact problems during measurements and worse bondability. In consequence, the DC pads of neighbour strips are designed staggered to allow a zigzag p-stop trace that maintains constant the separation between p- and n-implants.

Standard vs. Slim-edge: Besides the new 6-inch large area design of the HL-LHC sensors, the reduction of the sensor edge to achieve minimum inactive regions in the tracking system is another big improvement for the new devices. With the aim to test the performance of the detector with different bias-to-edge distances, the Main sensor is equipped with two different sets of dicing lines: the *slim-edge* and the *standard-edge*. The slim-edge configuration has a distance of 458 and 558 μm, longitudinal and lateral to the strips, respectively, measured as the distance from the inner edge of the n-implant of the bias ring to the silicon physical edge. On the other hand, the standard-edge has a distance of 1108 μm in both directions, similar to the edge configuration of the strip sensors currently installed in the ATLAS Semiconductor Tracker (SCT) [14].

Other features, such as a passivation opening along the upper and lower bias rail, to facilitate the sensor testing, new chip boundary (CB) markers in the first strip

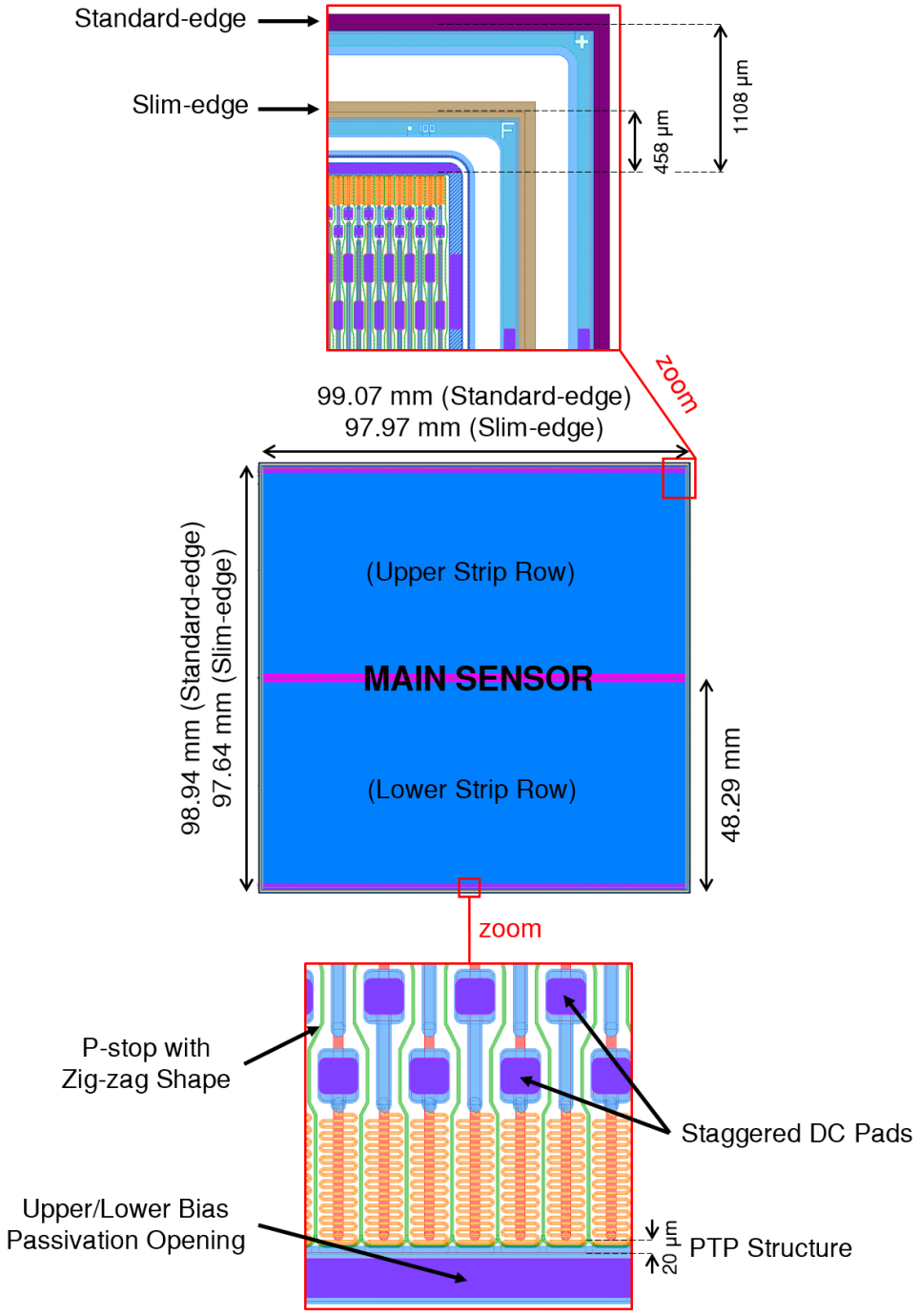


Fig. 4.4: ATLAS17 Barrel Long-Strip prototype Main sensor, designed for the participation of Infineon as a vendor for the Market Survey.

	Device	Quantity
Sensors	Main Sensor	1
	Miniature Sensor (Mini)	6
	Miniature Short-Strip Sensor (MiniSS)	1
	Miniature Long-Strip Sensor (MiniLS)	1
Test Sensors	Miniature Test Sensor (Mini_test)	2
	Miniature Short-Strip Test Sensor (MiniSS_test)	1
	Miniature Long-Strip Test Sensor (MiniLS_test)	1
Diodes	Monitor Diode 8 x 8 mm^2 (MD8)	4
	Monitor Diode 4 x 4 mm^2 (MD4)	12
	Monitor Diode 2 x 2 mm^2 (MD2)	39
	Monitor Diode 1 x 1 mm^2 (MD1)	74
	Test Diode 1 x 1 mm^2 Active Area (TD3)	6
Additional Structures	TestStrip	13
	TestSurf	13
	TestEdge with Guard Ring	1
	TestEdge without Guard Ring	1
	Infineon fabrication test structures	-

Tab. 4.3: ATLAS17LS-IFX full wafer layout inventory.

metal of every 128 strips, to avoid issues during the wire-bonding, or the inclusion of new fiducial marks, to help the sensor positioning in the module assembly, were also included in the ATLAS17LS-IFX prototype layout.

4.2.2 Full Wafer

Besides the Main sensor layout design, several test structures were generated using the ALGT, with the aim to assess the pre- and post-irradiation performance. The different test structures designed for the ATLAS17LS-IFX prototype will be described in the next Section 4.3. Additionally, a set of fabrication test structures, provided by Infineon, were also located in the wafer following the manufacturer design rules. Table 4.3 shows the complete list of devices included in the full wafer layout.

Figure 4.5 presents the full wafer layout for the ATLAS17LS-IFX prototype, including the different test structures positioned around the Main sensor, that is located in the center of the wafer. Most of the test structures share one dicing line with the Main sensor to take advantage of the principal cuts. Each dicing street includes a passivation opening to facilitate the dicing process.

The full wafer layout was designed following the ATLAS specifications and the Infineon design rules. The design was evaluated and approved by the collaboration, before the start of the fabrication of the ATLAS17LS-IFX prototype for the Market Survey.

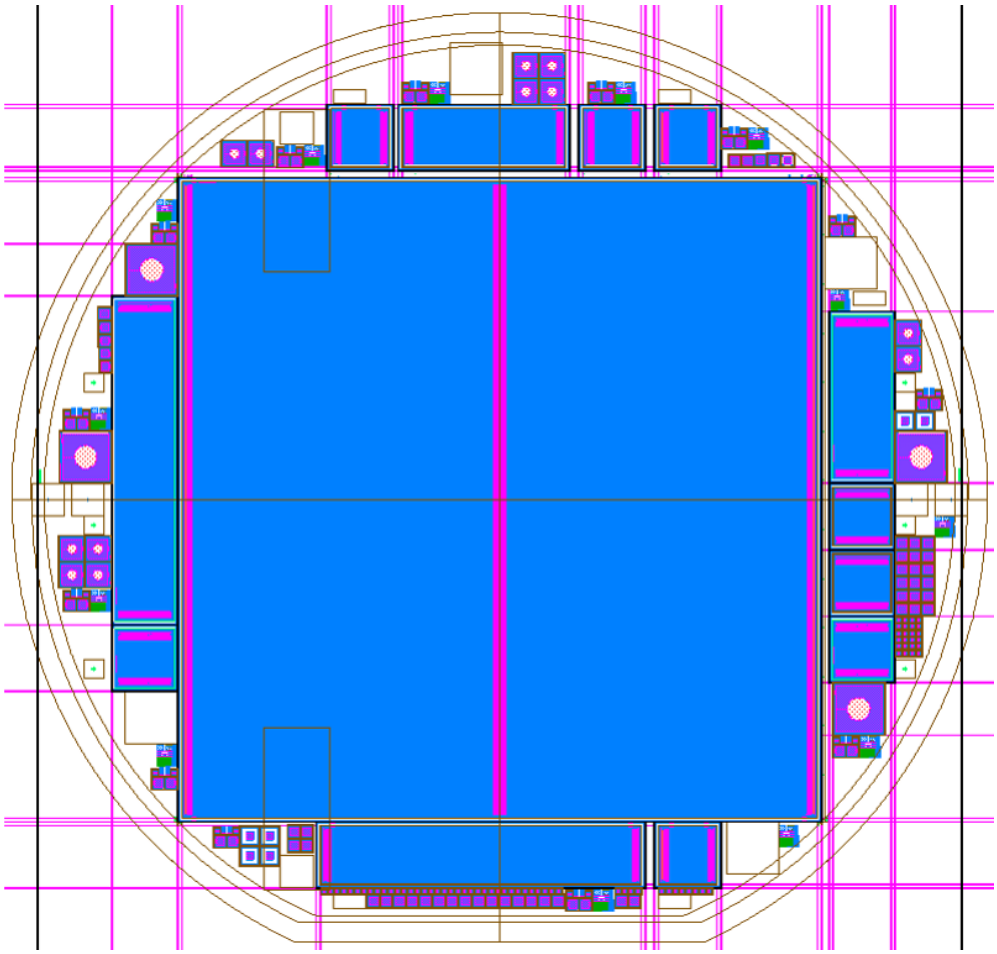


Fig. 4.5: ATLAS17LS wafer layout design for the participation of Infineon in the sensor production Market Survey.

4.3 Microelectronic Test Structures

The development of new large area strip sensors requires a complete validation of the devices under the expected radiation levels. This section presents a set of microelectronic test structures, designed at IMB-CNM during this PhD thesis, with the objective to validate the Infineon strip technology in the frame of the sensor Market Survey [77]. In addition, this section details the layout design of the different test chips included in the final ATLAS ITk strip Barrel and End-cap wafer designs to be used during production for Quality Assurance tests (Section 4.3.2).

4.3.1 Test Structures for Technology Development

The use of test structures is essential in the development of microelectronic technologies, allowing the direct measurement of key device parameters [78]. These structures can be replicated and distributed across the silicon substrate in order to study the homogeneity and spatial distribution of the different parameters. Additionally, the development of the new large area strip sensors, for the main CERN experiments, requires a complete validation of the devices under the increased radiation levels.

In the framework of the ATLAS ITk strip sensor Market Survey [10], as previously explained, a complete prototype wafer layout was designed by the ITk collaboration and fabricated by Infineon. Besides a large area prototype Barrel Long-Strip sensor (Main sensor), the wafer layout includes several miniature sensors (miniature sensors) and diodes, maintaining the bias/guard ring and edge configuration of the Main sensor, and a set of test structures.

Table 4.4 summarizes the most relevant parameters for the development of a strip sensor technology, going from global (or device-related) parameters, e.g. full depletion voltage or breakdown voltage, to more technological parameters, e.g. doping concentrations or surface currents, indicating also the test structures that can be used for their study.

Global Parameters

To test the global performance of a strip sensor, the basic parameters to evaluate are the leakage current, the full depletion voltage and the breakdown voltage. These parameters can be evaluated from commonly used test structures, such as miniature sensors. However, it is recommended the use of diodes for an accurate study of the full depletion voltage, in order to avoid the presence of parasitic resistances that require additional voltage to fully deplete the device.

	Key Parameters	Test Structure
Global Parameters	Reverse Leakage Current (I_r)	Mini sensors / Monitor Diodes
	Full Depletion Voltage (V_{fd})	Monitor Diodes
	Breakdown Voltage (V_{bd})	Mini sensors / Monitor Diodes
Inter-strip Parameters	Inter-strip Resistance (R_{int})	Mini sensors
	Inter-strip Capacitance (C_{int})	Mini sensors
Strip Parameters	Strip Metal Resistance (R_{metal})	Strip Metal Resistor (TestStrip)
	Strip Implant Resistance ($R_{implant}$)	Strip Implant Resistor (TestStrip)
	Bias Resistance (R_{bias})	Bias Resistor (TestStrip)
	Coupling Capacitance (C_{coupl})	Coupling Capacitor (TestStrip)
Technological Parameters	Flat Band Voltage (V_{fb})	MOS Capacitor (TestStrip) / Gated Diodes (TestSurf)
	Field Oxide Capacitance (C_{ox})	MOS Capacitor (TestStrip)
	Equivalent Oxide Thickness (t_{ox})	MOS Capacitor (TestStrip)
	Surface Generation Current (I_{gen},s)	Gated Diodes (TestSurf)
	Effective Doping Concentration (N_{eff})	Monitor Diodes

Tab. 4.4: Some of the key parameters to develop a strip sensor technology, and test structures associated with each one in the ATLAS17LS-IFX prototype.

For the ATLAS17LS-IFX Market Survey prototype, three miniaturized Barrel sensors (Figure 4.6) with different dimensions were designed: a 10x10 mm^2 (Mini), a 26x10 mm^2 (MiniSS) and a 50x10 mm^2 (MiniLS), the latter ones with the actual strip length of Short-Strip and Long-Strip Barrel sensors. These test devices maintain the Main sensor bias/guard ring configurations, also including the standard-edge and slim-edge dicing options.

On the other hand, a set of square monitor diodes (MD) (Figure 4.7) were designed, with slim-edge configuration but variable dimensions: 8x8 mm^2 (MD8), 4x4 mm^2 (MD4), 2x2 mm^2 (MD2) and 1x1 mm^2 (MD1). MD8 and MD4 diodes include a circular metal opening at the center of the active area that acts as a window to allow measurements with a laser source, and passivation openings for contacts at the guard ring and edge structures.

Additionally, the sensor edge geometry plays an important role on the global sensor performance. A special test structure, called *TestEdge* (Figure 4.8), was designed specifically to study the influence of the sensor edge configuration on the device breakdown voltage and leakage current. This structure is composed of five 2x2 mm^2 square diodes, with identical active area and one of the dicing lines aligned for all of them. The central diode has an edge configuration identical to the Main sensor, and the rest of the diodes have variable distances between active area and silicon physical edge, in steps of 30 μm, resulting in edge distances going from 315 to 435 μm (see cross-section in Figure 4.8). Two different sets of TestEdge structures were designed, one with and one without guard ring.

Strip Parameters

In strip sensor technologies, the proper performance of the individual strips is essential to achieve an accurate tracking detection. As it was shown in Chapter 3.2, a n-implant

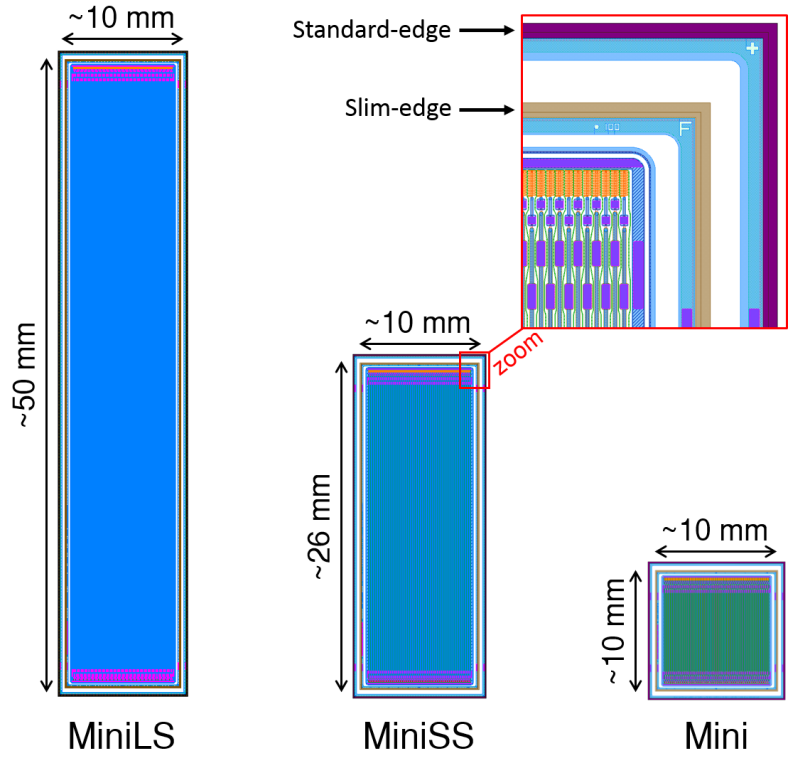


Fig. 4.6: Miniature sensors, including standard-edge and slim-edge dicing options.

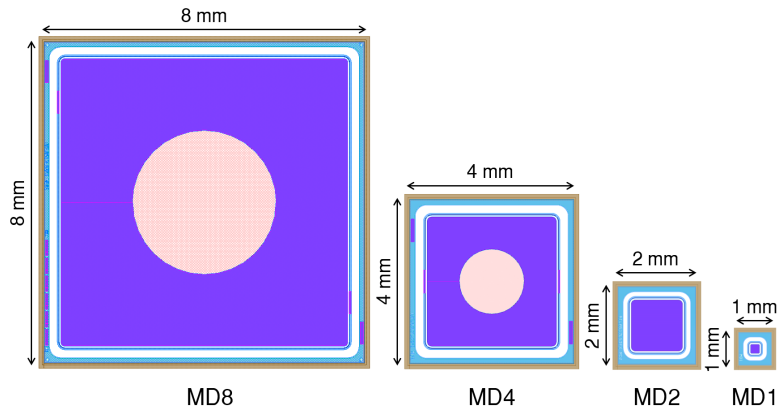


Fig. 4.7: Monitor diodes, including guard and edge ring testing pads and circular metal opening for laser measurements in MD8 and MD4 designs.

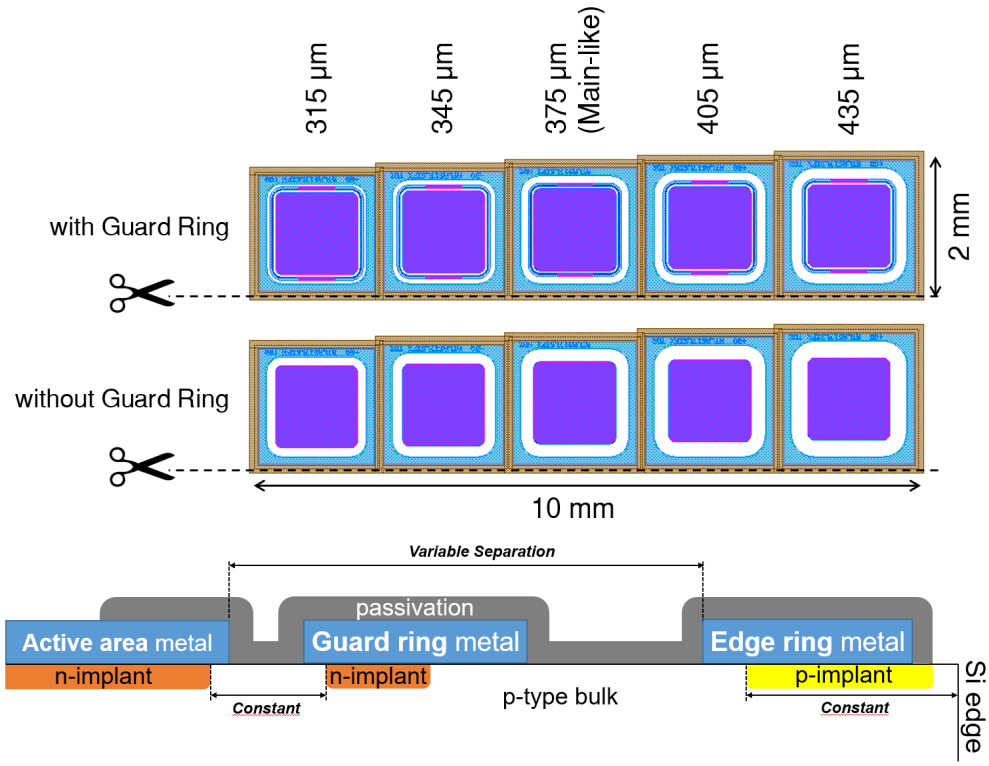


Fig. 4.8: TestEdge structure designed to study the influence of the sensor physical edge, respect to the active area. Five 2x2 mm^2 diodes with variations on the edge distance. Two different test structure sets designed, with (top) and without (center) guard ring. Cross-section of the TestEdge structure with guard ring also shown to provide details of the sensor edge configuration and variable separation (down).

collects the charge generated by a particle crossing the sensor. The readout is AC-coupled to a metal layer over the strip implant and each strip is biased via a polysilicon resistor. The strips are isolated by a p-implant equidistant between strips, called p-stop.

Figure 4.9 presents a set of test structures, called *TestStrip*, designed to study the most relevant strip parameters. The TestStrip includes three sets of sixteen pads in line with a pitch of 200 μm, enabling automatic tests using a probe-card and a switching matrix in an automatic probe station. In one of the sets, all pads are short-circuited with a metal layer, in order to check if the initial probe-card coordinates (x, y and z) provide good contact between the needles and the testing pads, ensuring the electrical contact for the rest of automatic measurements.

A polysilicon resistor, identical to the ones implemented in the Main sensor, is incorporated in this test structure to measure the bias resistance. A metal resistor, with length and width corresponding to the metal deposited over the Main sensor strips, is included in the TestStrip to check the resistance of the strip metal. A similar structure is also included using an n-implant layer, with p-stop isolation, to measure the resistance of the strip implant. All these resistance test structures are equipped with two pads per terminal in order to separate the current and voltage electrodes, eliminating the contact resistance and improving the accuracy of the measurement through the use of the Kelvin contact technique [79]. Finally, a square coupling capacitor, with an area similar to the Main sensor strips, is also included to measure the characteristics of the coupling oxide between the n-implant and the metal layer.

Inter-strip Parameters

The Main sensor consists of ten groups of 128 AC-coupled strips, reaching a number of 1280 strips per row in the new ATLAS Barrel strip sensors for HL-LHC, and even higher in some of the End-cap designs. The strips have a pitch of 75.5 μm in Barrel sensors and a variable pitch for the ones in the End-cap region. They include p-stop isolation.

In order to test the isolation of the strips, measurements of inter-strip resistance and capacitance are essential. The test of inter-strip parameters could be done in any of the miniature sensors (Figure 4.6), as we can assume that the inter-strip parameters, except in the region close to the strip ends, scale with strip length. Other dedicated structures, such as the interdigitated that will be presented in Section 4.3.2, can also be used to measure the inter-strip parameters. The possibility to use miniature sensors or interdigitated structures for the study of the inter-strip parameters of a Main sensor is specially useful, due to the high number of devices per wafer and their reduced dimensions, ideal for extensive irradiation campaigns.

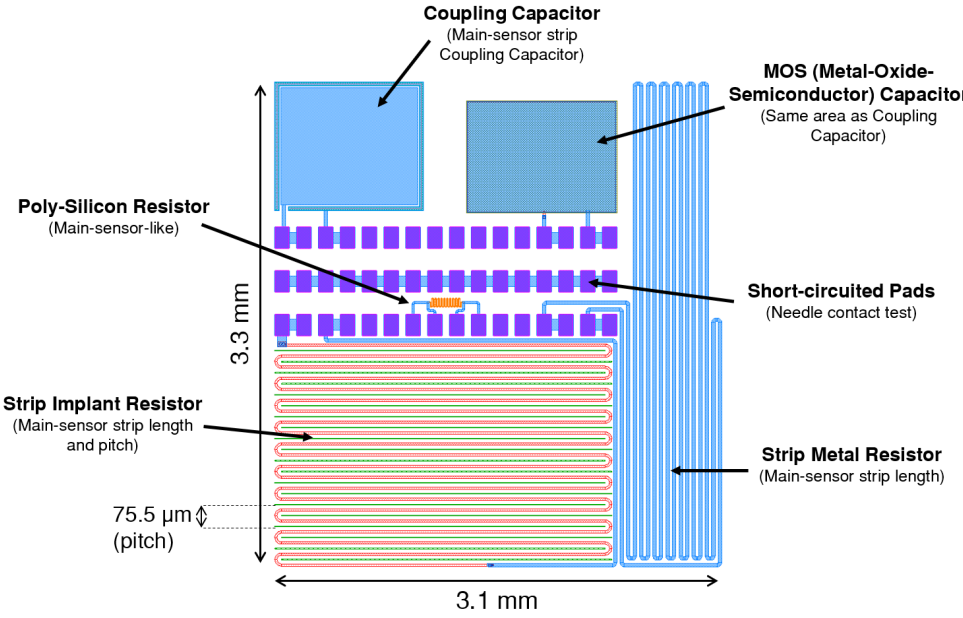


Fig. 4.9: TestStrip structure designed to study single strip parameters in the ATLAS17LS-IFX wafers.

Technological Parameters

Several parameters intrinsic to the strip technology can be studied to evaluate in detail the performance of the Main sensor. The effective doping concentration of the silicon substrate can be calculated from the full depletion voltage extracted from bulk capacitance measurements [54] of miniature sensors or monitor diodes. The TestStrip (Figure 4.9) also includes a square Metal-Oxide-Semiconductor (MOS) capacitor, with the same oxide thickness as the inter-strip oxide under the passivation (hereinafter referred as *field oxide*), from where we can evaluate parameters such as the flat band voltage, the capacitance or the thickness of the field oxide [79]. The investigation of the field oxide and its Si/SiO_2 interface quality, before and especially after irradiation, is also essential to ensure the correct performance of the strip sensors at the adverse working conditions expected in the future HEP experiments.

Figure 4.10 shows a test structure called *TestSurf* containing several *gated diodes*, designed and included in the layout for the Infineon prototype fabrication, with the aim to study the influence of radiation on the surface generation current ([80], [81]), and to complement the results extracted from the MOS capacitor. This structure contains a set of four diodes, each one with a square active area and a ring acting as a gate. In order to study the influence of the gated diode design in the surface characterization, two different perimeter-to-area ratios (1x1 mm^2 and 2x2 mm^2) and two different gate materials (metal and polysilicon) are implemented.

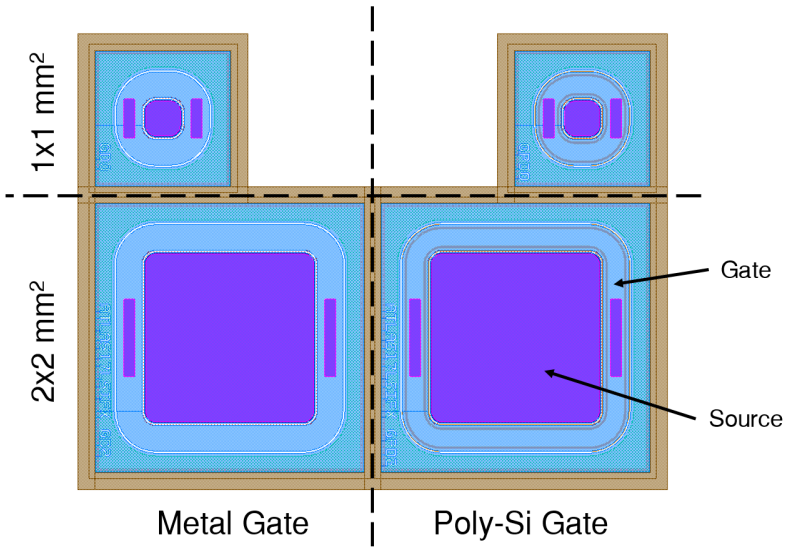


Fig. 4.10: TestSurf structure containing four gated diodes, with variations in perimeter-to-area ratio (1x1 mm^2 and 2x2 mm^2) and gate layers (metal and polysilicon).

4.3.2 Test Structures for Production Quality Assurance

For the ATLAS ITk strip sensor production, the collaboration has the responsibility to monitor the characteristics of the fabricated devices, comparing and complementing the in-site tests performed by the manufacturer. Since the fabrication will be produced in technological batches, and can be assumed that variations within batches are smaller than variations across batches, a representative percentage of the sensors and test structures per batch will be tested by the collaboration. The Quality Assurance (QA) programme [82] is focused on monitoring the fabrication process to detect eventual deviations and predict negative tendencies of key parameters during production (Figure 4.11) through the systematic study of test structures [83], whereas the Quality Control (QC) programme [84] checks the fulfilment of the ATLAS specifications performing tests directly on the Main sensors. For both testing programmes, dedicated QA and QC specification documents are being drafted to establish the testing methods and acceptance criteria.

In the frame of the QA programme for ATLAS ITk strip sensor production, a test chip (Figure 4.13) was designed at IMB-CNM during this PhD thesis with the objective to cover all the QA tests planned for the 5 years of production. This test chip includes several of the test structures described in the previous section and some new structures more specific for the production QA programme. The test chip design was evaluated by the ATLAS sensor community and approved to be included in the periphery of the eight different ATLAS18 production wafer layouts, two Barrel and six End-cap (Figure 4.12). Each of the wafers includes several instances of the test chip in different positions to

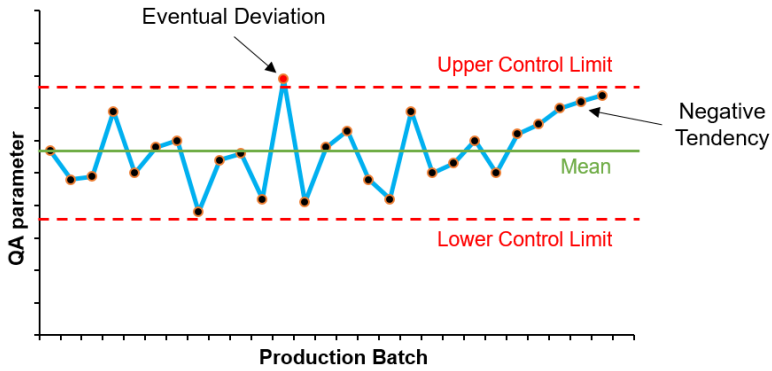


Fig. 4.11: Example of the evolution of a QA parameter during production, showing possible eventual deviations or negative tendencies.

allow the study of the homogeneity of the different parameters across the wafer, if necessary.

The reduced size of the test chip (10x12 mm^2) is specially useful for the routine irradiations planned for the production QA, facilitating the monitoring of the Main sensor radiation hardness using a test chip ten times smaller. Most of the structures included in the QA test chip are connected to a set of twelve pads in line, with a pitch of 200 μm in a grid of 50 μm within the test chip, enabling automatic tests using a probe-card and a switching matrix in an automatic probe station. Similarly to the TestStrip presented in the previous section (see Figure 4.9), the QA test chip includes one set of pads short-circuited with a metal layer, in order to provide a method to test the needle contact prior to the automatic measurements. Additionally, the most relevant test structures are routed with metal tracks to the edges of the test chip, facilitating the wire-bonding of the structures and their characterization with the chip assembled on a PCB board (Figure 4.15).

Figure 4.13 shows the layout of the ATLAS QA test chip for the Barrel wafer designs (SS and LS), indicating the position of the test structures, the test pads for capacitance open correction (OC) and needle contact test (CT), and the dimensions of the test chip. The QA test chip designs are identical for all the Barrel and End-cap wafers, except for the interdigitated structures (Figure 4.14) that are adapted to the strip length and pitch of the corresponding Main sensor. Below the characteristics of the different structures are described and the key device parameters that can be studied with them for the QA programme.

5-strips Structure: This structure is composed by five parallel strips with a pitch identical to the Barrel designs (75.5 μm), with an implant width identical to the Main sensors (16 μm) and including p-stop and AC/DC pads (Figure 4.13(a)). The structure

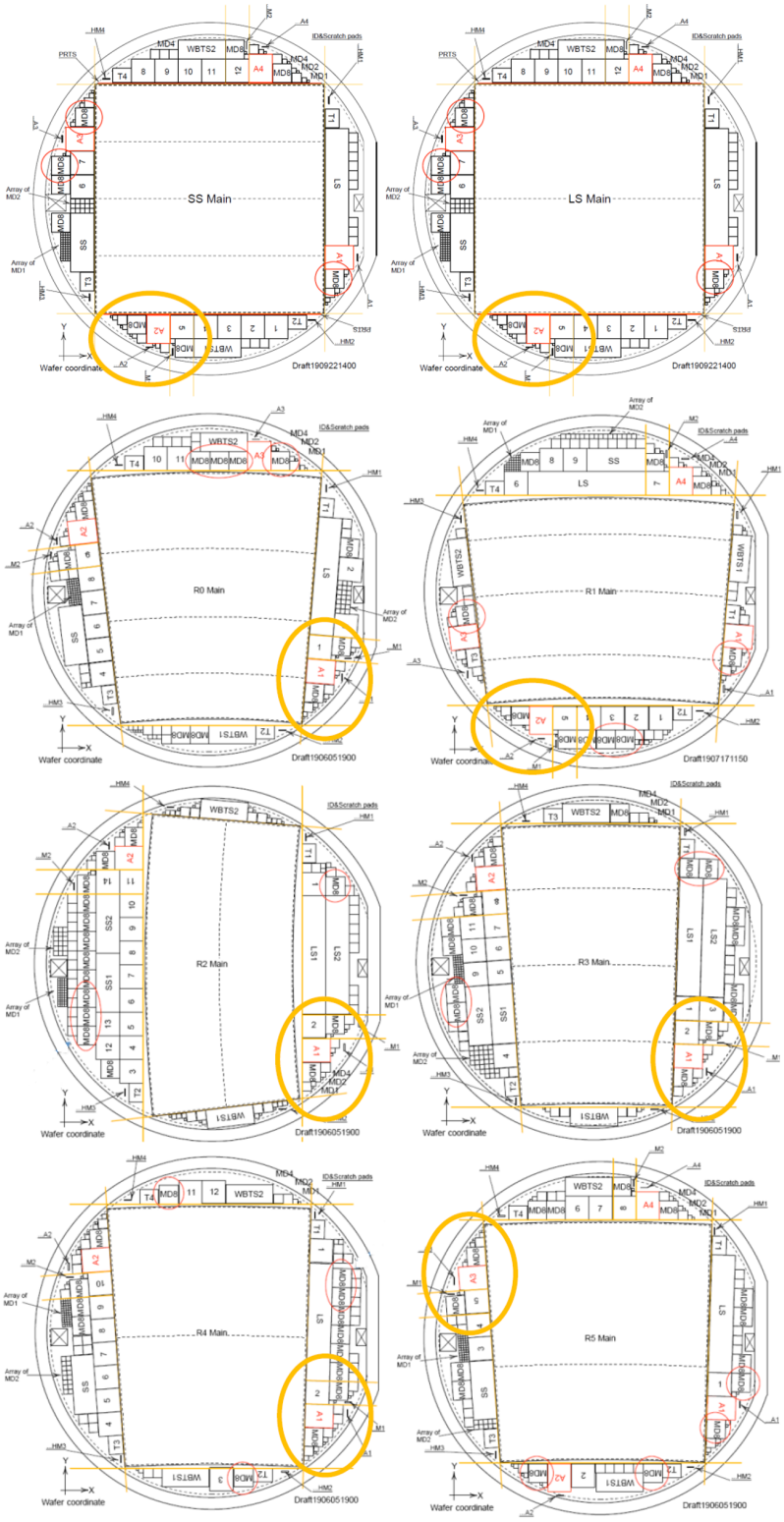


Fig. 4.12: Schemes of the eight wafers (two Barrel and six End-cap) to be used for the ATLAS ITk strip sensor production. QA test chip positions are indicated in red (labels from A1 to A4), and silicon pieces diced for the QA programme are circled in orange.

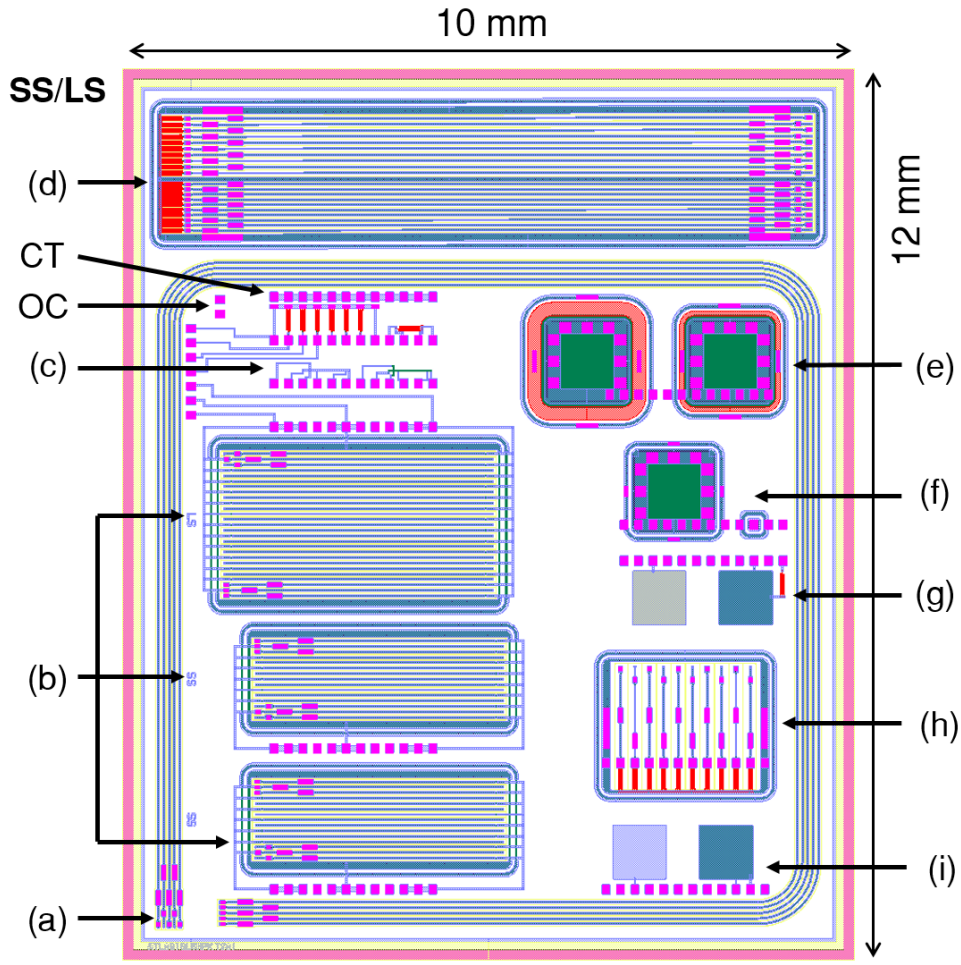


Fig. 4.13: ATLAS QA test chip, for the SS and LS Barrel wafer designs, including (a) 5-strips structure, (b) interdigitated structures, (c) bias and cross-bridge resistors, (d) miniaturized End-cap sensor, (e) gated diodes, (f) monitor diodes, (g) coupling capacitor for breakdown voltage and field oxide capacitor with p-stop, (h) punch-through protection structure and (i) coupling and field oxide capacitors. Each QA test chip also includes pads for capacitance open correction (OC) and needle contact tests (CT).

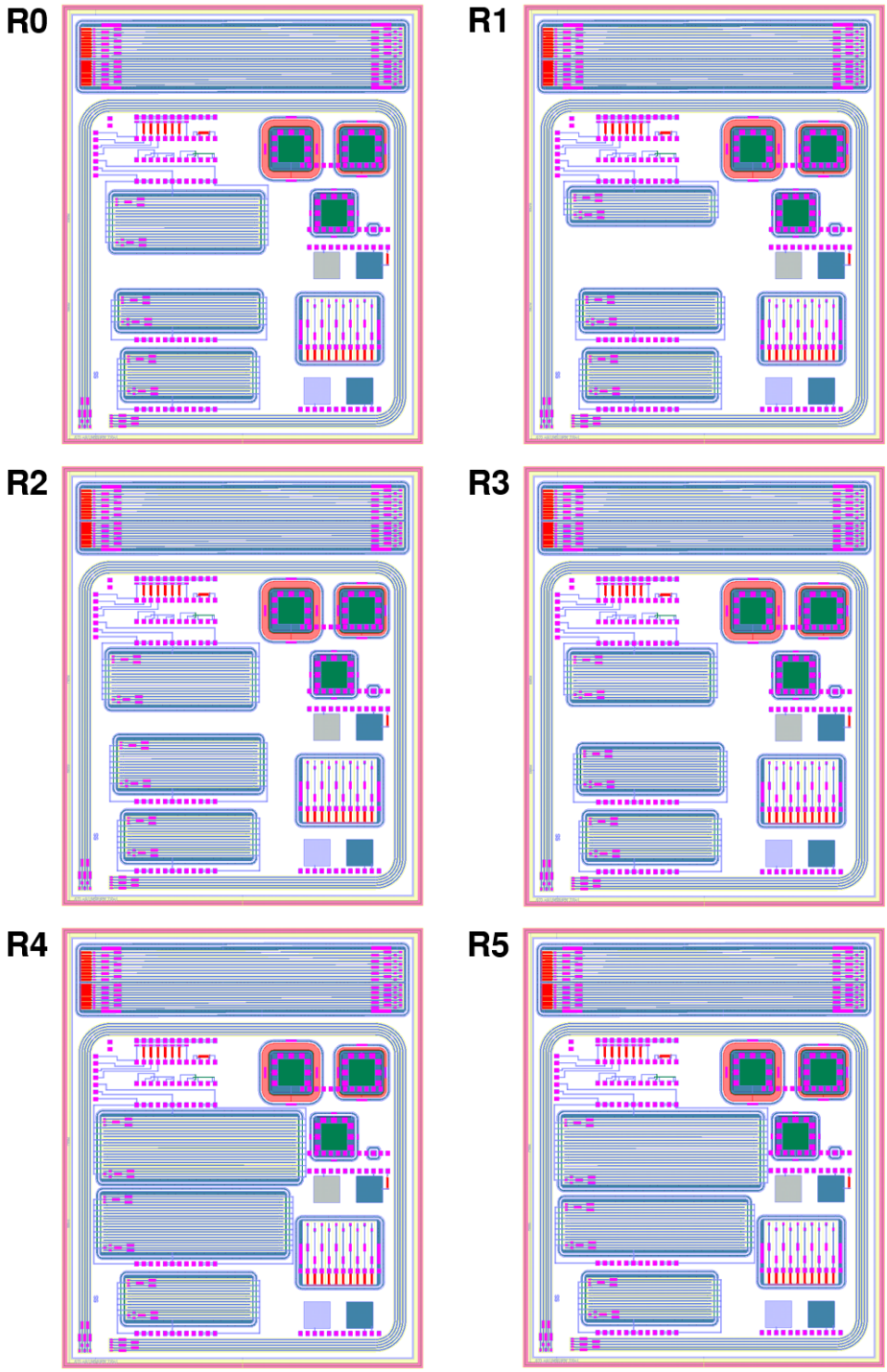


Fig. 4.14: ATLAS QA test chip for the R0, R1, R2, R3, R4 and R5 End-cap wafer designs, where the differences in the interdigitated structures can be observed.

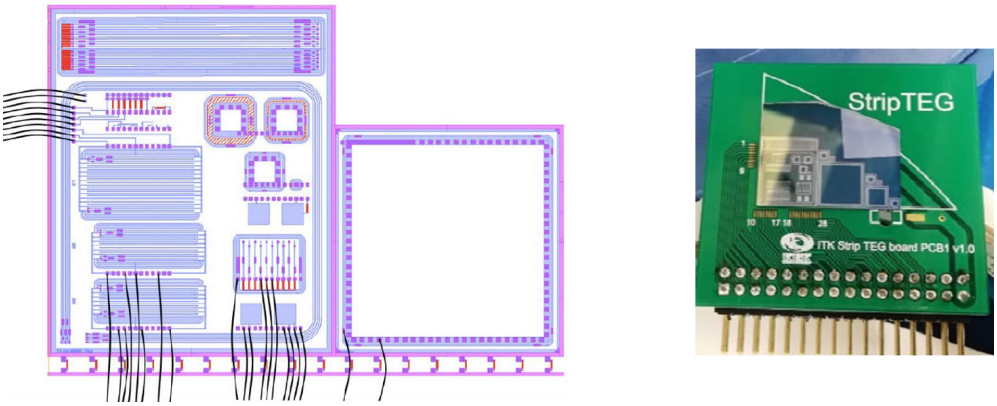


Fig. 4.15: Wire-bond schema (left) used for automatic tests of the QA silicon pieces on PCB board (right).

runs parallel to the perimeter of the test chip in order to gain as much length as possible. The total length of the central strip is 34 mm, which is close to the median of the different lengths of all the strip rows used in the different Main sensor designs, and the total area of the coupling capacitor of the central strip is 0.54 mm^2. The objective of the 5-strips structure is to measure most of the strip and inter-strip parameters, such as the strip implant resistance, strip metal resistance, coupling capacitance, inter-strip resistance and inter-strip capacitance. This structure is not equipped with probe-card pads, but allows the wire-bond of AC and DC pads due to the proximity to the chip edge (Figure 4.15).

Interdigitated Structures: The interdigitated structure consists of two sets of strip-like lines running parallel to each other, and each of the sets connected in parallel to one of the terminals of the structure at either side (Figure 4.16). The lines of each of the sets are alternated (interdigitated) with the lines of the other set. The total length and pitch is identical to the corresponding Main sensor, including p-stop isolation and AC/DC pads. A bias ring and a guard ring are included in order to deplete also the surrounding volume of the structure, similarly to the Main sensor.

Each QA test chip contains three different interdigitated structures adapted to each Barrel/End-cap Main sensor. For the Barrel wafer designs (ATLAS18LS and ATLAS18SS), two interdigitated structures corresponding to the SS (duplicated: bottom and central structures) and a third one corresponding to the LS (upper structure) are included in the QA test chip. On the other hand, for the End-cap wafer designs (ATLAS18R0 to R5), one interdigitated structure corresponds to the SS (bottom structure), in order to be able to compare between the different layouts, and the other two structures are associated to the bottom and upper strip rows of the corresponding End-cap Main sensor (see Figure 4.14 to observe the differences between test chips). With these structures, the measurement of inter-strip resistance with first neighbours is possible using a simple

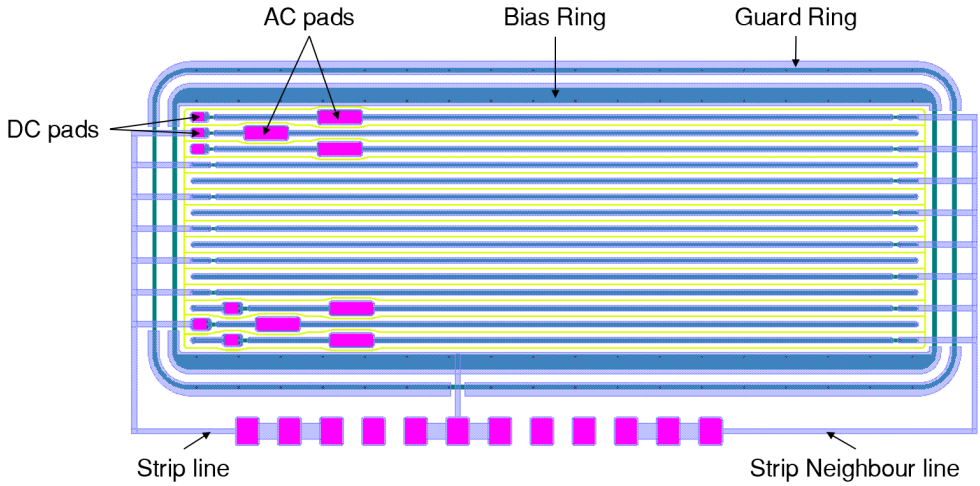


Fig. 4.16: Barrel Short-Strip interdigitated structure, corresponding to the strip length and pitch of the strip rows of the ATLAS18SS Main sensor.

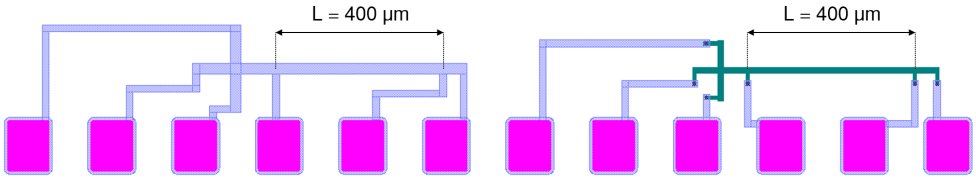


Fig. 4.17: Cross-bridge resistor structures for the strip metal (left) and for the strip implant (right).

resistance measurement between its two terminals. Inter-strip capacitance tests can also be made with this structure. Each interdigitated structure has a set of probe-card pads available, allowing also the possibility of wire-bonding due to the proximity to the edge of the test chip.

Bias and Cross-Bridge Resistors: The *cross-bridge resistor* (CBR) [85] structure is a combination of a *Greek cross* structure [86] and a *bridge resistor*. Two CBR structures are included, one for the metal and one for the strip implant (Figure 4.17), with a distance between the internal contacts in the bridge resistor of 400 μm for both structures. The objective of these structures is the measurement of the strip metal and strip implant sheet resistances and their effective line widths.

Additionally, a set of six bias resistors, identical to the ones included in the Main sensors, are included next to the CBR structures. The six (vertical) bias resistors include n-implant below the resistor, to replicate the topology present in the real Main sensors. These bias resistors are connected to test pads in one of their terminals, and to a common bus in the other terminal (Figure 4.18). An additional (horizontal) bias resistor is included which is connected to four test pads to allow for more precise

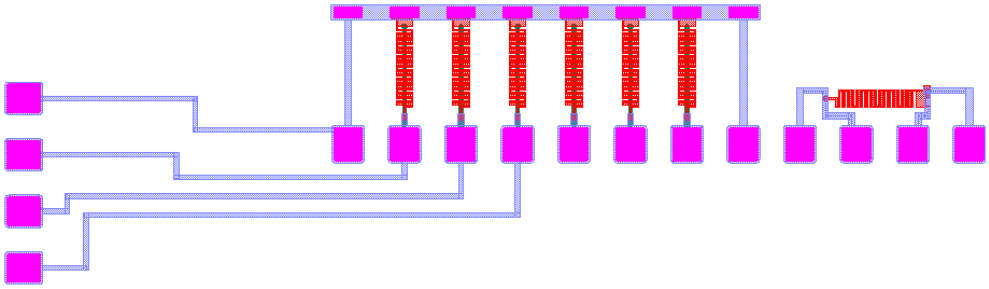


Fig. 4.18: Bias resistors test structure layout, including the bonding pads taken to the chip edge at the left hand side.

four-probe Kelvin measurements [79]. This structure includes bonding pads at the edge of the test chip to allow the measurement of three of the resistors by wire-bonding.

Miniature End-cap Sensor: This structure reproduces two sets of ten End-cap strips in a fan configuration in two independent active areas. The first active area (lower in Figure 4.13(d)) similar the shorter strip pitch in the End-cap petal (R3 lower strip row), starting with a 70 μm pitch with a 109.5 μrad pitch angle. The second active area (upper in Figure 4.13(d)) similar to the larger strip pitch in the End-cap petal (R0 upper strip row), finishing with a 83.9 μm pitch with a 171.7 μrad pitch angle. The bias ring and guard ring have a configuration identical to the Main sensors, and both active areas are separated by a bias rail. This structure can be also used to measure all the strip and inter-strip device parameters, but in this case the inter-strip parameters will be closer to the extremal End-cap cases. The structure has the possibility to wire-bond AC, DC and bias pads due to the proximity to the test chip edges.

Gated Diodes: Similarly to the gated diodes in the previous section (see Figure 4.10), in the QA test chip a set of two square 2x2 mm^2 diodes are included, but this time only with polysilicon gate in both diodes (Figure 4.13(e)). One gated diode with shorter gate (60 μm long) and other gated diode with larger gate (180 μm long). This structure can be used for the characterization of the Si/SiO_2 interface, via parametrization of the surface generation current. The set of pads are placed to be able to contact the diodes with a probe-card in an automatic probe table.

Monitor Diodes: A set of two square monitor diodes (2x2 and 1x1 mm^2), identical to the rest of the diodes included in the wafer, but without the edge structure (Figure 4.13(f)) are also included in the QA test chips. These diodes have pads in the central implant and guard ring of the 2x2 mm^2 diode for manual tests. As previously explained in Section 4.3.1, monitor diodes can be used to evaluate global parameters of the Main sensor, such as reverse leakage current, full depletion voltage or breakdown voltage, and can serve as a reference to standard diode for the gated diodes. A set of probe-card pads are placed to allow the measurement in an automatic probe table.

Field Oxide and Coupling Capacitors: A MOS field oxide capacitor (left in Figure 4.13(i)), and a square coupling capacitor (right in Figure 4.13(i)) are also included. The MOS structure has the same total area as the n-implant of the central strip of the 5-strips structure (0.54 mm^2), while the square coupling capacitor has a total area corresponding to the metal of the central strip of the 5-strips structure (0.56 mm^2). Both structures are connected to a set of probe-card pads, with the possibility of wire-bonding due to the proximity to the bottom edge of the test chip. As explained in the previous section, the MOS structure can be used to extract the values of the field oxide capacitance, field oxide thickness and the flat-band voltage through the capacitance measurements at high frequency.

Additionally, a second set composed of a MOS field oxide capacitor and a square coupling capacitor is included in the test chip (Figure 4.13(g)). In this case, the MOS structure includes a p-implant layer to extract the capacitance and thickness of the oxide on top of the p-stop. On the other hand, the square coupling capacitor includes a polysilicon bias resistor in series with the metal pad with the aim to perform destructive tests measuring the actual breakdown voltage of the coupling capacitor avoiding fast high current pulses when the breakdown is produced.

Punch-Through Protection (PTP) Structure: This structure consists of ten strip ends at the side of the bias resistor which includes the PTP structure, and surrounding everything with a bias ring and a guard ring (Figure 4.13(h)). The strip pitch is adapted to agree with the pitch between the test pads for automatic measurements (see Figure 4.19). The objective of the structure is to evaluate the PTP behaviour in the Main sensor by obtaining the PTP voltage and the effective PTP resistance. This structure has also the possibility of wire-bonding due to the proximity to the bottom edge of the QA test chip.

4.4 Embedded Pitch Adapters

In the development of the future generation of strip tracking sensors, a key aspect that also should be optimized is the interconnection of the sensors and the readout electronics. The rapid evolution of microelectronics brings to the HEP community the possibility to design sensors with larger dimensions, while the size of the readout ASICs is reduced and the number of channels is increased. A direct consequence of these modifications is a higher density of channels and an increase of the difference between the sensor strip pitch and the readout channel pitch. In these conditions, the module assembly process becomes especially challenging, due to the elevated number of connections combined with an increase of the angle needed to wire-bond each strip with the corresponding readout channels.

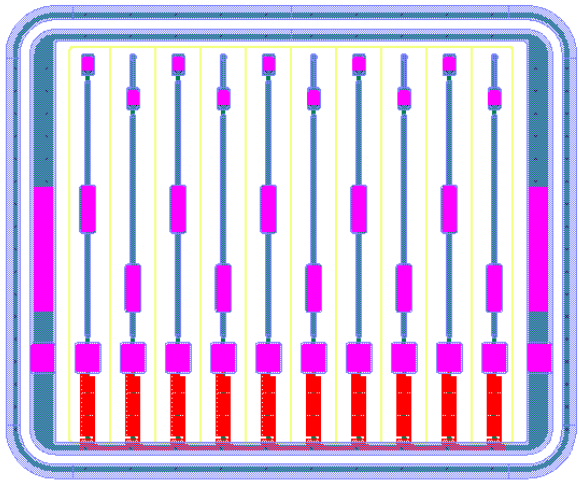


Fig. 4.19: Punch-Through Protection (PTP) structure with ten strip ends at the side of the bias resistor, with the pitch adapted to the probe-card pads, to evaluate the PTP behaviour of the Main sensor.

The interconnection issue of the HEP strip tracking sensors was previously faced by the ATLAS collaboration during the development of the sensors currently installed in the SCT. With the aim to facilitate the wire-bonding of the readout chip, an external pitch adapter was designed and fabricated on a glass substrate [87], and glued between the sensor and the readout electronics. The adapter was composed of metal tracks routing the strip pads (AC pads) to a new set of pads with the pitch of the ASICs channels ([88], [89]) (Figure 4.20). These pitch adapters allow the direct connection with parallel wire-bonds, avoiding angles that could lead in a reduction of the yield. However, although the bonding is very much facilitated, the number of wire-bonds is doubled, introducing new steps in the module assembly process, increasing also the total mass and cost of the tracking system. In consequence, the groups involved in the developments of the new ATLAS ITk decided in the prototype phase to avoid the use of external pitch adapters.

The new ATLAS ITk system is composed of eight sensor flavours with a novel approach in the End-cap region. The strips of the six different End-cap sensors are radially oriented, with a variable strip pitch, leading to a very challenging new scenario for the interconnection. Several studies were made to identify the maximum angle that can be achieved by direct wire-bonding between sensors and ASICs [90], concluding that angles below 20º can be considered safe, which can be applied to the Barrel sensors but could lead to a yield reduction for the End-cap designs.

A novel approach to solve the interconnectivity issues was proposed during the prototyping stage of the End-cap sensors. The solution consists of fabricating the large area sensors for the End-cap region with integrated, or “embedded”, pitch adapters.

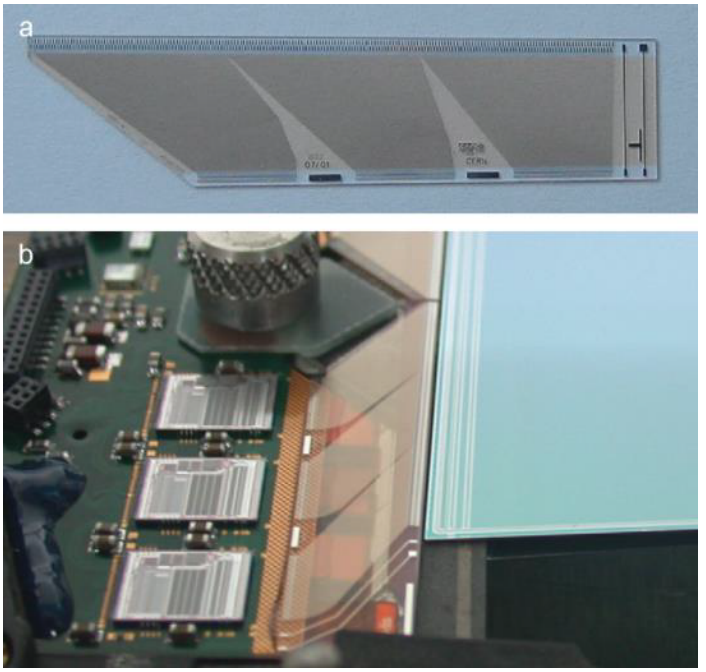


Fig. 4.20: Pitch adapter images. Glass pitch adapter (a) and its position in a current ATLAS End-cap module (b) [89].

To implement the Embedded Pitch Adapters (EPA), a second metal layer is used in the back end of line (BEOL) of the sensor fabrication. Additional metal tracks are created to route the top metal of the strip coupling capacitors (AC pads) to a new set of pads (embedded pads), with a pitch identical to the readout channels, located in front of the corresponding ASICs pads. This solution allows the direct wire-bonding, without the need to neither double the number of wire-bonds nor making them in angle, facilitating the interconnection between sensor and readout electronics (Figure 4.21). However, the implementation of the EPA can introduce possible adverse electro-mechanical effects that should be assessed not to compromise the production yield and sensor performance.

4.4.1 Design Considerations

From a mechanical point of view, the introduction of new steps in the sensor fabrication process, such as extra photolithographic steps for the second metal deposition and their contact opening (via) with the strip metal, could reduce the number of good sensors per batch affecting the production yield. A critical parameter in the fabrication of a large area strip sensor, with a complex multi-layer technology, is the stress generated in the wafer by the different layers, increasing drastically the bowing of the large format sensors. In consequence, the final device can compromise the module assembly or even present losses in performance efficiency. Moreover, the increase on the sensor bowing

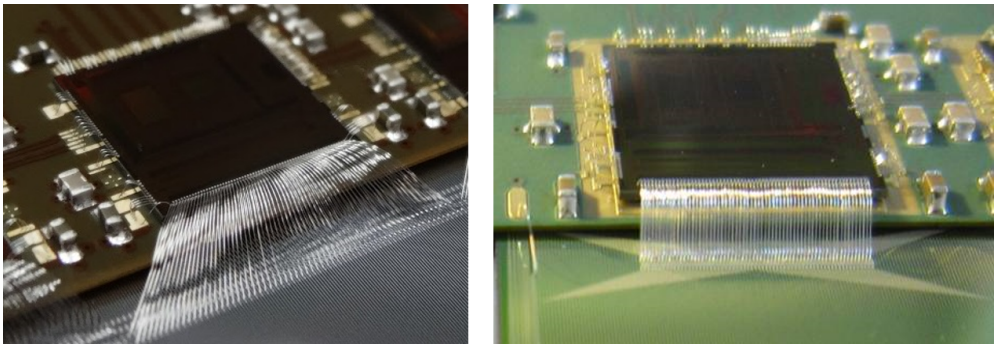


Fig. 4.21: Sensor-readout interconnection without pitch adapter (left) and with embedded pitch adapter (right).

can also difficult the mask alignment during the photolithographic processes, inducing the appearance of short-circuited or open channels. Thus, the fabrication process of large area sensors with EPA should be optimized to minimize the mechanical variations in the final device [91], ensuring the fulfillment of the sensor specifications established by the collaboration.

On the other hand, from an electrical point of view, the new solution can introduce effects in the sensor performance that should be taken into account to optimize the design of the EPA structures:

Inter-strip capacitance: The introduction of new metal tracks, routing the standard strip metals to a new set of embedded pads, increment the total length of the strip metals, inducing also a higher density of metal tracks conducting electrical signals. In consequence, an increase of the inter-strip capacitance is expected in the sensors with EPA, that implies an increase in the overall noise of the detector. Additionally, as the density and length of the different channels strongly depends on the way that the strips are routed, an increase in the noise variability between channels is also expected [91].

Cross-talk: The signal can be transmitted between the standard strip metal tracks and the EPA metal tracks due to the coupling between them. This phenomenon can induce spurious signals in channels not hitted and in loss of signal in the channel hit, which could result in a loss of efficiency.

Pick-up: Charges created in the bulk, when a particle crosses the sensor, can induce signals in the EPA metal tracks directly from the bulk [92]. Similarly to the cross-talk effect, the pick-up phenomenon can induce signals in channels not hitted and loss of efficiency in the hitted channels.

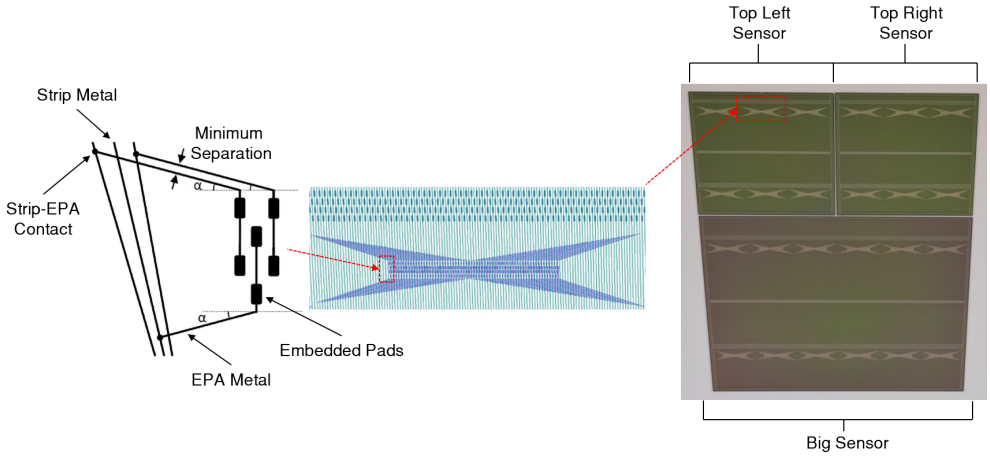


Fig. 4.22: First EPA design (*Basic*) showing initial design considerations for paths from strips to a double row of embedded pads (left), layout image of the Basic EPA design, showing the routing metal tracks in blue (center) and picture of the three Petalet sensors (Top left, Top right and Big sensor) with all the strips routed with the EPA Basic structure. Figure adapted from reference [23].

4.4.2 Layout Designs

At the first stages of the End-cap prototype phase, prior to this PhD thesis, a prototype called *Petalet* ([23], [93]) was developed by the ATLAS collaboration, and fabricated at the clean room of the IMB-CNM, to test the reliability of the novel strip tracking system. The Petalet prototype was composed of three different sensors, two at the upper part (*Top sensors*) and one at the bottom (*Big sensor*), with strips radially oriented emulating the final End-cap Petal system with reduced dimensions.

Taking advantage of this prototyping stage, a first EPA layout, called *Basic*, was designed and implemented on some of the Petalet sensors (Figure 4.22). In this first design, the EPA metal tracks keep the same angle (α in Figure 4.22) in each of the four quadrants, i.e. they are parallel to each other in the same quadrant, and this angle is the maximum that can be used for a minimum (technologically safe) separation between tracks of 20 μm. The structure is nearly symmetric with respect to the vertical and horizontal axis, the latter one coinciding with a double row of embedded bond pads. Strips with even numbers have the via contact, connecting them to the EPA tracks, located such that they are connected to the lower row of embedded bond pads, while odd-numbered strips are connected to the upper bond pads row from the other side (see Figure 4.22 (left)).

First results on these sensors showed no indication of cross-talk or pick-up from laser tests [63] but, as expected, an increase in noise and noise variability was observed in the first modules assembled with those sensors. Figure 4.23 shows a comparative plot

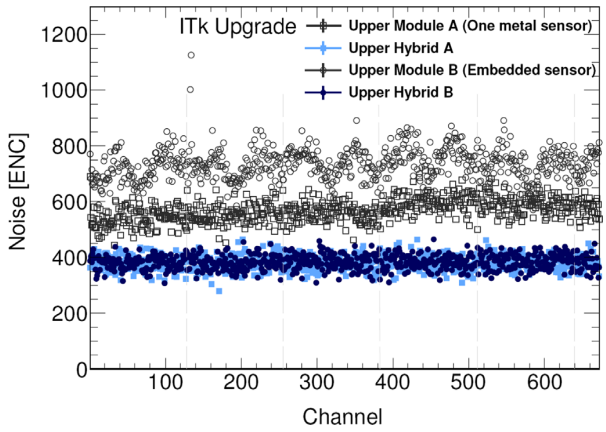


Fig. 4.23: Noise results on module for sensors with and without first Basic EPA design implemented, showing also the noise of the readout system, without the sensors, for reference [91].

of the noise measured on Top Left and Top Right Petalet sensors, with and without Basic EPA structures, showing an increase of the noise and a higher variability. This increased variability could be associated with an increase and variation of the inter-strip capacitance [91].

With these first results, indicating a clear influence of the EPA in the module noise, a new set of EPA structures were designed with the objective to optimize the electrical performance of the sensor. Besides the initial Basic structure, four different designs were laid out:

Equalized: Similarly to the Basic structure, the Equalized structure has parallel embedded tracks, with the same angle and separation between them, but all the tracks are enlarged in order to have the same length (Figure 4.24(b)). The aim of this structure is to equalize the inter-strip capacitance between the channels and to minimize the noise variability.

Varying: The embedded tracks in this structure have a constant angle with respect to each other. This angle is calculated so that they occupy all the 360º (180º/63=2.86º) (Figure 4.24(c)). The objective of this design is to reduce the inter-strip capacitance between EPA tracks, maximizing the separation between them. The tracks are also enlarged in the center to make them have roughly the same length, reducing the noise variability.

Rectangular-A: In this structure the EPA tracks go parallel to the strip metals from the embedded pads until they can cross perpendicularly to them to reach their corresponding via contact with the strip metal (see Figure 4.24(d)). The embedded tracks go in between the strip metals, and on top of the p-stop. The aim of this design is to reduce

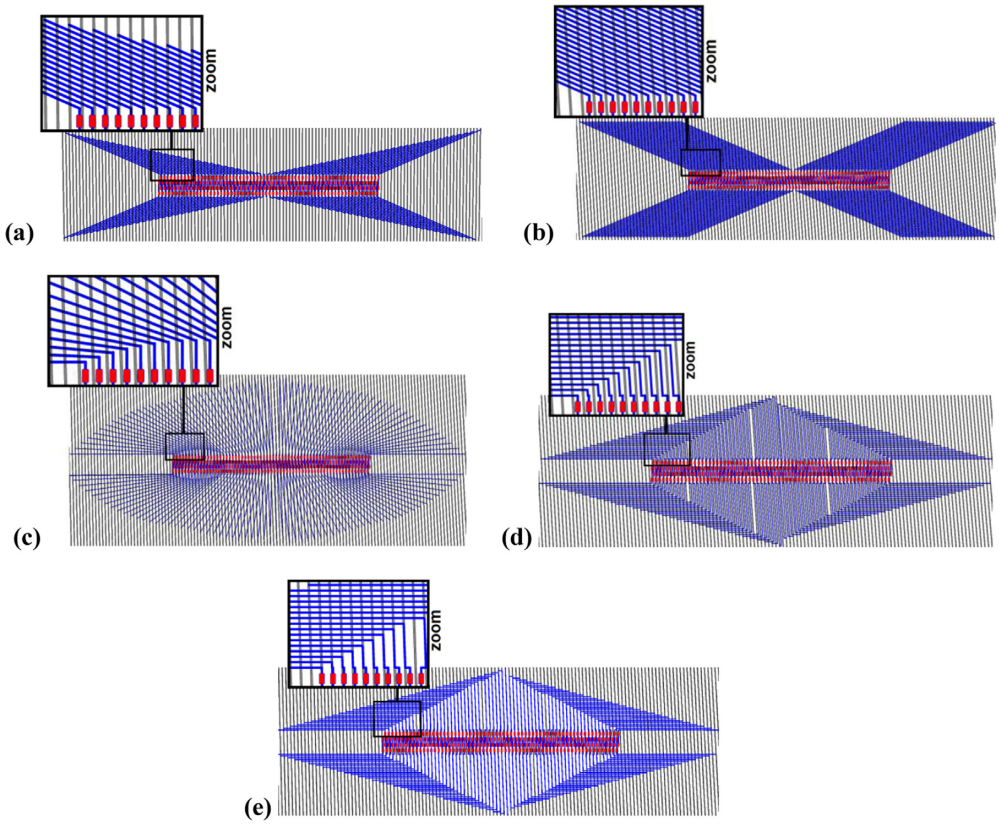


Fig. 4.24: Images of the five different EPA layouts designed: Basic (a), Equalized (b), Varying (c), Rectangular-A (d) and Rectangular-B (e) [91]. Strip metals are shown in grey and EPA metal tracks in blue.

the cross-talk and the pick-up placing the EPA tracks as far as possible from the strip metals and also on top of the p-stop, where it is expected that the signal coupling to the EPA tracks is minimized.

Rectangular-B: Similarly to the Rectangular-A structure, in this design the embedded tracks go parallel to the strip metals from the embedded pads, crossing perpendicularly to the strip metals directly to the corresponding via contacts, but in this case the EPA tracks go on top of the strip metals (Figure 4.24(e)). This structure minimizes the pick-up phenomenon, but an increase of the inter-strip capacitance and cross-talk between EPA tracks and strip metals can be expected.

Additionally, in order to study the variation of the inter-strip capacitance between embedded tracks, two versions of each EPA design were laid out: one with a track width of 20 μm and a second one with 10 μm. Finally, the fabrication of wafers was planned to include different oxide thicknesses (1, 2, 3 and 4 μm) between the strip metals and the EPA tracks, in order to minimize their contribution to the inter-strip

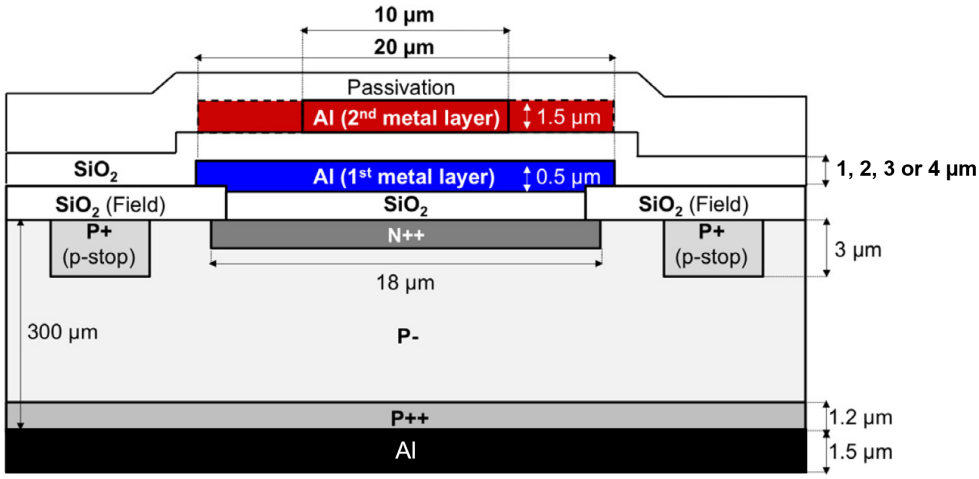


Fig. 4.25: Cross-sectional view of the Rectangular-B structure, where the embedded tracks (red) runs on top of the strip metals (blue), showing the planned variations on track width (10 and 20 μm) and inter-metal oxide (1, 2, 3 or 4 μm).

capacitance, studying also the influence on the wafer bowing and technological viability (Figure 4.25).

All these EPA designs were added to a new version of the Petalet Top sensors layout. Each of these sensors has two strip rows, each one with 384 strips that have to be connected to three ABC250 [94] readout chips, with 128 channels per chip. Then, the six EPA structures, including their alternative versions with different track width, were laid out on top of the Petalet sensors. The Basic structure, with a track width of 10 and 20 μm, was duplicated in order to cover all the strips available in both sensors. Figure 4.26 shows an image of the Petalet Top sensors layout, indicating the position of the different embedded pitch adapters.

4.5 Large Area Prototypes at Centro Nacional de Microelectrónica (IMB-CNM)

The fabrication of full-size prototypes is an essential stage in the development of the new large area strip technologies. IMB-CNM has the possibility to widely contribute to the R&D process thanks to its layout design and microfabrication capabilities. The novel ALGT software developed in the course of this PhD thesis, and detailed in Section 4.1, can be used to generate for the first time large area prototype layouts adapted to the IMB-CNM design rules. Moreover, the institute has in its cleanroom microfabrication facility most of the equipment necessary to fabricate strip sensors in 6-inch wafers, but the technology should be tested and optimized.

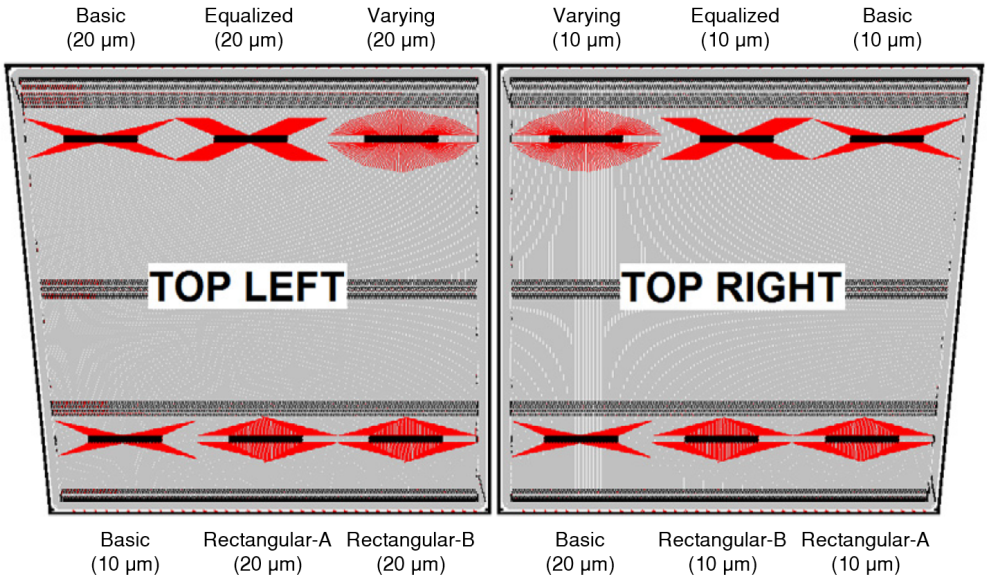


Fig. 4.26: Layout of the two Petalet Top sensors showing the position of the different EPA structures (in red).

4.5.1 Optimization of 6-inch Technology

With the aim to test the capability of IMB-CNM to fabricate strip sensors in 6-inch wafers, a first fabrication of ten wafers, called *Petalet150* prototype, was done using the Petalet Big sensor 4-inch masks on 6-inch wafers. Several critical fabrication steps were identified and studied during fabrication:

Field oxide: In order to isolate the silicon bulk and surface from readout lines and pads, the wafers were introduced in a tubular furnace to grow a thick silicon oxide (field oxide) layer of 800 nm, through a wet oxidation process. Measurements of the oxide thickness grown in the first 6-inch dummy wafers show areas with deviations up to 8.2% (Figure 4.27(left)), respect to the target value of 800 nm. A gradient of oxide thickness from the upper to the lower sides of the wafer is observed, with a total variation higher than 10%. Since the equipment is usually dedicated to process 4-inch wafers at IMB-CNM, the thickness variations could be attributed to a non-uniform diffusion of the oxidizer (i.e. H_2O saturated vapor) through the 6-inch wafer surface, causing variations in the oxide grown velocity in different areas of the wafer. In consequence, for this first prototype fabrication, the field oxide growth was adapted for 6-inch wafers carrying out the oxidation in two steps, performing a first oxidation of 400 nm and a second one rotating the wafers 180º. The wafers processed with this preliminary method present good uniformity of the field oxide thickness, showing variations of less than 3% (Figure 4.27(right)). Further studies should be done to

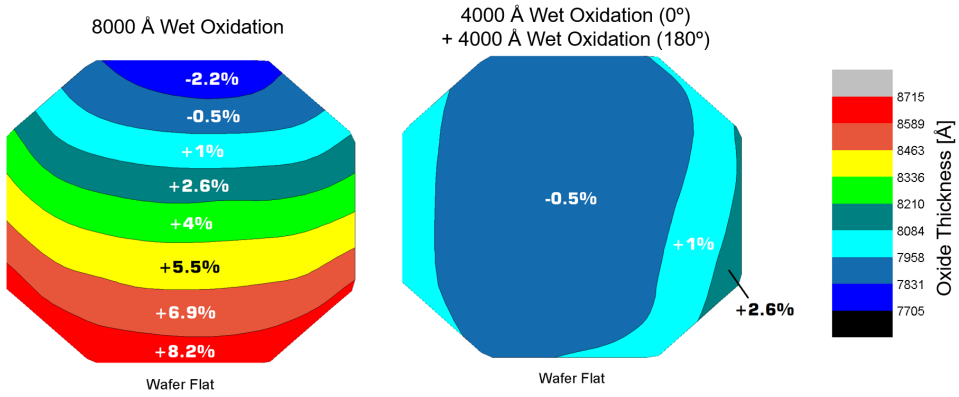


Fig. 4.27: Field oxide thickness homogeneity after an 800 nm wet oxidation performed in one step (left) and performed in two steps of 400 nm, rotating the wafer 180º (right).

optimize the parameters (i.e. oxidizer flow rate and pressure) to be used to obtain an uniform oxide grown over the 6-inch wafer surface in a single step.

Polysilicon bias resistor: The deposition of a 600 nm LPCVD (Low Pressure Chemical Vapor Deposition) polysilicon layer was carried out in the cleanroom of the Fondazione Bruno Kessler (FBK) [95], due to unavailability of equipment to deposit polysilicon layers in 6-inch wafers at IMB-CNM at the time of this fabrication. Beside the ten wafers for the prototype fabrication, three reference wafers were also sent to IMB-CNM, with polysilicon deposited, to calibrate the boron implantation dose (Figure 4.28) needed to obtain the target value of sheet resistance. From the bias resistor design included in the Petalet Big sensor wafer layout, a target polysilicon sheet resistance value of 3.8 ± 1.3 kΩ/square can be calculated in order to fulfil the ATLAS specifications for the bias resistance (1.5 ± 0.5 MΩ). The reference wafers were implanted with three different boron implantation doses and the sheet resistance was measured. A dose of $5{\cdot}10^{14}$ at/cm^2, with an implantation energy of 100 keV, was established for the fabrication process. At the end of this PhD thesis, IMB-CNM is installing a new LPCVD equipment able to deposit polysilicon layers in 6-inch wafers. Then, IMB-CNM will be able to deposit polysilicon layers in-house, but new tests should be performed in order to calibrate the new deposition and implantation parameters.

Homogeneous implantation area: The new large area designs for the ITk upgrade require homogeneous layers and implantations within a minimum wafer diameter of 140 mm in order to fit the full-size strip sensors. A first test was done on the edge of the 6-inch wafer to determine the area where the implantation is homogeneous. Taking advantage of the reference wafers used for the calibration of the polysilicon layer implantation, sheet resistance measurements were performed in steps of 2 mm at the very edge of the wafers to determine the variability of the implantation in this area. This experiment only showed remarkable variations, out of the wafer average values,

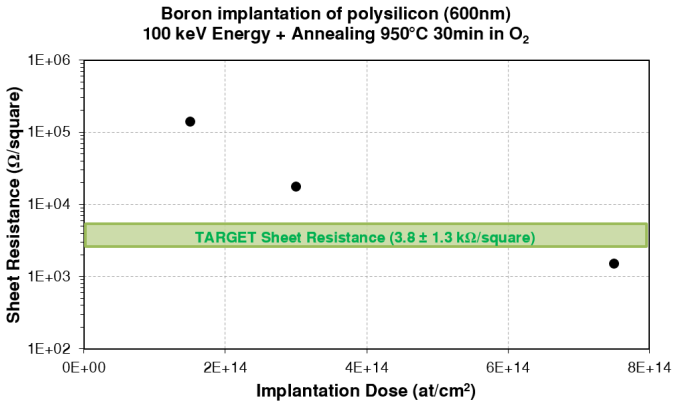


Fig. 4.28: Calibration of boron implantation dose, in a polysilicon layer deposited at FBK, to achieve a target sheet resistance of 3.8 $\pm$ 1.3 kΩ/square.

for distances to the silicon physical edge below 10 mm (Figure 4.29). Thus, this first experiment indicates that boron implantations within a diameter of 140 mm, in 6-inch wafers, can achieve good homogeneity. Further studies should be done to assess also the homogeneity of the different layers at the edge of the wafer.

Figure 4.30 shows a picture of one of the wafers, where strip sensors are fabricated for the first time on 6-inch wafers at IMB-CNM. The studies above show promising results in the fabrication of large area prototypes at the clean room of the IMB-CNM. However, further tests, e.g. wafer bowing or detailed studies of test structures, should still be done to optimize the fabrication steps and ensure a final sensor performance within the ATLAS specifications.

4.5.2 First Layout Design of Large Area IMB-CNM Prototype

In view of the promising results just mentioned about the capability of the IMB-CNM clean room to fabricate strip sensors in 6-inch wafers, a first layout of a full-size sensor was planned with the aim to fabricate the first in-house large area prototype. The ALGT software was used to generate a first version of a full-size Barrel Long-Strip sensor adapted to the IMB-CNM design rules (Figure 4.31), called *CNMBarrel150* prototype. Additionally, initial layouts of two different miniature sensors (10x10 mm^2 and 50x10 mm^2), with variations in the guard ring design (single guard ring and multiple guard rings), were also generated. Unfortunately, at the end of this PhD thesis the layout design, of the different devices and test structures, was not fully optimized due to time constraints. The layout design will be finished and fabricated in the near future, due to the demonstrated capability of IMB-CNM to fabricate strip sensors in 6-inch wafers.

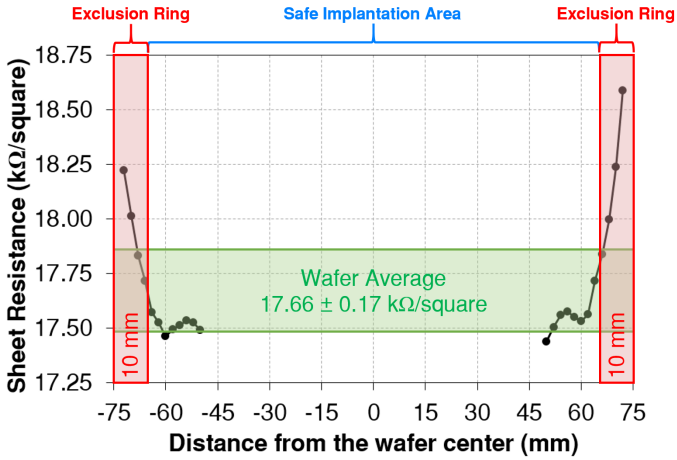


Fig. 4.29: Variability of polysilicon sheet resistance, after boron implantation, at the edge of the silicon substrate. No remarkable deviations out of the wafer average values (green) were observed for distances to the silicon edge above 10 mm (red).

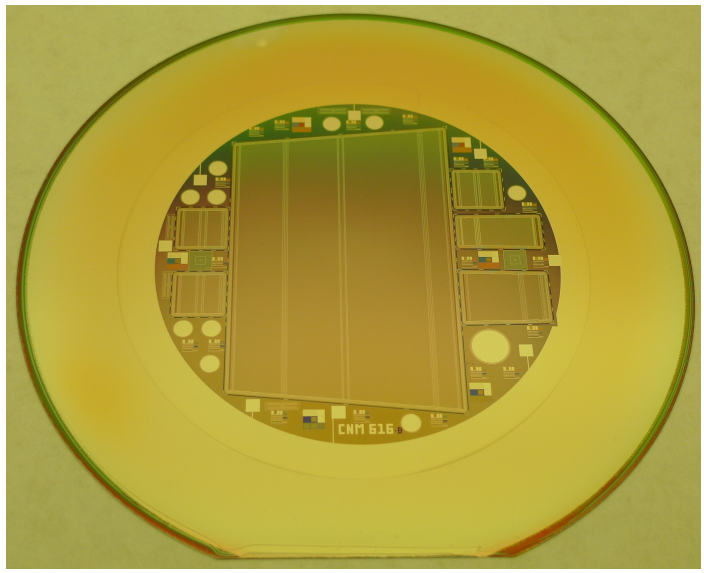


Fig. 4.30: Picture of Petalet Big sensor fabricated in 6-inch wafers (Petalet150 prototype).

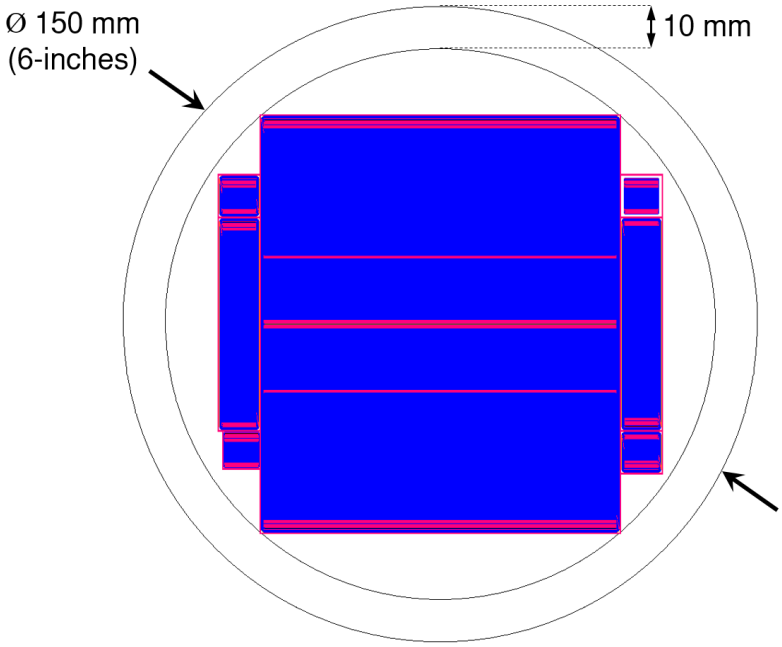


Fig. 4.31: Layout image of the first large area strip sensor designed with the IMB-CNM design rules (CNMBarrel150 prototype).

5

Characterization and Validation of Silicon Strip Detectors for the ATLAS Inner-Tracker Upgrade

This chapter presents the characterization work carried out during this PhD thesis for the development, evaluation and monitoring of new large area strip sensors for the forthcoming upgrade of the ATLAS Inner-Tracker (ITk). The first part of the chapter (Section 5.1) is dedicated to introduce the sensor performance requirements, irradiation campaigns and characterization methods established by the ATLAS collaboration for the evaluation of prototypes in the frame of the production Market Survey.

The second part evaluates the performance of the prototypes fabricated by the different foundries candidates to produce the new devices, i.e. Infineon Technologies AG and Hamamatsu Photonics KK. In particular, Section 5.2 presents the characterization of full-size Barrel Long-Strip sensors fabricated by Infineon using the layout detailed in Chapter 4. Similarly, Section 5.3 presents the evaluation of Hamamatsu as a candidate in the Market Survey, but this time the devices studied are miniature strip sensors included in the prototype wafers. The results of this evaluation were presented in the Final Design Review (FDR) of the ITk strip sensors with the objective to validate the sensor designs for the ATLAS upgrade.

The third part of the chapter is dedicated to the study of the microelectronic test structures designed in the framework of this thesis, also detailed in Chapter 4. Section 5.4 presents the results obtained with the test structures designed for the Infineon prototype, that demonstrate their usefulness in the development of new large area strip technologies. In addition, Section 5.5 shows first measurements of the Quality Assurance (QA) test structures to be used to monitor the performance of the devices fabricated by Hamamatsu during the five years of production. Finally, as a reference, Section 5.6 summarizes all the results presented in this chapter.

		ATLAS ITk Strip Sensor Specifications	
		Market Survey (ATLAS17LS)	*Production (ATLAS18)*
Global Parameters	***Leakage Current*** ***($\mu A/cm^2$)***	<0.1 at 700 V (Pre-irrad) <100 at 700 V (Post-irrad)	
	Breakdown Voltage (V)	>700 (Pre-irrad) >700 (Post-irrad)	
	Full Depletion Voltage (V)	<300 (Pre-irrad) No Criteria (Post-irrad)	<330 (Pre-irrad) No Criteria (Post-irrad)
Inter-strip Parameters	***Inter-strip Capacitance (pF/cm)***	<1 at 300 V (Pre-irrad) <1 at 300 V (Post-irrad)	<1 at 300 V (Pre-irrad) <1 at 400 V (Post-irrad)
	Inter-strip Resistance (GΩ)	$>1.5{\cdot}10^{-2}$ at 300 V (Pre-irrad) $>1.5{\cdot}10^{-2}$ at 300 V (Post-irrad)	$>1.5{\cdot}10^{-2}$ at 300 V (Pre-irrad) $>1.5{\cdot}10^{-2}$ at 400 V (Post-irrad)
Single Strip Parameters	***Coupling Capacitance (pF/cm)***	$\geq$ 20 (Pre-irrad) No Criteria (Post-irrad)	
	Strip Implant Resistance (kΩ/cm)	<50 (Pre-irrad) No Criteria (Post-irrad)	
	Strip Metal Resistance (Ω/cm)	<30 (Pre-irrad) No Criteria (Post-irrad)	
	Bias Resistance (MΩ)	1.5 $\pm$ 0.5 MOhm (Pre-irrad) 1.5 $\pm$ 0.5 MOhm (Post-irrad)	
	Punch-through Voltage (V)	No Criteria	

Tab. 5.1: ATLAS Specifications for the ITk strip sensor Market Survey (ATLAS17LS) and for the strip sensor production (ATLAS18).

5.1 ATLAS Specifications, Irradiation Campaigns and Test Methods

The ATLAS collaboration developed a complete characterization programme to evaluate the capability of different foundries to fabricate large area strip sensors. The results obtained through these tests are compared with the specifications established for the forthcoming High-Luminosity Large Hadron Collider (HL-LHC). These requirements can be found in the document *Technical Specification for the Supply of ATLAS17LS Strip Sensors* [67], published in June 2017 as reference for the ITk strip sensor Market Survey. After this evaluation process, the collaboration decided to adapt a few of these requirements for the production stage (ATLAS18), based on the knowledge acquired during the Market Survey. Table 5.1 summarizes the parameter requirements stated in these documents, that will be used to evaluate the different results obtained in this chapter.

In order to test the radiation hardness of the fabricated devices, a set of full-size sensors and test structures were selected and irradiated to increasing fluences up to the ones expected at the end of the ten years of lifetime of the HL-LHC experiment. In particular, the proton irradiations were performed making use of three different facilities: the *Cyclotron and Radioisotope Center* (CYRIC) of Tohoku University (Japan) [96] with 70 MeV protons, the *Proton Synchrotron* (PS) at CERN (Switzerland) [97] with 24 GeV protons, and the *Birmingham Irradiation Facility* of University of Birmingham

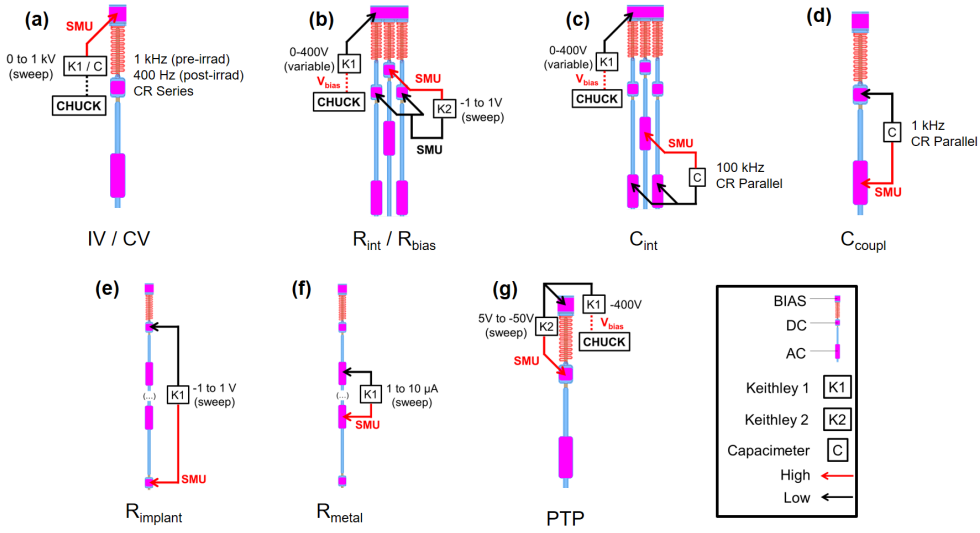


Fig. 5.1: Testing methods for the ATLAS strip sensor Market Survey to evaluate the sensor leakage current (IV) and bulk capacitance (CV) (a), inter-strip (R_{int}) and bias (R_{bias}) resistance (b), inter-strip capacitance (C_{int}) (c), coupling capacitance (C_{coupl}) (d), strip implant resistance ($R_{implant}$) (e), strip metal resistance (R_{metal}) (f) and punch-through protection (PTP) (g).

(United Kingdom) [98] with 23 MeV protons. Devices were irradiated to different proton fluences up to a 1-MeV equivalent neutron (n_{eq}) fluence of 10^{16} cm^{-2}. The neutron irradiations were performed at the *TRIGA-Mark-III nuclear reactor* of the Jožef Stefan Institute (Slovenia) ([99]–[101]) up to 10^{16} n_{eq}/cm^2. The gamma irradiations were carried out at *Institute of Physics of the Czech Academy of Sciences* (FZU) (Czech Republic) [102], with ^{60}Co gammas, up to a total ionizing dose of 70 Mrad(Si). All the irradiated devices were annealed for 80 minutes at 60°C in a dry environment (RH<5%), parameters corresponding to the optimal *short term* annealing, as discussed in Section 2.3.3.

Based on the standard test methods, detailed in Section 2.4, and the ATLAS specification documents, Figure 5.1 shows schematic representations of the characterization methods and parameters used for the evaluation of the devices fabricated for the Market Survey. A shielded Cascade Summit probe station in a dry environment (RH<5%), using a nitrogen flow, was used for all the electrical tests. Keithley 2410 instruments were used as a power supplies and Source-Meter Units (SMU), except for the set-up to obtain the bias resistance and the inter-strip resistance (Figure 5.1(b)), that were measured using a Keithley 4200 as a SMU. On the other hand, an Agilent 4284A LCR meter was used for all the set-ups involving capacitance measurements (Figure 5.1(a), (c) and (d)). Except for a few cases, explicitly indicated in the text, all the measurements before irradiation were performed at 20°C and after irradiation at -20°C, using for the device cooling an ESPEC ETC-200L thermal chuck.

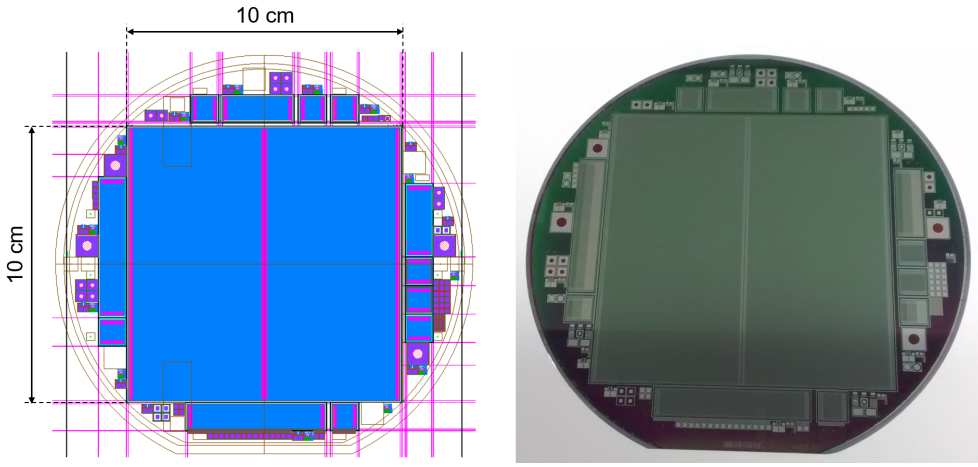


Fig. 5.2: Layout image (left), showing the dimensions of the Main sensor, and fabricated wafer (right) for the participation of Infineon in the ATLAS ITk strip sensor Market Survey.

5.2 Market Survey Evaluation of Infineon Technologies AG

For the ATLAS strip sensor Market Survey, Infineon Technologies AG (IFX) provided a total of six full wafers to the ATLAS collaboration, fabricated using the ATLAS17LS-IFX full wafer layout (Figure 5.2) detailed in Section 4.2.2. As shown in Table 4.3, each wafer contains a Barrel Long-Strip (LS) sensor (*Main sensor*), eight miniature sensors (1x1 cm^2), two miniature Short-Strip (SS) sensors (2.6x1 cm^2), two miniature Long-Strip sensors (5x1 cm^2), several monitor diodes (from 1x1 to 8x8 mm^2) and a wide range of microelectronic test structures for the technological studies.

5.2.1 Devices Tested

Two Main sensors were selected and irradiated with protons and with neutrons, at CYRIC and IJS respectively, both up to $5.1 \cdot 10^{14}$ n_{eq}/cm^2. A non-irradiated sensor was also tested to evaluate the performance of the Infineon Main sensors before irradiation.

Additionally, the ATLAS collaboration has assembled one of the Main sensors fabricated by Infineon in a prototype Barrel module. Although this study is not a part of the Market Survey, it is a valuable tool to verify the performance of the sensor in working conditions similar to the expected after its installation on the ATLAS detector. First results on module leakage current and module noise will be also shown in this section.

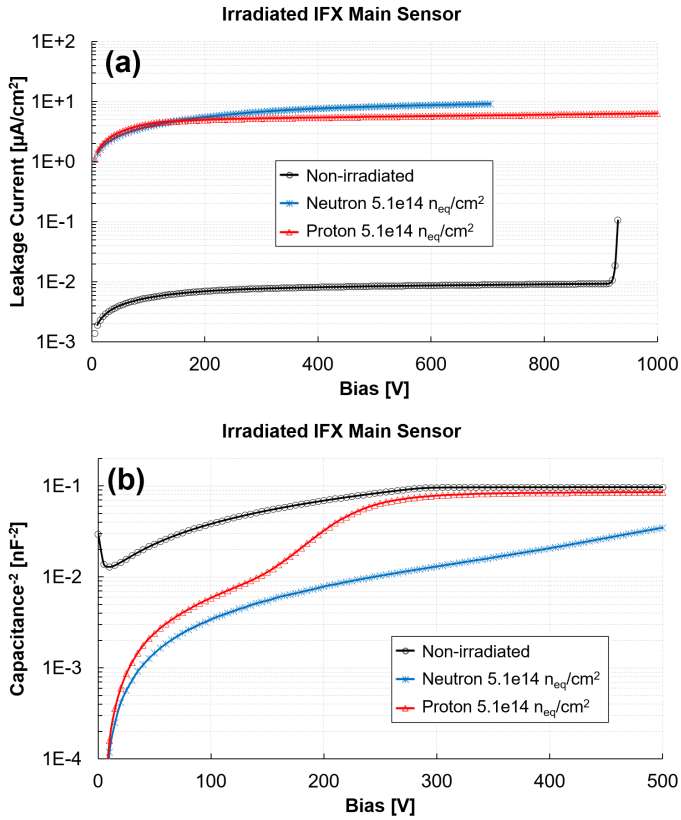


Fig. 5.3: Reverse bias leakage current (a) and bulk capacitance (b) of ATLAS17LS-IFX Main sensor before and after proton and neutron irradiation.

5.2.2 Global Performance Evaluation

The reverse bias leakage current measurement and bulk capacitance measurement were performed using the set-up schematized in Figure 5.1(a). For this Market Survey evaluation, the bias voltage sweep was applied up to 1 kV for the IV test, and up to 500 V for the CV measurement. The bulk capacitance was measured at 1 kHz for the unirradiated sensor and at 400 Hz after irradiation, with a RC-series configuration.

Figure 5.3 shows the IV and CV measurements of the Main sensors before and after proton and neutron irradiation. The sensor not irradiated shows a baseline current below 0.1 μA/cm^2, and below 0.1 μA/cm^2 after irradiation, showing no breakdown below 700 V. The full depletion voltage was extracted from the representation of the inverse-square of the bulk capacitance [35], considering the voltage corresponding to the intersection point of the two linear fits the bias needed to fully deplete the devices, obtaining a value of 290 V before irradiation. All these parameters are in good agreement with the limits established in the ATLAS specifications (Table 5.1).

5.2.3 Inter-strip Characterization

The study of the inter-strip parameters, such as the capacitance or the resistance between consecutive strips, provides valuable information of the strip isolation or the level of noise that these devices will have assembled in modules, that is directly related to the inter-strip capacitance of the sensors. These measurements were performed using the set-up shown in Figure 5.1(b) and (c). Both tests were carried out increasing the bias voltage up to 400 V with the objective to fully deplete the devices, and check its influence on the inter-strip characteristics. A sweep voltage, from -1 to 1 V, was applied to the strip under test for the inter-strip resistance measurement. On the other hand, the inter-strip capacitance was tested at a frequency of 100 kHz, with a RC-parallel configuration, before and after irradiation.

Figure 5.4(a) presents the measured inter-strip resistance (R_{int}) as a function of the bias voltage, showing a decrease of approximately two and four orders of magnitude, at 400 V, for sensors irradiated with neutrons and protons, respectively. Figure 5.4(b) presents the inter-strip capacitance (C_{int}) measured in twelve consecutive strips, showing no influence of radiation. Both inter-strip parameters show good homogeneity across the strips, with only some variability for the inter-strip resistance of the unirradiated sensor, that can be associated with the low currents measured, close to the limit of the equipment (below nA). All the inter-strip parameters are within the ATLAS specifications, that sets a lower limit of 20 MΩ for the inter-strip resistance and an upper limit of 1 pF/cm for the inter-strip capacitance.

5.2.4 Single Strip Characterization

The single strip characterization for the Market Survey evaluation consisted of five different measurements to test basic parameters, such as the bias resistance (R_{bias}, the coupling capacitance (C_{coupl}), the strip implant resistance ($R_{implant}$), the strip metal resistance (R_{metal}), and the punch-through voltage (V_{PT}). The set-ups used for the single strip characterization are shown in Figure 5.1(b), (d), (e), (f) and (g), respectively. In particular, for the Market Survey evaluation, the coupling capacitance was measured at 1 kHz in RC-parallel mode, and the resistance tests were performed applying a voltage sweep from -1 to 1 V, for the bias resistance and implant resistance, and a current sweep[1] from 1 to 10 μA, for the metal resistance. The characterization of the PTP structure, on the other hand, was performed with the device fully depleted at 400 V, and applying a voltage sweep from -5 to 50 V to the strip under test.

[1] Strip metal resistance measurements are performed applying current, and measuring voltage, in order to avoid the high currents expected for a resistance in the order of few Ω/cm.

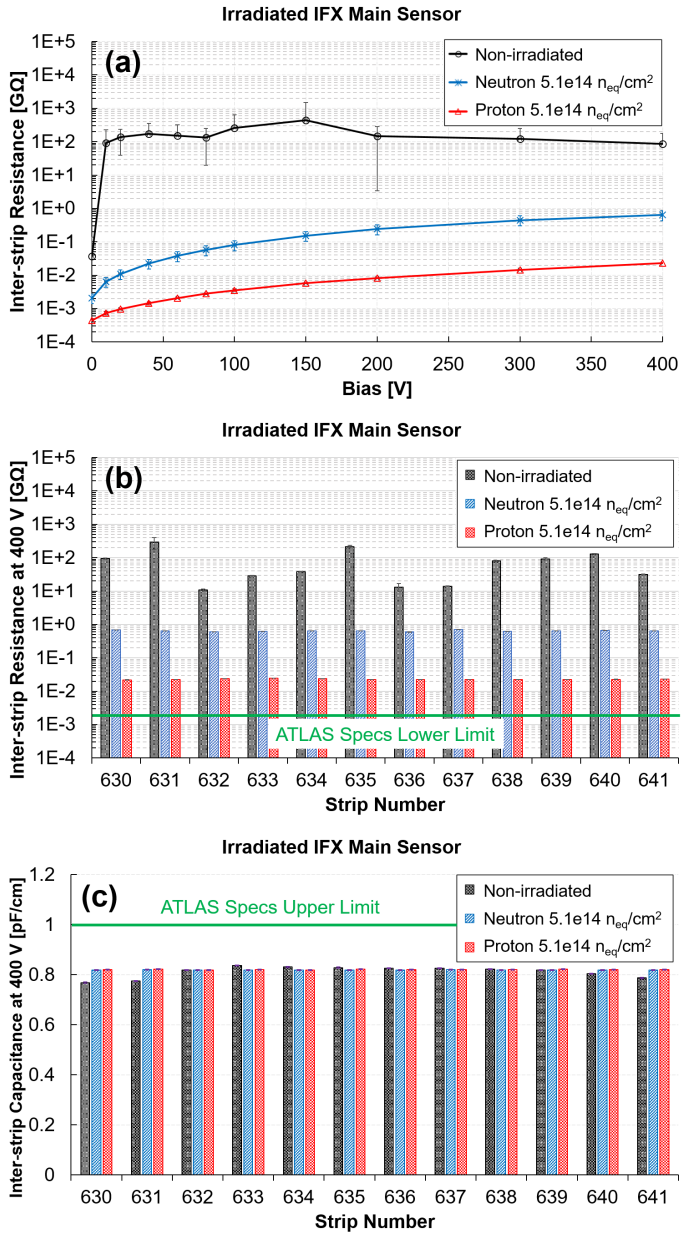


Fig. 5.4: Average inter-strip resistance in function of bias voltage (a), inter-strip resistance (b) and inter-strip capacitance (c) at 400 V for twelve consecutive strips of the ATLAS17LS-IFX Main sensor before and after proton and neutron irradiation.

Figure 5.5(a) shows the coupling capacitance values, averaged for measurements of twelve consecutive strips. Similarly, Figure 5.5(b) and (c) shows the averaged resistance values for the strip implant and strip metal, and Figure 5.5 the bias resistance results. No remarkable influence of irradiation is observed for these parameters, showing values within the ATLAS specifications. However, it is worth noting that the values obtained for the polysilicon bias resistance are slightly higher than the range established by ATLAS, with an increase after irradiation, especially for the sensor irradiated with neutrons. Nevertheless, the polysilicon bias resistance value could be easily tuned, adapting the layout and/or the doping process of the polysilicon layer to reduce its sheet resistance. Finally, Figure 5.7 presents the strip-to-bias ring current and the PTP effective resistance versus the voltage applied to the strip, calculated using Equation 2.5. Then, the punch-through voltage (V_{PT}) can be extracted if the condition $R_{PT} = R_{bias}$ [44], i.e. $R_{eff} = R_{bias}/2$, is applied to the equation, obtaining a value of 7.4 V for the unirradiated sensor, and 18.4 and 30.6 V for the devices irradiated with protons and neutrons, respectively. Thus, a clear increase of the punch-through voltage after proton and neutron irradiations is observed. The punch-through performance is a key parameter to evaluate the capability of the strips to evacuate high currents through the grounded bias implant, e.g. in case of beam-loss failure[2], but the limits for the different punch-through parameters are not defined in the ATLAS ITk specifications.

5.2.5 Module Performance

The ATLAS17LS-IFX Main sensor, used for the tests before irradiation shown in the previous section, was sent to the Santa Cruz Institute for Particle Physics (SCIPP) in the USA. The sensor was assembled on a prototype Barrel module [103] (Figure 5.8) with the aim to test the sensor performance with all the module components. As detailed in Section 4.2, the ATLAS17LS-IFX Main sensor is composed of two strip rows, each one containing 1280 strips and two unconnected edge strips. All the strips were wire-bonded to 10 analogue front-end ABC130 readout chips, each one with 256 input channels, supported by a flexible circuit board (hybrid) glued on top of the sensor, close to the center of the sensor to facilitate the connection of both strip rows. The hybrid board also contains a *Hybrid Chip Controller* (HCC130), that provides the interface between the ABC130 readout chip and the off-detector electronics. A DCDC power converter, a high voltage switch and a monitoring chip are implemented on a flex circuit board, called powerboard, and also glued on top of the sensor.

Figure 5.9 shows the sensor leakage current before and after the module assembly, both performed at 20ºC and dry environment (RH<10%). For this particular module, SCIPP reported a built-in curvature on the hybrid used, which interferes with the usual hybrid support, so a non-standard technique was used for the assembly, including spacers

[2]Study of the punch-through protection performance in a beam-loss scenario is presented in Section 6.2.

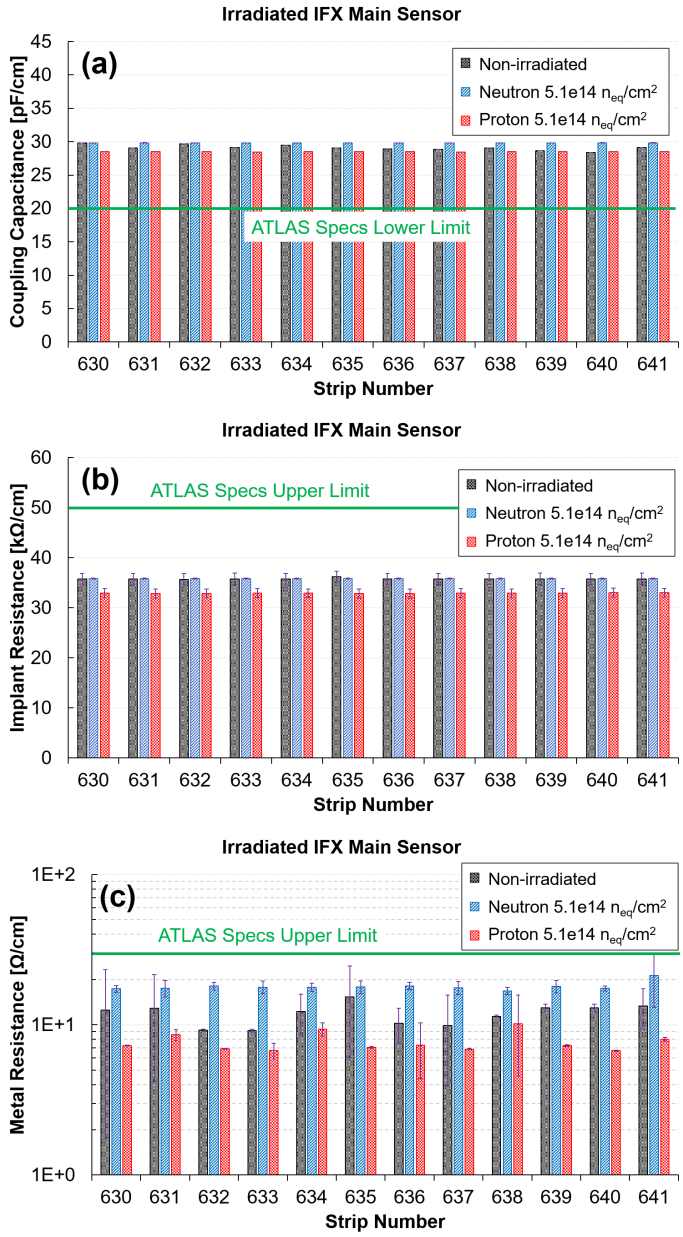


Fig. 5.5: Coupling capacitance (a), strip implant resistance (b) and strip metal resistance (c) for twelve consecutive strips of ATLAS17LS-IFX Main sensors before and after proton and neutron irradiation.

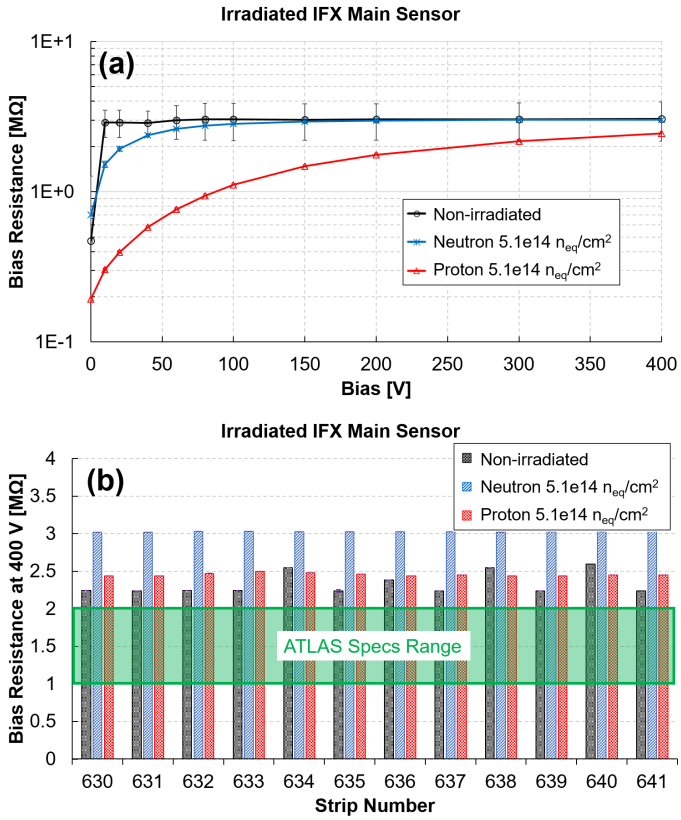


Fig. 5.6: Average bias resistance in function of bias voltage (a) and value at 400 V for twelve consecutive strips of ATLAS17LS-IFX Main sensors before and after proton and neutron irradiation.

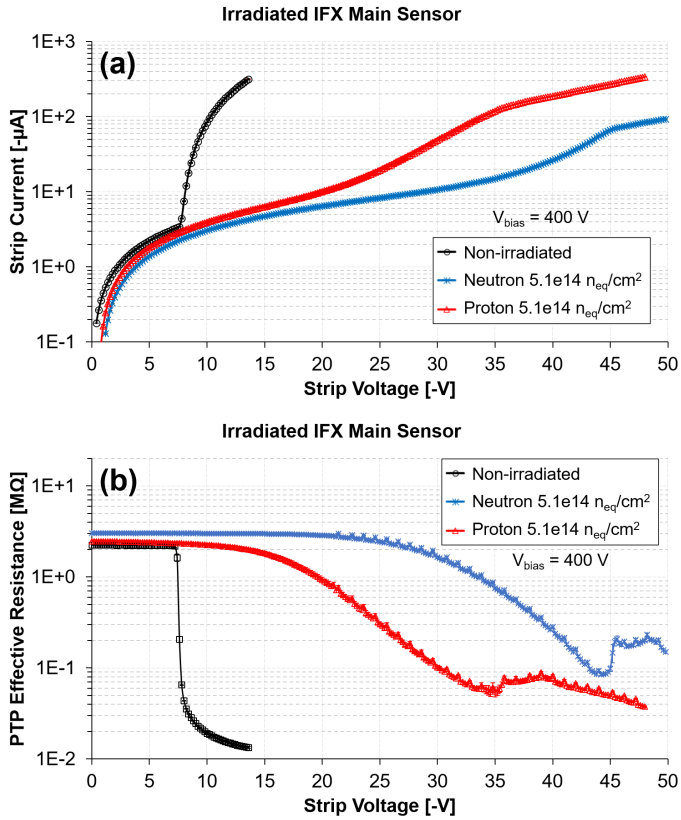


Fig. 5.7: Average strip current (a) and punch-through protection effective resistance (b) at 400 V for twelve consecutive strips of ATLAS17LS-IFX Main sensors before and after proton and neutron irradiation.

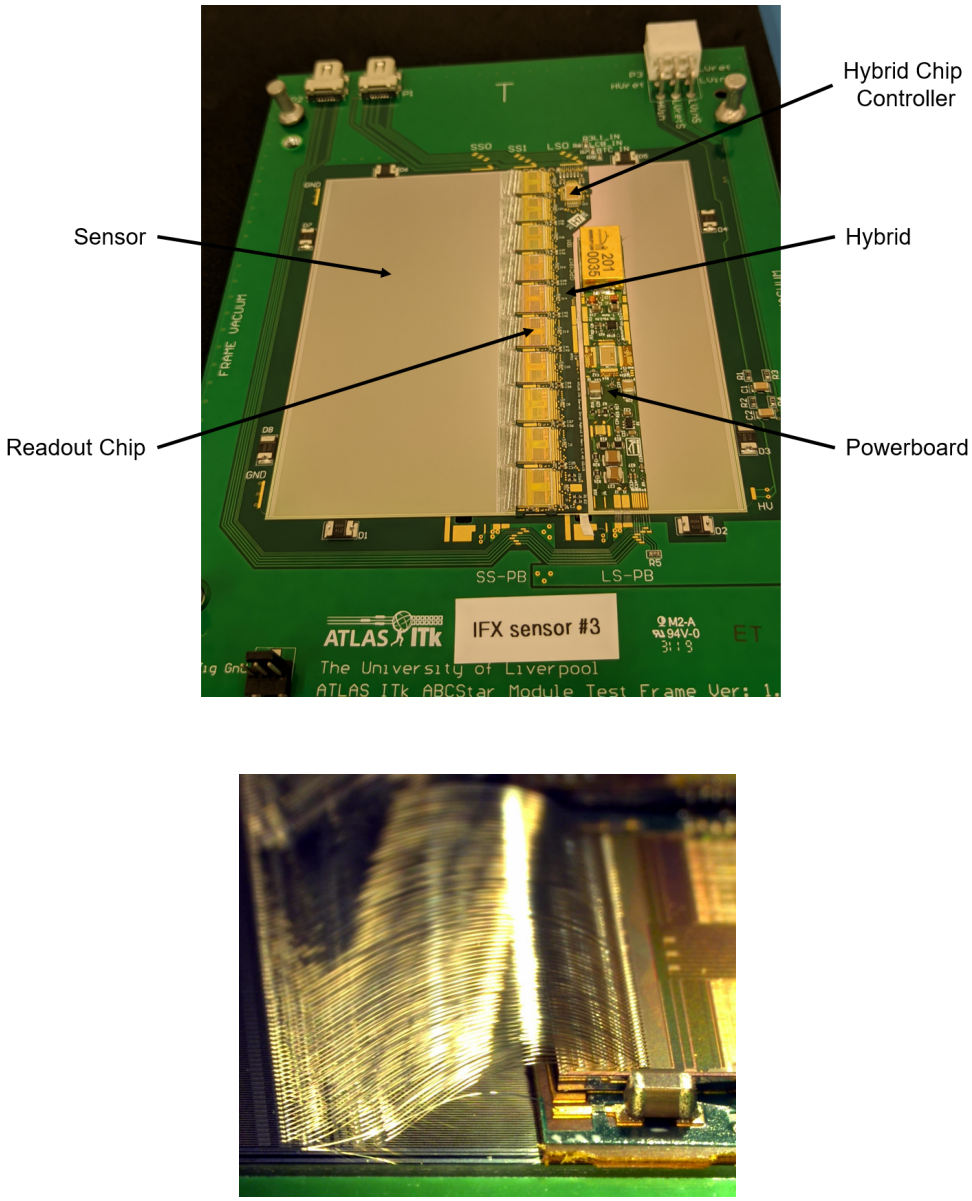


Fig. 5.8: Main sensor fabricated by Infineon for its participation in the Market Survey (ATLAS17LS-IFX), assembled in a prototype Barrel module (top), and picture of an ABC130 readout chip wire-bonded to a Barrel LS sensor (bottom), taken by the ATLAS collaboration during the module prototyping phase [103].

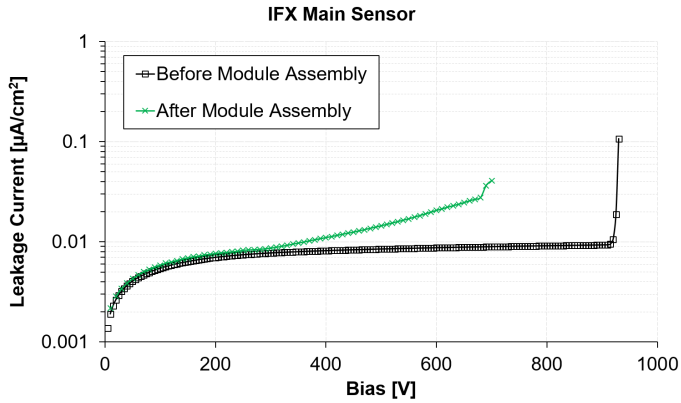


Fig. 5.9: Reverse bias leakage current of the ATLAS17LS-IFX Main sensor before and after module assembly.

under the hybrid positioned very close to the bias ring. Consequently, the soft rise of the current, and the reduction of the breakdown voltage, observed after the module assembly process could be related to this variation in the assembly process.

Additionally, *Three Point Gain* measurements were performed injecting three different amounts of charge and varying the threshold value of the discriminator from zero to its maximum. The measured average hit rate versus threshold was fitted with a sigmoidal curve, and the value at its 50% (V_t50) was extracted as well as its sigma. The noise and gain were then obtained from a linear fit of charge versus V_t50 (Figure 5.10). The gain and input noise values obtained present good uniformity across the 2560 channels, showing abnormally higher/lower values only in 19 channels, representing less than 0.01% of the total sensor channels. In order to identify the origin of these deviations, the strips showing clear variations were inspected with a microscope. The reduction of the gain in some of the channels seems to be related with the presence of metal residues short-circuiting two or three neighbouring strips (Figure 5.11), probably associated with the presence of photoresist residues on the mask during the photolithographic step. On the other hand, some groups of channels show high noise values that are currently being investigated by the sensor experts at SCIPP.

5.3 Market Survey Evaluation of Hamamatsu Photonics K.K.

The Japanese company Hamamatsu Photonics K.K. (HPK) was the other foundry evaluated by ATLAS as a candidate to produce the new ITk strip sensors, reaching the final stage (step-3) of the Market Survey. Unlike Infineon, Hamamatsu was in charge

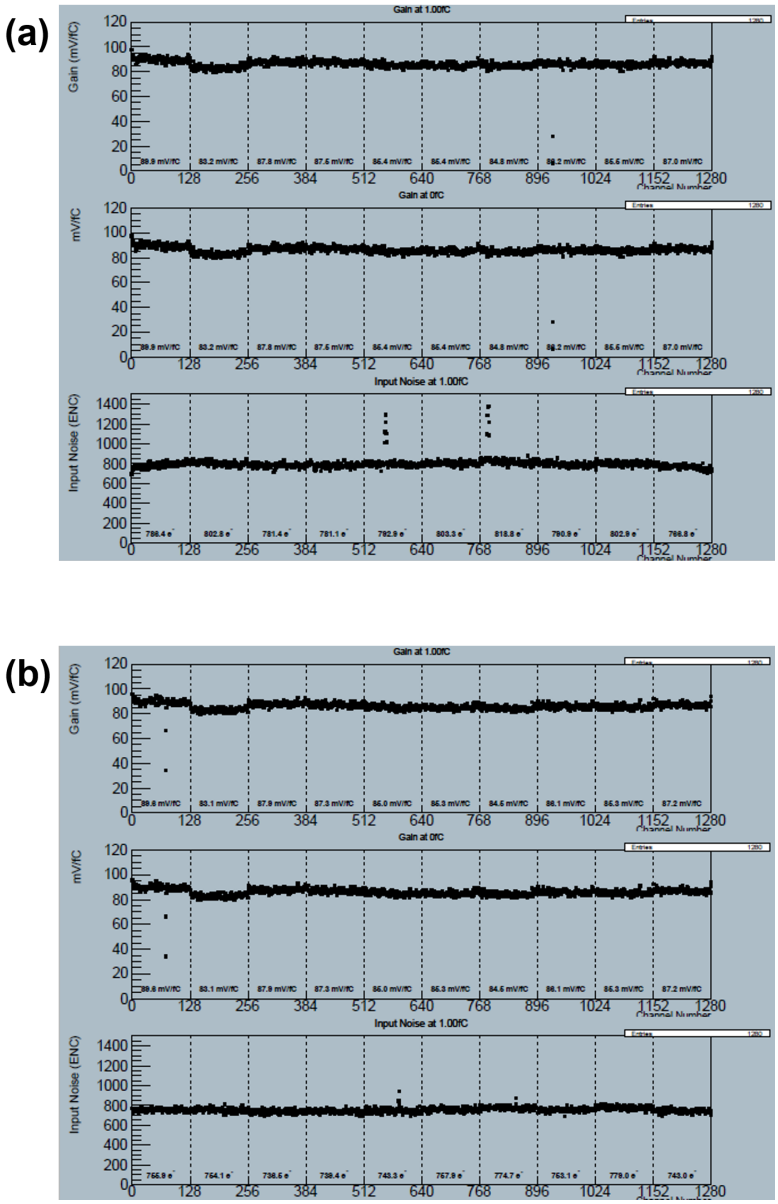


Fig. 5.10: Module noise and gain of upper (top) and lower (bottom) strip rows of an ATLAS17LS-IFX Main sensor.

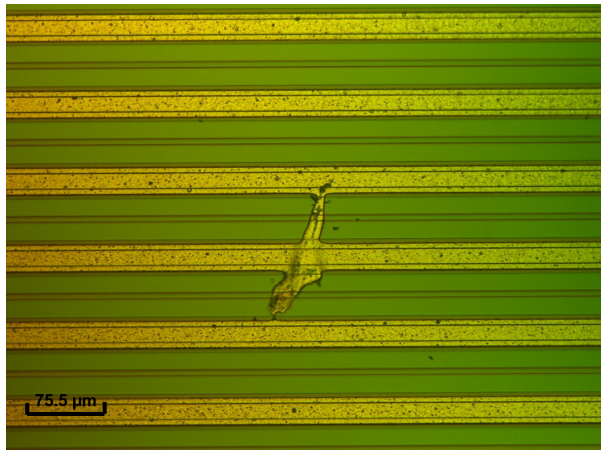


Fig. 5.11: Picture of ATLAS17LS-IFX Main sensor showing three strips shorted by the metal layer.

of his own full wafer layout design, called ATLAS17LS-HPK, following the guidelines stated in the ATLAS specifications for the Market Survey. Similarly to the Infineon prototype, each ATLAS17LS-HPK wafer contained a full-size Barrel LS sensor, eight miniature sensors (1x1 cm^2), two miniature SS sensors (2.6x1 cm^2), two miniature LS sensors (5x1 cm^2), several monitor diodes (from 1x1 to 8x8 mm^2) and several microelectronic test structures.

5.3.1 Devices Tested

Hamamatsu fabricated a batch of prototype wafers and provided to the ATLAS collaboration the different devices properly diced for their evaluation. As planned for the Market Survey step-3 stage, an extensive irradiation campaign was carried out by the collaboration, irradiating some of the devices with protons, neutrons and gammas to different fluences up to the ones expected in the future HL-LHC inner-trackers, and the irradiated devices were distributed to the different ATLAS institutes. Particularly, as part of its contribution to the Market Survey step-3, IMB-CNM received several 1x1 cm^2 miniature sensors, some of them irradiated with gammas at FZU up to 10, 35 and 70 Mrad. As part of IMB-CNM's contribution to the Market Survey step-3, a complete characterization was performed on these devices to evaluate Hamamatsu as a candidate to produce strip sensors for the ATLAS upgrade.

Similarly to the tests performed for the evaluation of Infineon, the characterization methods and parameters used to test the devices fabricated by Hamamatsu are summarized in Figure 5.1.

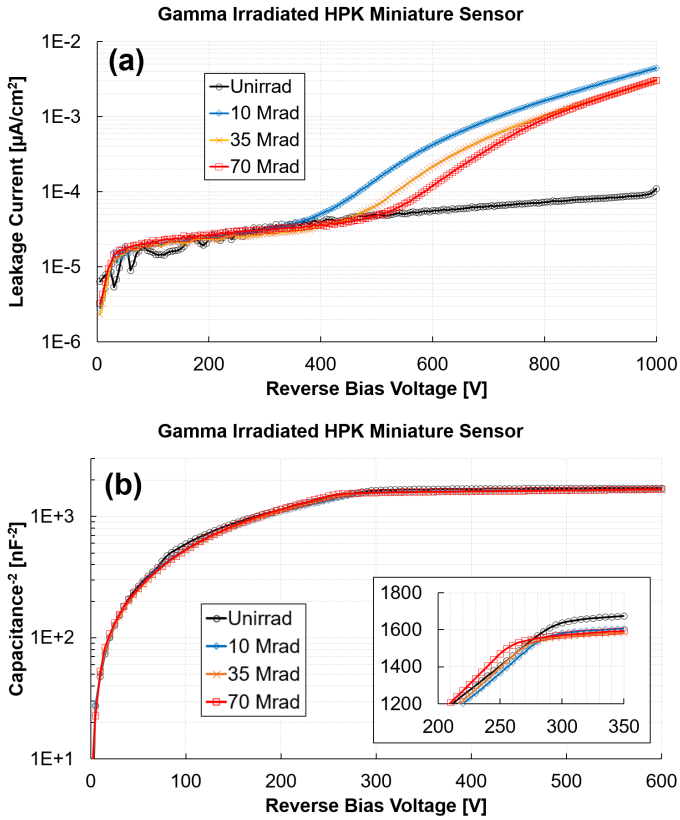


Fig. 5.12: Reverse bias leakage current (a) and bulk capacitance (b) of ATLAS17LS-HPK Miniature sensors at different gamma doses up to 70 Mrad.

5.3.2 Global Performance Evaluation

Figure 5.12(a) presents the leakage current per unit area measured in the different devices up to 1 kV bias voltage. As expected for gamma irradiations, the miniature sensors show only a low increment of the leakage current after irradiation, mainly due to an increase of the surface currents that can be associated to the creation of mid-gap energy levels in the silicon close to the SiO_2/Si interface[3]. On the other hand, Figure 5.12(b) presents the bulk capacitance measured up to 600 V, where an influence of the gamma irradiation can be observed on the full depletion voltage (V_{fd}) of the different devices (see inner plot of Figure 5.12(b)).

In particular, a progressive reduction of the full depletion voltage can be extracted from these measurements, showing no saturation even for the highest gamma dose. The effective doping concentration (N_{eff}), or the difference between acceptor-like and donor-like states, can be determined from Equation 1.7 using the full depletion voltage

[3] Surface damage produced by ionizing radiation discussed in Section 2.3.1.

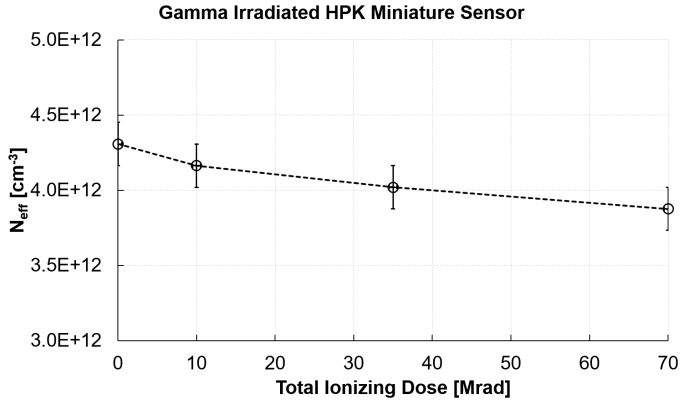


Fig. 5.13: Effective doping concentration of ATLAS17LS-HPK Miniature sensors at different gamma doses up to 70 Mrad.

obtained. Figure 5.13 presents the calculated values, showing a decrease of the N_{eff}, due to gamma irradiation. The decrease in the effective doping concentration of the substrate can be attributed to the effect of the secondary electrons with 1 MeV energy generated in the silicon bulk by the ^{60}Co gammas.

In general terms, the results obtained with the miniature sensors fabricated by Hamamatsu are in good agreement with the ATLAS specifications, that establish a maximum leakage current of 0.1 μA/cm^2 at 700 V and a maximum full depletion voltage of 300 V for the Market Survey evaluation. However, it is worth noting that devices before irradiation are close to the limit on full depletion voltage. After the Market Survey evaluation, the collaboration modified the specifications for the final ITk sensors, increasing the maximum full depletion voltage from 300 to 330 V.

5.3.3 Inter-strip Characterization

The inter-strip characterization was performed on ten strips, of the 128 strips available, uniformly distributed along the miniature sensors. Additionally, each test was performed at different bias voltages, up to 500 V, in order to evaluate the dependence of the inter-strip parameters with the sensor bias.

Figure 5.14 presents the results obtained for the inter-strip capacitance characterization. For bias voltages below 200 V, an increase of the capacitance can be observed for devices irradiated with gammas that increases with the radiation dose (Figure 5.14(a)). However, for bias voltages higher than 200 V, when most of the silicon bulk is already depleted, the inter-strip capacitance decreases to its non-irradiated value. In all cases, this parameter shows good uniformity along the miniature sensor (Figure 5.14(b)) and

values at 400 V below the maximum of 1 pF/cm (Figure 5.14(c)), established in the ATLAS specifications.

Similarly, the inter-strip resistance was measured in the same strips of each sensor, in order to evaluate the isolation between strips for the devices fabricated by Hamamatsu. Figure 5.15 shows the results obtained for this parameter. A clear influence of the gamma irradiation is observed, showing a reduction of several orders of magnitude for the highest doses (Figure 5.15(a)). The deterioration of the strip isolation, after high doses of ionizing radiation, can be associated with the generation of fixed positive charge in the SiO_2/Si interface, which induces the appearance of electron accumulation layers between neighbouring strip implants. In any case, as can be seen in Figure 5.15(b), the Hamamatsu sensors present a good uniformity across the device, remaining above the 20 MΩ lower limit established by ATLAS, even for a gamma dose of 70 Mrad (Figure 5.15(c)).

5.3.4 Single Strip Characterization

Finally, in the framework of the Market Survey, several parameters directly related to the performance of single strips were also tested to assess the most basic elements of this technology. Similarly to the inter-strip characterization, the different parameters were measured in ten strips uniformly distributed along the miniature sensors, with the aim to evaluate their variability and to average the results obtained for each device.

Figure 5.16 presents the results obtained for the coupling capacitance, between the strip implant and strip metal, showing good uniformity across the sensor, no influence of gamma irradiation and values above the ATLAS lower limit of 20 pF/cm. In the same manner, the measurements of strip implant resistance (Figure 5.17) and strip metal resistance (Figure 5.18) present values well below the ATLAS upper limits of 30 Ω/cm and 50 kΩ/cm, respectively, without remarkable variability among the strips, but showing values roughly two times higher after irradiation in the case of the strip implant measurements (Figure 5.17(b)).

On the other hand, despite the fact that the values obtained for the bias resistance are within the ATLAS range of 1.5 ± 0.5 MΩ at 400 V (Figure 5.19), and each sensor presents good homogeneity among the strips, the measured bias resistances reach values close to the upper limit, especially for intermediate doses. Fortunately, for future fabrication runs this is easily solvable as the total bias resistance can be tuned by increasing the polysilicon implantation dose to reduce the final sheet resistance of the bias resistor, as was previously discussed for the characterization of Infineon sensors.

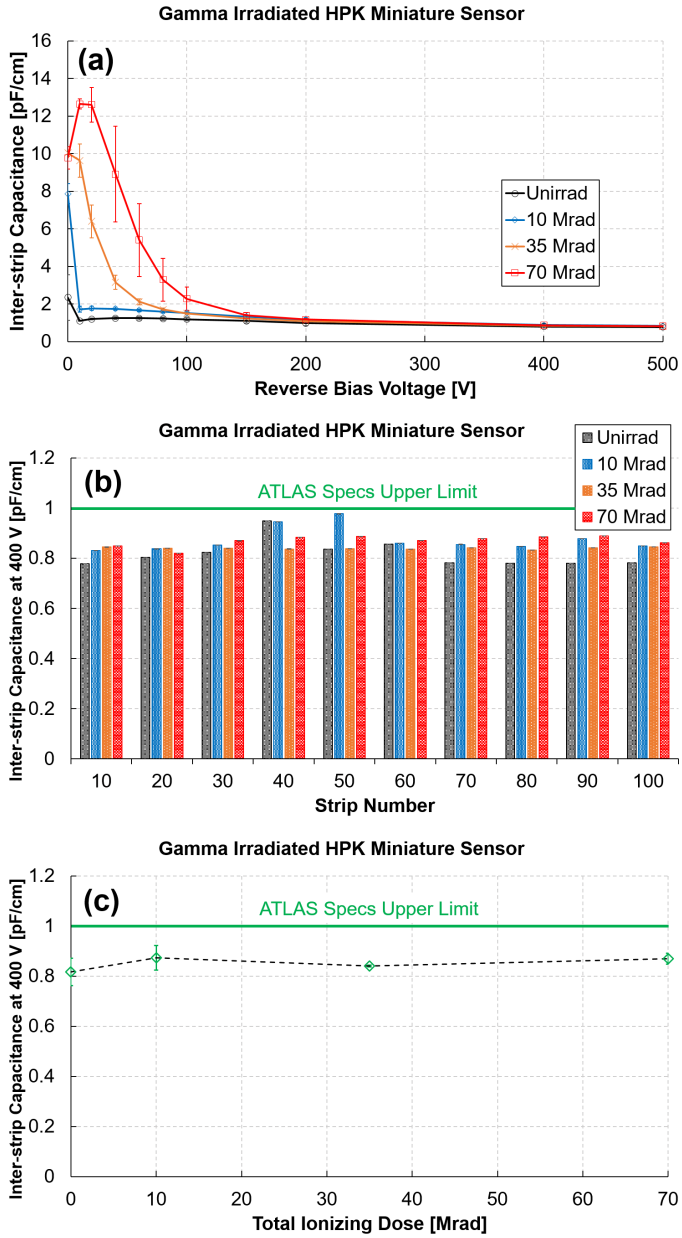


Fig. 5.14: Average inter-strip capacitance in function of bias voltage (a), values at 400 V for ten strips along the sensor (b) and average value at 400 V in function of the total ionizing dose (c) of ATLAS17LS-HPK Miniature sensors at different gamma doses up to 70 Mrad.

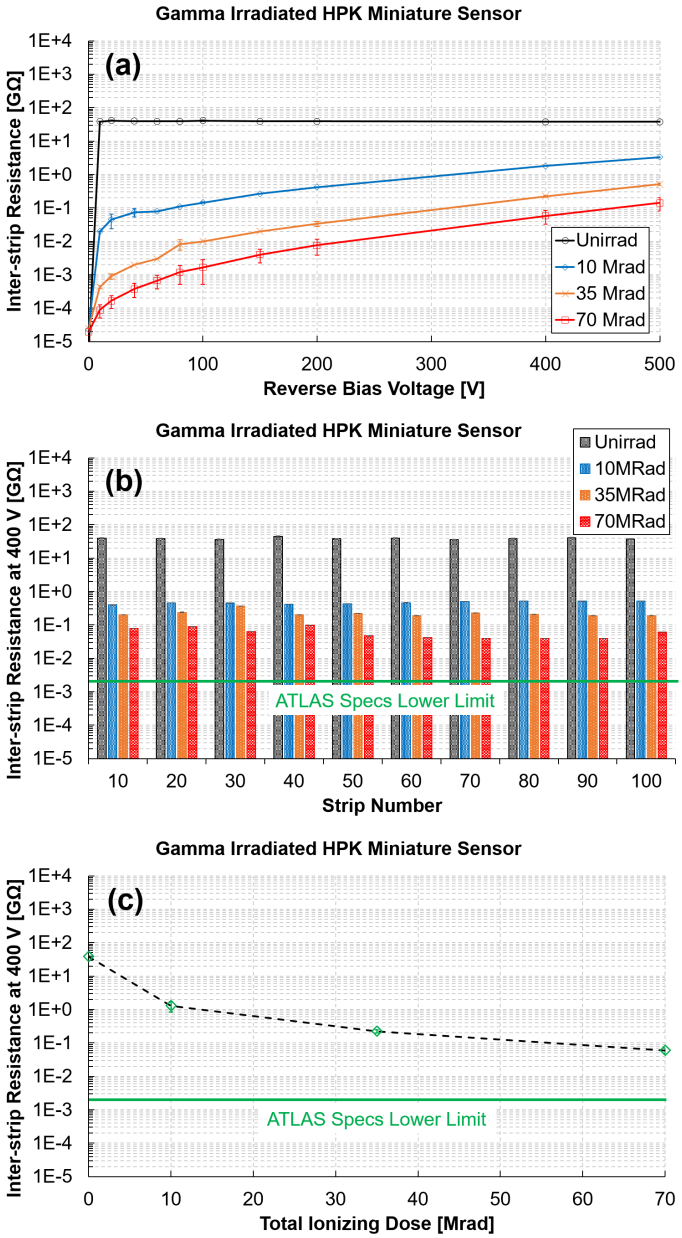


Fig. 5.15: Average inter-strip resistance in function of bias voltage (a), values at 400 V for ten strips along the sensor (b) and average value at 400 V in function of the total ionizing dose (c) of ATLAS17LS-HPK Miniature sensors at different gamma doses up to 70 Mrad.

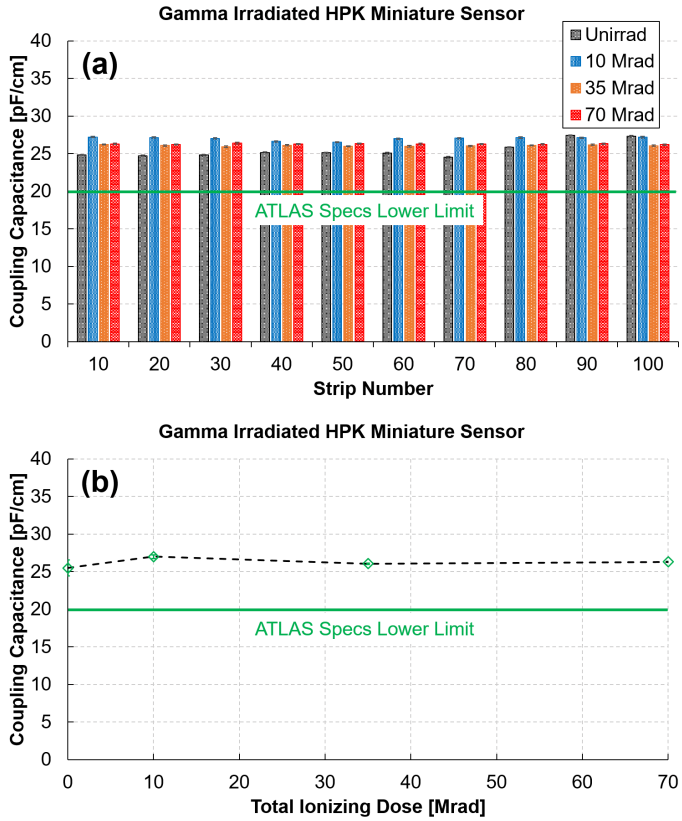


Fig. 5.16: Coupling capacitance for ten strips along the sensor (a) and average value in function of the total ionizing dose of ATLAS17LS-HPK Miniature sensors at different gamma doses up to 70 Mrad (b).

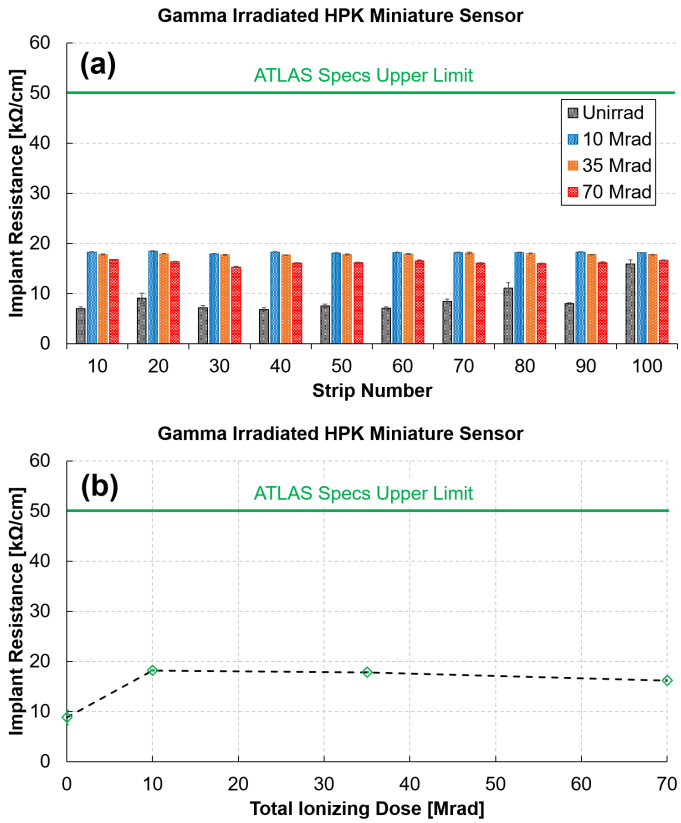


Fig. 5.17: Strip implant resistance for ten strips along the sensor (a) and average value in function of the total ionizing dose of ATLAS17LS-HPK Miniature sensors at different gamma doses up to 70 Mrad (b).

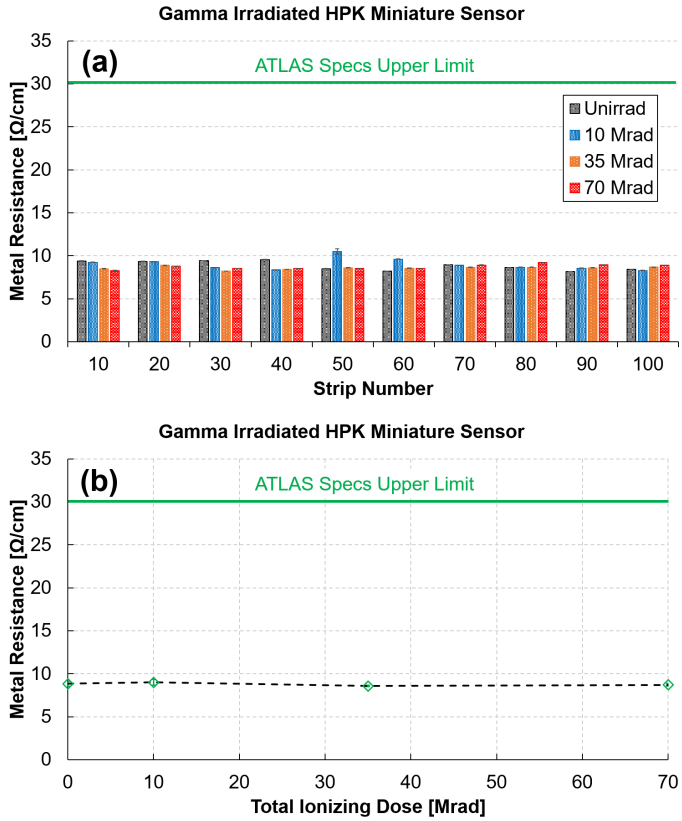


Fig. 5.18: Strip metal resistance for ten strips along the sensor (a) and average value in function of the total ionizing dose of ATLAS17LS-HPK Miniature sensors at different gamma doses up to 70 Mrad (b).

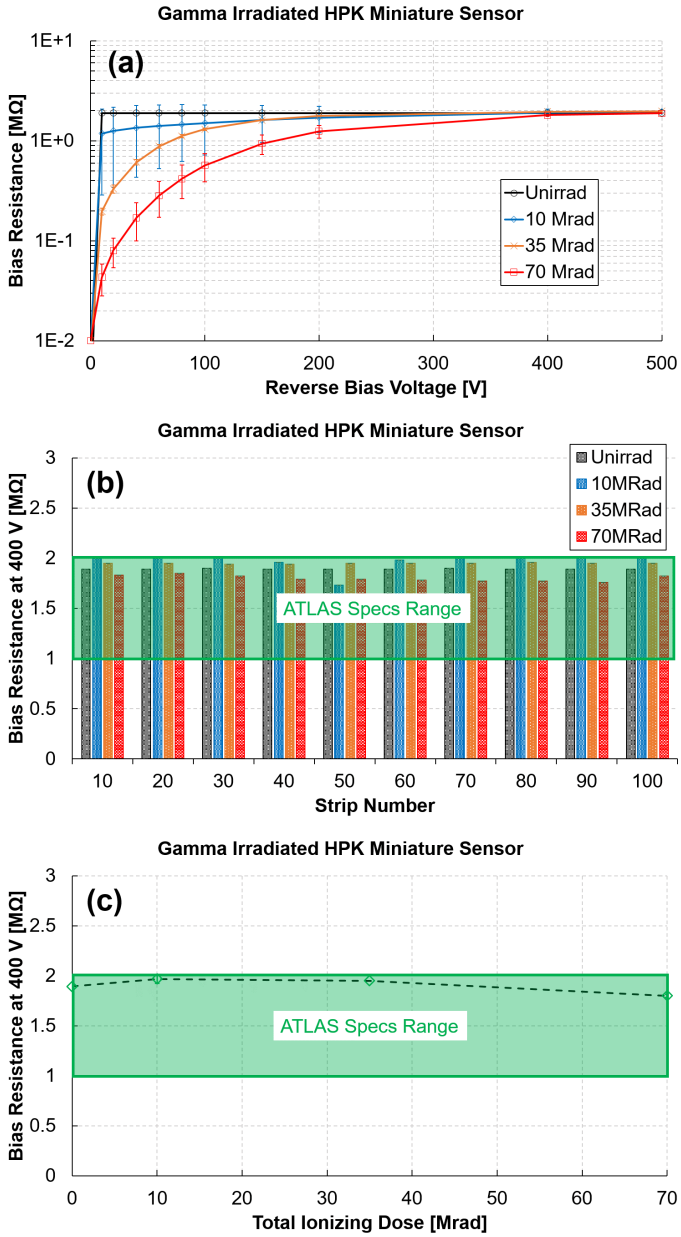


Fig. 5.19: Average bias resistance in function of bias voltage (a), values at 400 V for ten strips along the sensor (b) and average value at 400 V in function of the total ionizing dose (c) of ATLAS17LS-HPK Miniature sensors at different gamma doses up to 70 Mrad.

Finally, the punch-through protection, included in the bias side of each strip of the new ITk sensors, was also characterized to evaluate its performance before and after gamma irradiations. An IV measurement was performed between the strip implant and the bias implant (Figure 5.20(a)), with the sensor fully depleted at 400 V. Similarly to the PTP tests on Infineon sensors, Equation 2.5 was used to calculate the punch-through effective resistance and the punch-through voltage for each strip and each gamma dose (Figure 5.20(b) and (c)), showing some variability after irradiation. The punch-through voltage experiments a clear increment after a gamma dose of 10 Mrad, but recovers its value, prior to irradiation, for the highest dose.

5.4 Test Structures for Technology Development

As part of the layout design carried out for the participation of Infineon in the production Market Survey, a complete set of microelectronic test structures were designed and included in the periphery of the prototype wafer ATLAS17LS-IFX. These structures, detailed in Section 4.3.1, were conceived to study in detail the strip technology fabricated by Infineon, and to help optimize the performance of the Main sensors, but are also an example that can be used for the development of any strip sensor technology for High Energy Physics (HEP) experiments.

5.4.1 Devices Tested

Figure 5.21 shows layout images and a picture of the TestEdge, TestStrip and TestSurf structures[4], fabricated by Infineon and used in this study. In addition, well-known structures such as miniature sensors and diodes were used to complement the characterization.

In order to study the radiation hardness of the strip technology fabricated by Infineon, some of these test structures were irradiated with protons and gammas. One set of test structures was irradiated with protons at CYRIC up to $1.16{\cdot}10^{14}$, $5.06{\cdot}10^{14}$, $1.08{\cdot}10^{15}$, $2.16{\cdot}10^{15}$ and $1.01{\cdot}10^{16}$ n_{eq}/cm^2. A second set was irradiated with gammas at FZU up to 10, 17.5, 35, 52.5 and 70 Mrad. Additionally, non-irradiated test structures were tested for reference.

[4]Test structures presented in Section 4.3.1.

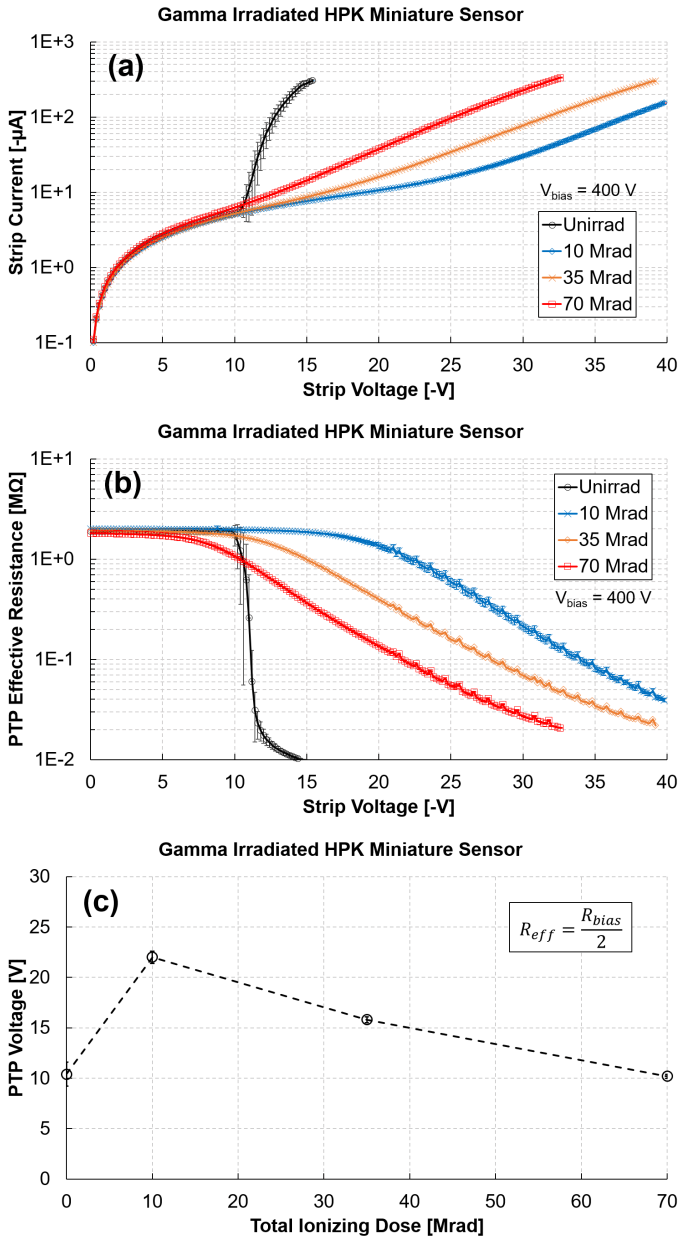


Fig. 5.20: Average strip current (a), calculated punch-through effective resistance (b) and punch-through voltage (c) at 400 V for ten strips along of ATLAS17LS-HPK Miniature sensors at different gamma doses up to 70 Mrad.

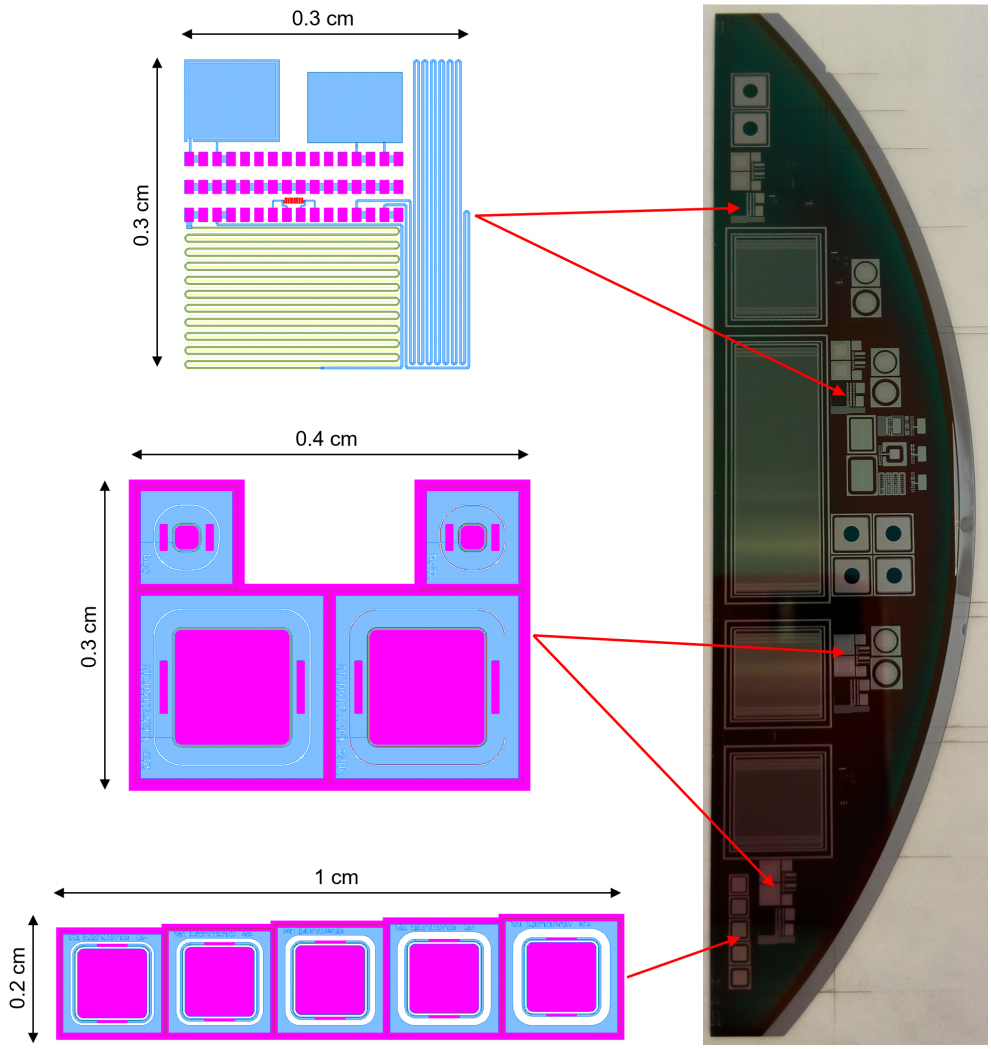


Fig. 5.21: Layout images of TestStrip (top), TestSurf (center) and TestEdge (bottom) structures characterized for the development of strip technologies, showing their position in one *half-moon* of the fabricated wafers.

5.4.2 Global Performance Evaluation

Several 8x8 mm^2 monitor diodes irradiated to different proton fluences, and 10x10 mm^2 miniature sensors irradiated with gammas, were used to test the evolution of the leakage current and full depletion voltage, respectively, basic parameters to control in order to ensure the proper performance of the final Main sensors. Similarly to the test performed for the Market Survey evaluation, the IV and CV measurements were performed using the set-up detailed in Figure 5.1). Exceptionally, for the test structures, IV and CV measurements, before and after irradiation, were performed at 20ºC, in a dry environment, in order to assess the variation in current after irradiation.

Figure 5.22 presents the leakage current of diodes irradiated with protons, up to 10^{15} n_{eq}/cm^2, showing an increase of approximately five orders of magnitude for the highest fluences and no breakdown below 1 kV. The measured increase in current is proportional to the fluence and can thus be described by Equation 2.2. Then, the proportionality factor known as current related damage rate (α) can be calculated, obtaining a value of $3.34 \cdot 10^{-17}$ A/cm, in agreement with the damage rates expected for proton irradiations in silicon detectors ([36], [37]). Additional studies of the depleted area, before and after irradiation, using diodes included in the prototype wafer fabricated by Infineon can be found in ([104], [105]).

Figure 5.23(a) shows normalized CV measurements of miniature sensors irradiated with gammas, up to 70 Mrad. The full depletion voltage is extracted from the representation of the inverse square of the capacitance versus the applied voltage. As observed for the miniature sensors fabricated by Hamamatsu (Figure 5.12), the sensors fabricated by Infineon also experiment a reduction of the full depletion voltage after gamma irradiation.

As in Section 5.3.2, the effective doping concentration can be calculated from the full depletion voltage, using Equation 1.7. Figure 5.23(b) presents the calculated values, showing a decrease of N_{eff}, due to gamma irradiation. Hence, the study of this test structure revealed a decrease in the effective doping concentration of the substrate, that could be attributed to the displacement damage produced by the secondary electrons generated during gamma irradiations. A deeper investigation is ongoing within the ATLAS ITk collaboration, using devices fabricated by different foundries, to fully understand this behaviour.

5.4.3 Sensor Edge Influence

The TestEdge structure, presented in Section 4.3.1 (see Figure 4.8), was used to evaluate the influence of the distance between the sensor physical edge and the active

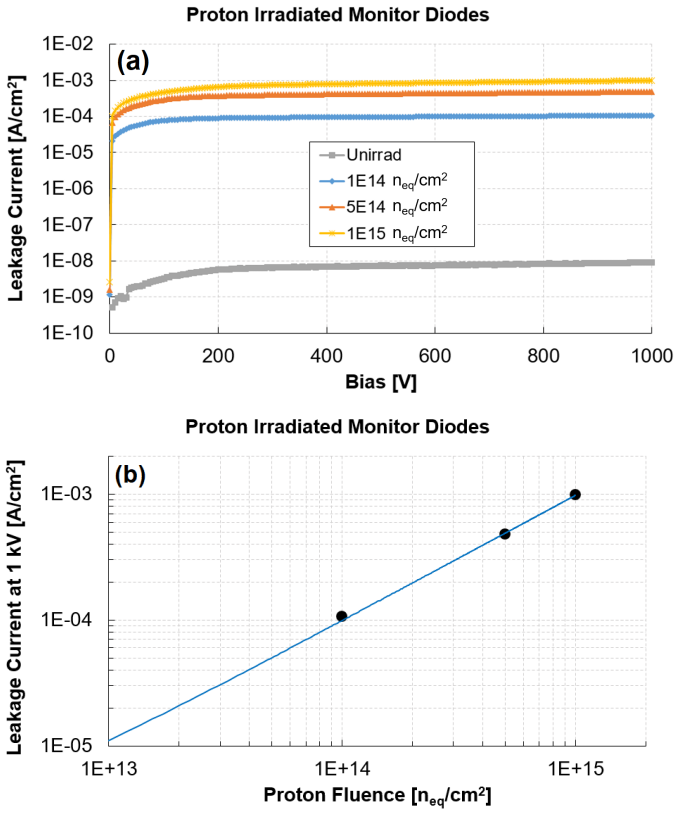


Fig. 5.22: Leakage current per unit area of monitor diodes irradiated with protons (a) and increment of leakage current at 1 kV (b).

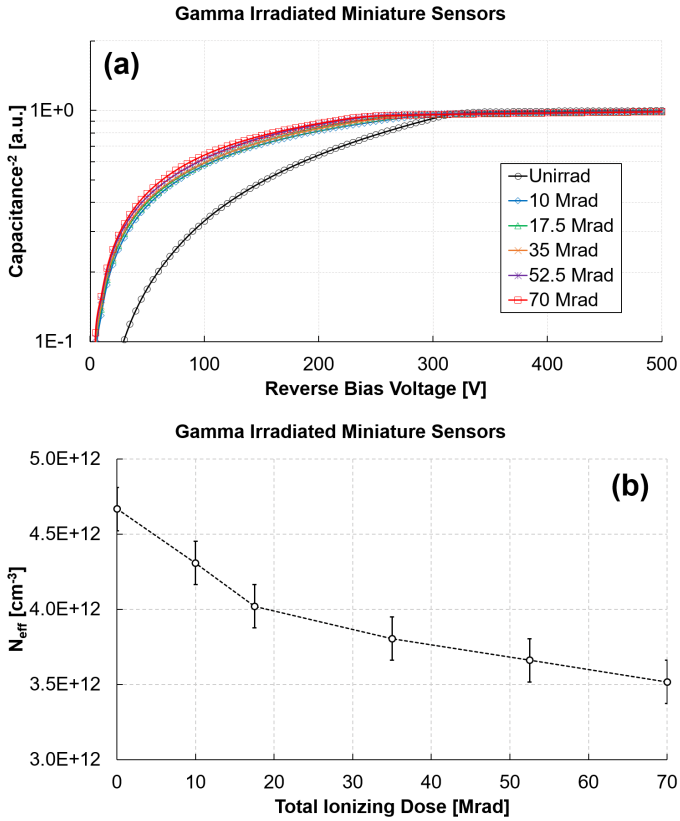


Fig. 5.23: Normalized bulk capacitance measured on gamma irradiated 10x10 mm^2 miniature sensors (a), and effective doping concentration (b) extracted from their full depletion voltage.

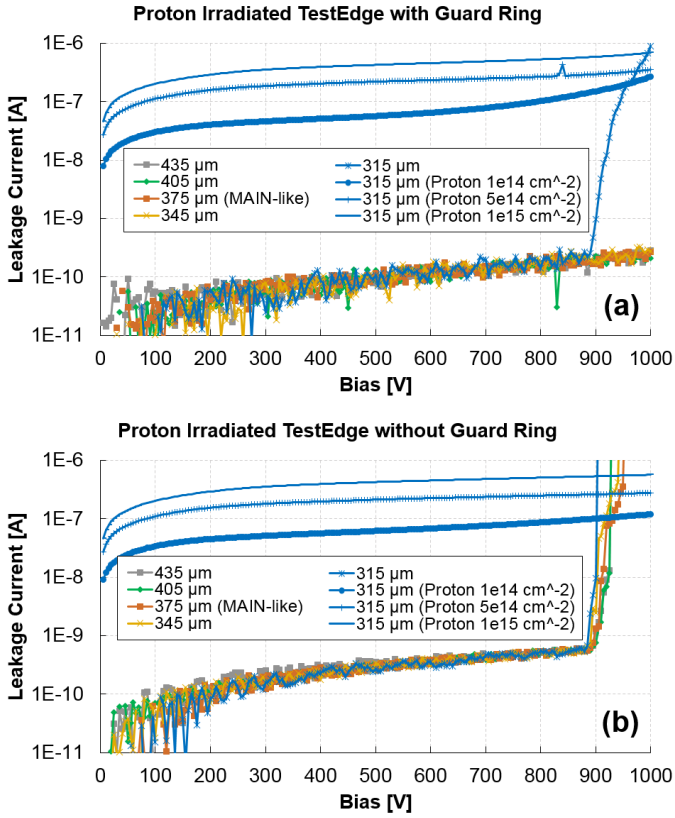


Fig. 5.24: Leakage current and breakdown voltage measured on TestEdge structures with (a) and without (b) guard ring, and comparison with proton irradiated samples.

area on the device breakdown voltage for different proton fluences, up to HL-LHC levels. In this case, all IV measurements, before and after irradiation, were performed at -20ºC in a dry environment (RH<5%) and using the IV testing method detailed in Figure 5.1(a).

Figure 5.24(a) shows the IV curves obtained for the TestEdge structure with guard ring. A lower breakdown voltage is observed in the unirradiated diode with narrower edge (315 μm). On the other hand, Figure 5.24(b) shows lower breakdown voltages in the non-irradiated diodes without guard ring, independently of the distance between the silicon edge and the active area, but showing no variations in samples irradiated with protons.

These results suggest that, in order to avoid premature breakdown voltages, the strip sensors fabricated with these particular technological options should have a distance higher than 315 μm to the silicon physical edge where a high density of defects is present. In addition, the use of a guard ring structure shapes the electric field, avoiding premature breakdown voltages. The results obtained with this test structure validate

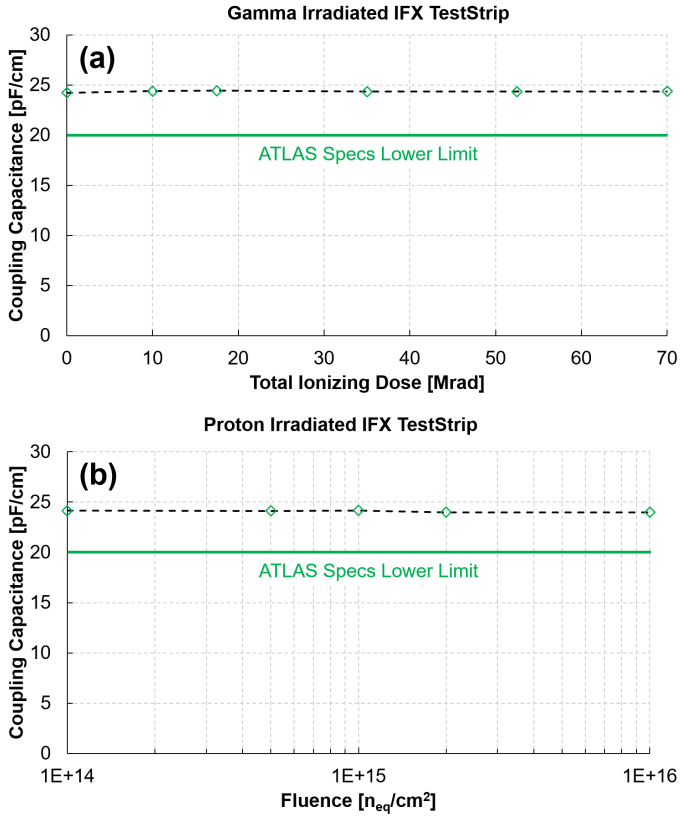


Fig. 5.25: Coupling capacitance, between strip implant and metal, measured on TestStrip structures irradiated with gammas (a) and protons (b).

the actual edge configuration of the Main sensor, with a distance of 375 μm with guard ring, revealing also the limits on the edge distance and influence of proton irradiation for the Infineon strip sensor technology.

5.4.4 Single Strip Characterization

The TestStrip structure, described in Section 4.3.1 (see Figure 4.9), was used to characterize the most important parameters associated to the performance of single strips, such as the coupling capacitance (Figure 5.25), the strip metal resistance (Figure 5.27), the strip implant resistance (Figure 5.26) and the polysilicon bias resistance (Figure 5.28), before and after proton and gamma irradiation. Resistance parameters were extracted from the inverse slope of the IV measurements, and capacitance values were measured connecting the metal and the n-implant to the AC and voltage outputs, respectively, of the LCR meter at 1 kHz with CR in parallel. All the measurements, before and after irradiation, were performed at -20°C in a dry environment.

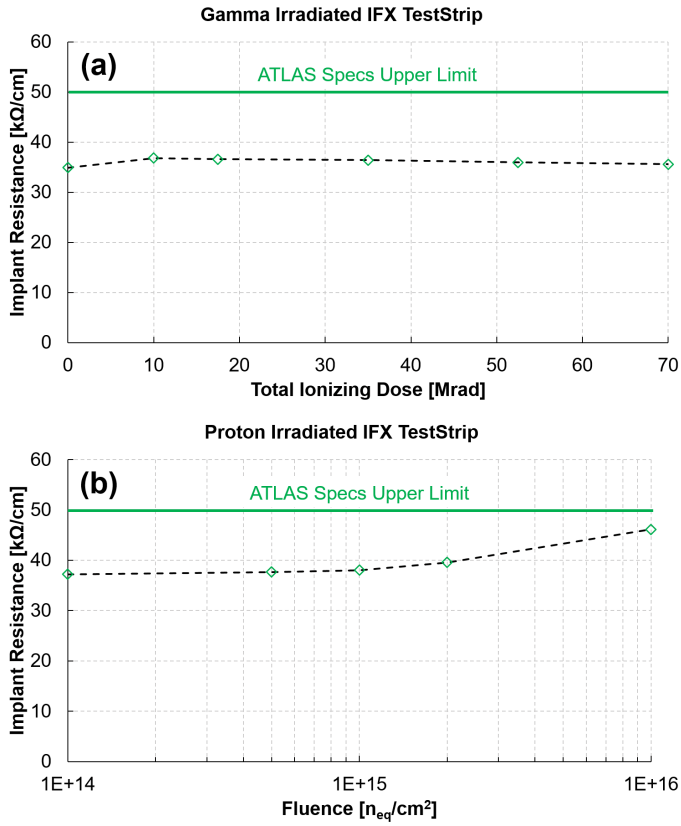


Fig. 5.26: Strip implant resistance measured on TestStrip structures irradiated with gammas (a) and protons (b).

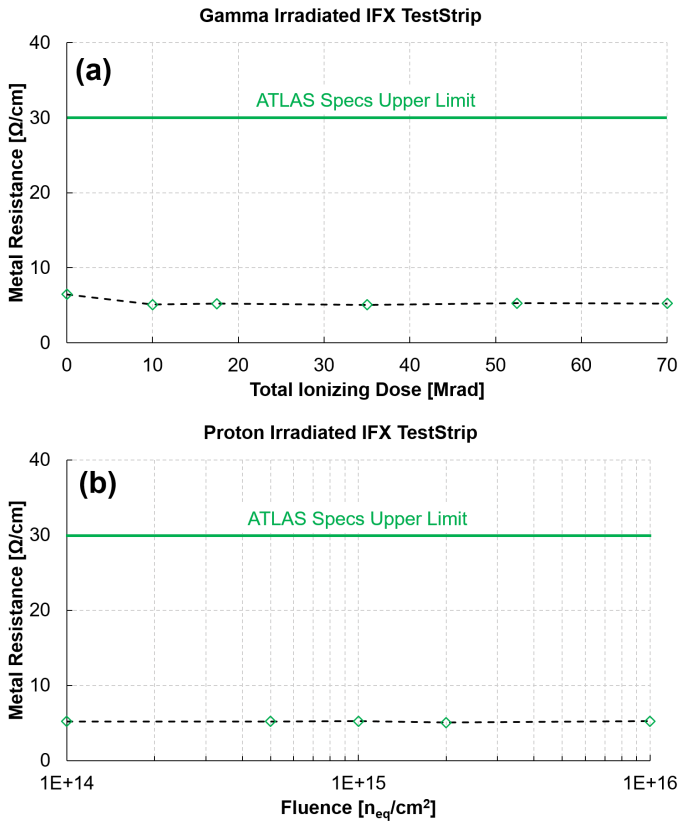


Fig. 5.27: Strip metal resistance measured on TestStrip structures irradiated with gammas (a) and protons (b).

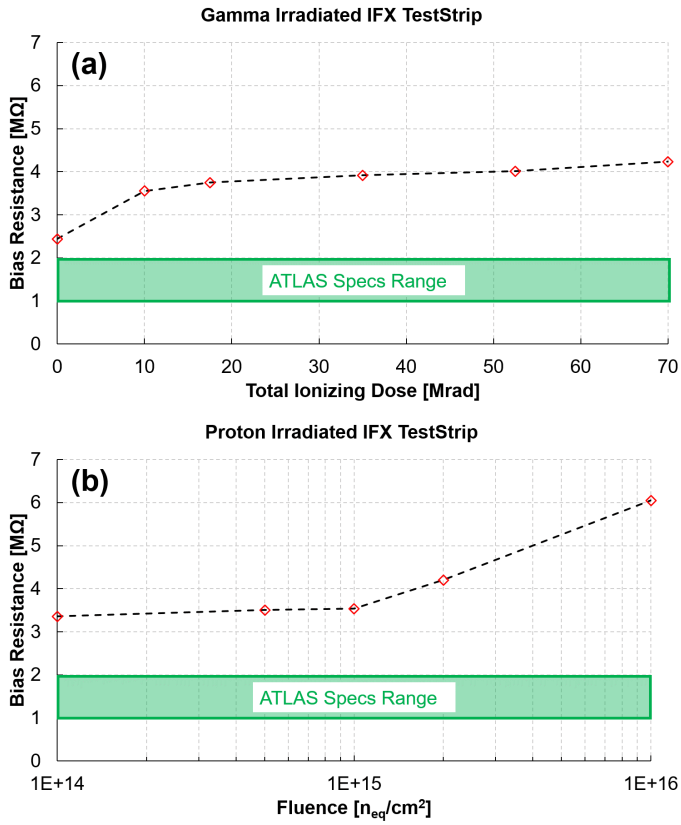


Fig. 5.28: Bias resistance measured on TestStrip structures irradiated with gammas (a) and protons (b).

All the results obtained for this test structure show negligible differences compared to the values measured directly in the Main sensor, proving the usefulness of these structures to predict the parameters associated with the Main sensor. Coupling capacitance and strip metal resistance measurements present values within the ATLAS specifications, showing no variation with gamma or proton irradiation even for the highest doses. However, although the strip implant resistance shows values below the ATLAS upper limit before and after proton irradiation (Figure 5.26(b)), it suffers a clear increase due to the de-activation of dopants in the strip implant, reaching resistance values close to the upper limit at a fluence of 10^{16} n_{eq}/cm^2.

On the other hand, the bias resistance results show a value before irradiation higher than the range established in the ATLAS specifications (Figure 5.28), as already concluded from measurements performed directly on the Main sensor (Figures 5.5(d)). This deviation becomes higher when the gamma and proton irradiation doses increase, reaching values 2.5 times higher for proton fluences of 10^{16} n_{eq}/cm^2. However, as discussed in Section 5.2.4, the high resistance value observed before irradiation can be easily tuned using longer and/or thinner polysilicon lines or with higher doping implantations. In consequence, the final sheet resistance, and total bias resistance, can be optimized and the radiation effects taken into account.

5.4.5 Field Oxide Quality

The Metal-Oxide-Semiconductor (MOS) capacitor is a well-known test structure that allows to investigate the silicon oxide and Si/SiO_2 interface quality [79], which are directly related to the fabrication processes. Particularly, in the strip sensor technology, MOS structures can provide valuable information of the field oxide (the oxide in between implants in microelectronic technologies). This oxide corresponds to the one on top of the silicon in the inter-strip areas in strip silicon detectors, previous to the deposition of the final passivation. Figure 5.29 shows CV measurements performed at 100 kHz on the MOS capacitor of the TestStrip structure (see Figure 4.9) irradiated with gammas. From measurements of the unirradiated sample in strong accumulation, we can extract a field oxide capacitance (C_{ox}) value of 53 pF. The equivalent oxide thickness (t_{ox}) can be calculated as:

$$t_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{C_{ox}} \tag{5.1}$$

where A is the area of the MOS capacitor, with a value of 0.76 mm^2. This results in a field oxide thickness of 497 nm.

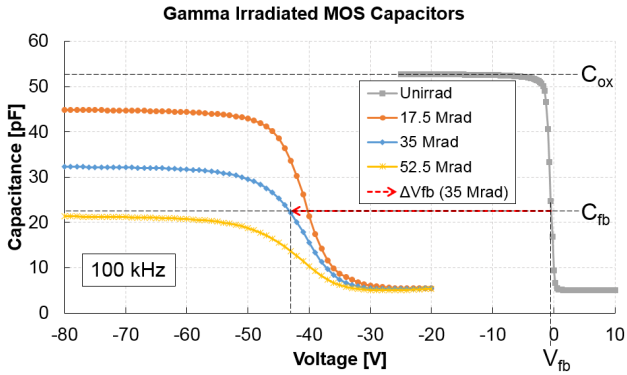


Fig. 5.29: CV measurements of the MOS capacitor included in TestStrip structure, showing the variation of flat band voltage (V_{fb}) after gamma irradiations.

The flat band voltage (V_{fb}) is the voltage corresponding to the MOS structure flat band capacitance (C_{fb}), calculated as the series of the oxide capacitance and the semiconductor capacitance in flat band condition (Cs_{fb})

$$C_{fb} = \left(\frac{1}{C_{ox}} + \frac{1}{Cs_{fb}} \right)^{-1} \tag{5.2}$$

where Cs_{fb} can be calculated as

$$Cs_{fb} = A \sqrt{\frac{e^2 \varepsilon_0 \varepsilon_{Si} N_{eff}}{k_B T}} \tag{5.3}$$

where k_B is the Boltzmann constant and T is the temperature.

From Equations 5.2 and 5.3, and using the N_{eff} previously calculated from Equation 1.7 (Figure 5.23(b)), a C_{fb} value of 23 pF is obtained for the unirradiated sample, corresponding to a V_{fb} of -0.5 V, indicating a good field oxide quality.

The energy deposited by the ionizing radiation generates electron-hole pairs in the silicon oxide of the MOS capacitor. Some of the charge carriers recombine immediately and the remaining carriers migrate to the metal or to Si/SiO_2 interface. A fraction of the holes are trapped in the oxide close to the interface resulting on a radiation-induced positive field oxide charge, as discussed in Section 2.3. In addition, interface traps are also produced with energy levels distributed throughout the silicon band gap and whose occupation depends on the gate voltage and frequency [106]. These defects induce a displacement of the flat band voltage that depends both on the total ionizing dose and on the measurement frequency of the CV curve. From the 35 Mrad gamma irradiated sample CV curve (Figure 5.29) we can estimate a flat band voltage variation

(ΔV_{fb}) of -42 V, that can be used to calculate also the variation on the oxide charge density (ΔN_{ox}) as

$$\Delta N_{ox} = \Delta V_{fb} \frac{C_{ox}}{eA} \tag{5.4}$$

which corresponds to a variation of $1.9{\cdot}10^{12}$ cm^{-2}, similar to the typical values expected for comparable oxide layers [54]. However, the appearance of a radiation-induced series resistance and other frequency-dependent defects hinder the extraction of V_{fb} for high irradiation doses [106].

5.4.6 Surface Currents

The gated diodes from the TestSurf structure (see Figure 4.10 in Section 4.3.1), exposed to gamma doses up to 70 Mrad, were used to evaluate the ionizing radiation influence on the surface recombination-generation rate. This parameter gives an indication of the expected surface currents in the Main sensor. A fixed bias voltage of 5 V is applied to the diode active area, in order to deplete the region under the n-implant. Then, a voltage sweep is applied to the diode gate, measuring the current induced in the active area of the gated diode [80].

Figure 5.30(a) shows the diode current as a function of the gate voltage for different gamma irradiation doses. Accumulation, depletion and inversion phases, originated through the evolution of the recombination-generation centres under the gate with the applied voltage, are indicated for reference in Figure 5.30(a). As explained in [107], the generation current within the depletion region of the metallurgical junction ($I_{gen,MJ}$), the generation current within the depletion region of the field-induced junction ($I_{gen,FIJ}$) and the surface generation current ($I_{gen,s}$) can be extracted from the change of current in the different phases as indicated with arrows in Figure 5.30(a). The curve for the unirradiated gated diode is also included to illustrate the low current values obtained, corresponding to a very small number of recombination-generation centres before irradiation.

The calculated $I_{gen,s}$ is represented in Figure 5.30(b), showing that the surface current is already saturated for an ionizing radiation dose of 17.5 Mrad. The plot also shows that the surface generation current is independent of the gate material (metal or polysilicon). From the curve obtained for the unirradiated gated diode (Figure 5.30(a)), a flat band voltage value of -0.5 V can be estimated. This value is estimated from the change of depletion to accumulation phases, confirming the MOS measurements before irradiation presented in the previous Section 5.4.5, and the high quality of the oxide produced by Infineon.

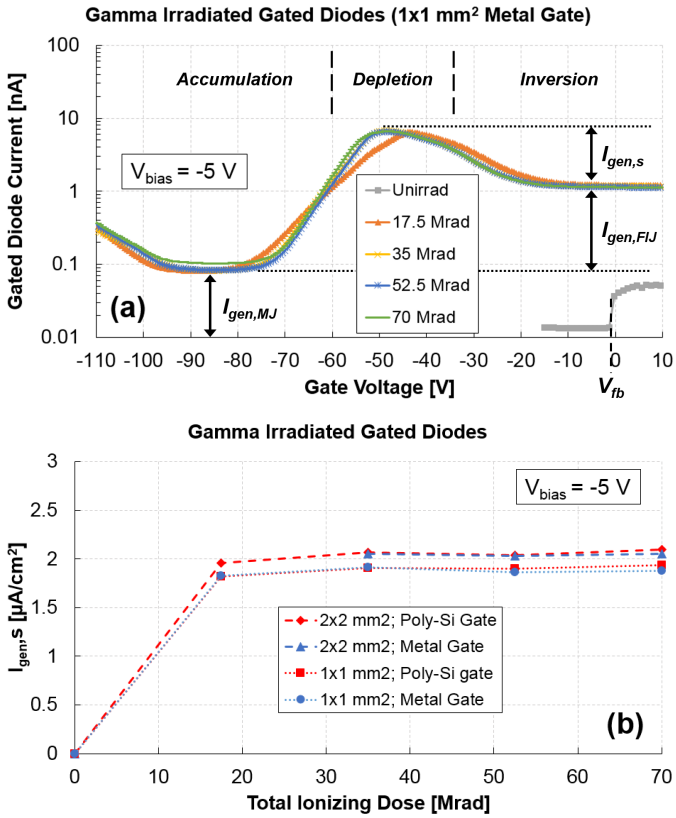


Fig. 5.30: Currents measured on 1x1 mm^2 gated diodes with metal gate (a) and calculated surface generation current ($I_{gen,s}$) for the different gated diodes included in the TestSurf structure (b).

5.5 Test Structures for Production Quality Assurance

For the last stage of the preparation of the forthcoming massive production of strip sensors for the ATLAS ITk, Hamamatsu fabricated, at the beginning of 2020, a first prototype batch using one of the final designs, the Barrel Short-Strip sensor wafer (ATLAS18SS). At this pre-production stage, the collaboration focuses on the preparation of the Quality Assurance (QA) and Quality Control (QC) programmes. Before the official production start, during the fall of 2020, the tests will be fully defined and automatized in order to carry out an efficient and exhaustive monitoring during the 5 years of sensor production.

The *QA Test Chips* designed in the framework of this thesis, and detailed in Section 4.3.2, are one of the novel devices that will be tested for the first time in the prototype batch. Additionally, miniature sensors and monitor diodes will be used to test the global performance of the Main sensors, measuring key parameters such as the leakage current or the full depletion voltage. The different test devices are arranged with the objective to reduce the dicing steps during production and to minimize the size of the silicon pieces for QA purposes, facilitating their irradiation and distribution between the different ATLAS institutes. In consequence, two different pieces will be dedicated for the QA programme, one containing a QA Test Chip and a set of Monitor Diodes, called *Testchip&MD8*, and a second one containing a 1x1 cm^2 miniature sensor and another set of monitor diodes, called *Mini&MD8*.

5.5.1 First Devices Tested

IMB-CNM received two diced Testchip&MD8 silicon pieces (Figure 5.31), one from the upper side and the second one from the lower side of the same wafer, both from one of the prototype wafers fabricated. The electrical tests presented below were done at IMB-CNM, in a shielded Cascade Summit manual probe station in a dry environment (RH<5%) at 20ºC. The objective of this first characterization is the extraction of the pre-irradiation parameters for the QA programme, along with the obtention of reference measurements to validate future automatic tests.

5.5.2 Monitor Diodes

In the QA programme established by the ATLAS collaboration, the leakage current, the breakdown voltage and the full depletion voltage of the Main sensors will be monitored using 8x8 mm^2 diodes (MD8). IV and CV measurements were performed according

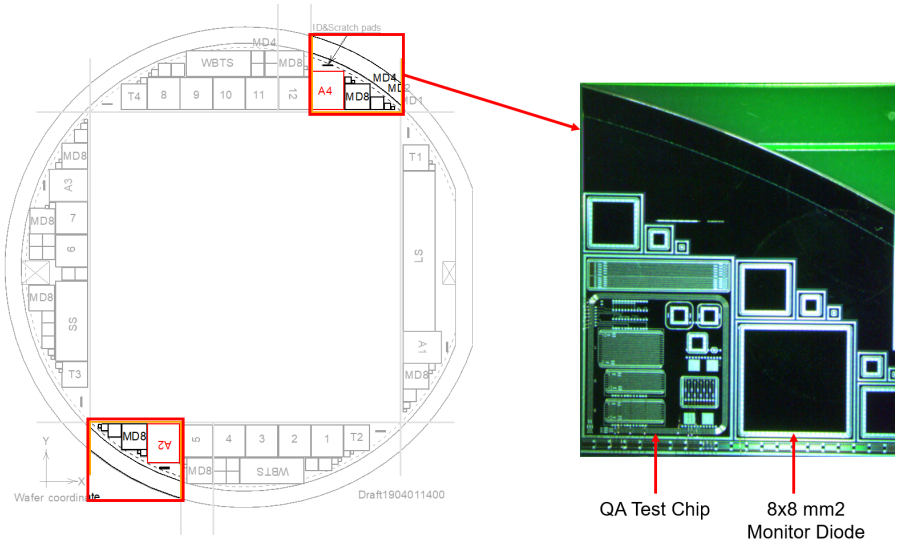


Fig. 5.31: Wafer scheme showing the silicon pieces received at IMB-CNM (left) and picture of one of the Testchip&MD8 pieces (right) to be used for the ATLAS ITk strip sensor QA programme, containing a Barrel QA Test Chip and several monitor diodes.

to the procedures described in the QA document, in this case, identical to the Market Survey testing methods described in Figure 5.1(a).

Figure 5.32(a) presents the leakage current per unit area of the monitor diodes, showing no breakdown below 700 V and a value around $2{\cdot}10^{-3}$ μA/cm^2 at 500 V, well below the 0.1 μA/cm^2 established for QA production tests. On the other hand, from the bulk capacitance measurements (Figure 5.32(b)), a full depletion voltage of 325 V can be extracted for both devices, also fulfilling the specifications for production (<330 V). Additionally, the full depletion voltage can be used to obtain an effective doping concentration of $5.4{\cdot}10^{12}$ cm^{-3}, calculated from Equation 1.7.

5.5.3 Quality Assurance Test Chip

As detailed in Section 4.3.2, the QA Test Chip contains a range of test structures that can help in the detection of possible deviations of key Main sensor parameters during production. For this first study, only some of the most relevant test structures were tested and analysed.

Interdigitated Structures:

The quality assurance of the inter-strip parameters during production will be monitored using the novel interdigitated structures. For this first study, the inter-strip capacitance and the inter-strip resistance were measured manually on the three interdigitated

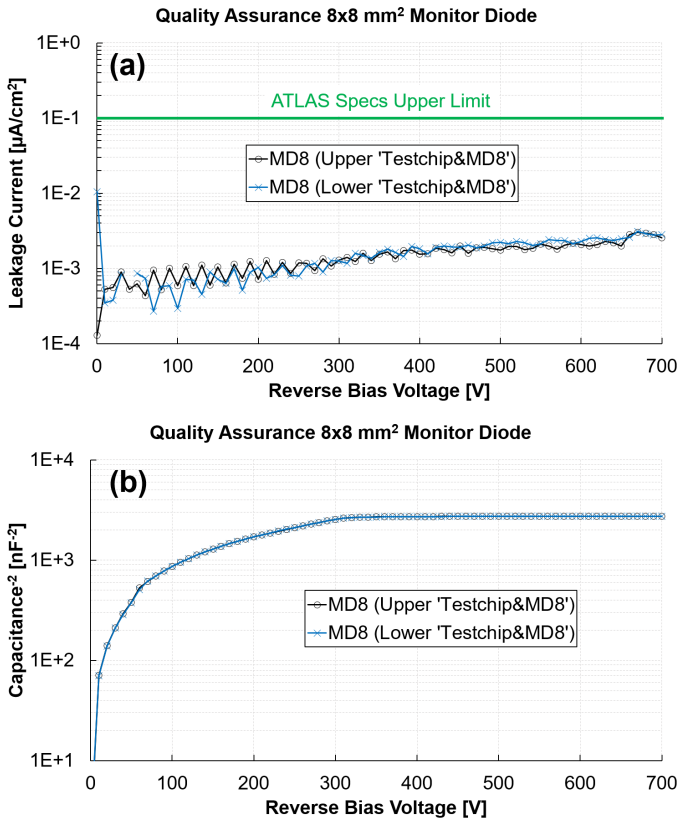


Fig. 5.32: Leakage current (a) and bulk capacitance (b) measurement of 8x8 mm^2 monitor diodes to be used for ATLAS ITk strip sensor production QA tests.

structures available, two of them corresponding to the length and pitch of the Short-strip sensor and the third one to the Long-strip sensor (Figure 4.13(b)).

For the measurements of these structures, the silicon bulk should be biased in full depletion by setting pad number 6 (bias ring), of the interdigitated structure (Figure 5.33(a)), to ground and the chip backplane to a voltage of -400 V, and to -500 V after irradiation. For the inter-strip capacitance measurement, the pad number 1 (strip line) should be contacted to the AC output of the CV meter, and pad number 10 (strip neighbour line) to the voltage output, with the CV meter sourcing 0 V. Then, the capacitance is measured using 100 kHz test frequency with circuit model set to CR in parallel.The result is divided by the strip length of the corresponding Main sensor to obtain the value of capacitance per unit length. On the other hand, for the inter-strip resistance measurement, the pad number 10 is set to ground and a sweep voltage, from 0 V to 10 V in steps of 0.1 V, is applied to pad 1 measuring the current in the same pad. Then, the inter-strip resistance is extracted from the inverse of the slope of the IV curve.

Figure 5.33(b) and (c) show the results obtained for the inter-strip capacitance and resistance, respectively. Unfortunately some of the interdigitated structures tested present an unexpected early breakdown below the 400 V backplane bias established in the QA specifications for the pre-irradiation tests. In any case, as can be seen in Figure 5.33(b) and also in the measurements done in the HPK miniature sensors in Figure 5.14, the inter-strip capacitance saturates at low voltages so its value at 150 V is very similar to the one expected at 400 V bias. The measured inter-strip capacitance value is below the limit of 1 pF/cm fixed in the QA specifications and is also in agreement with the results obtained in the HPK Miniature sensors during the Market Survey (Section 5.3.3). Similarly, the non-irradiated inter-strip resistance saturates at very low voltages as seen in Figure 5.15 so we can state that the inter-strip resistance measured with the interdigitated structures fulfils the ATLAS specifications for QA, and also presents values in accordance with previous tests performed on Hamamatsu sensors. The results obtained demonstrate the usefulness of these novel structures to evaluate the inter-strip characteristics of the Main sensor with simple tests.

Bias Resistors:

The bias resistors structure included in the test chip (Figure 5.34) will be used to monitor the polysilicon bias resistance of the Main sensor strips. The measurement procedure consists of setting pad 1 to ground, then performing an IV up to 5 V in each of the pads from 2 to 7. The bias resistance is extracted from the inverse of the slope of the IV curve for the six bias resistors.

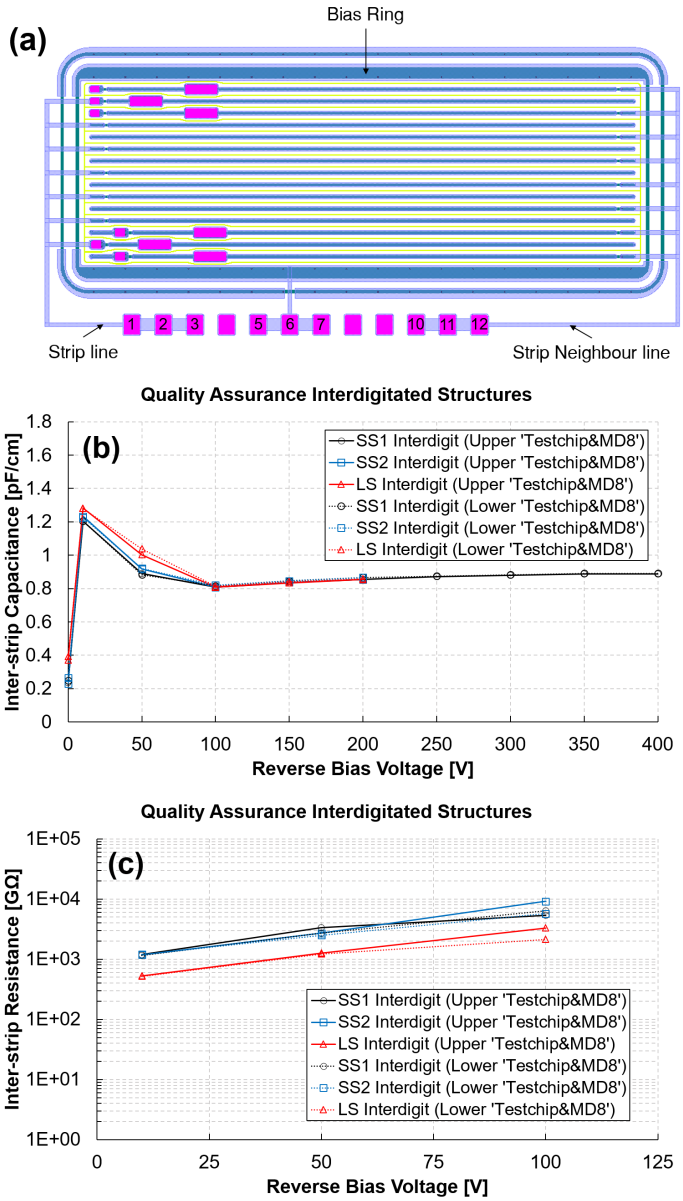


Fig. 5.33: Layout example of an interdigitated structure (a), inter-strip capacitance (b) and inter-strip resistance (c) measured in Short-strip (SS) and Long-strip (LS) interdigitated structures included in the Barrel QA Test Chip.

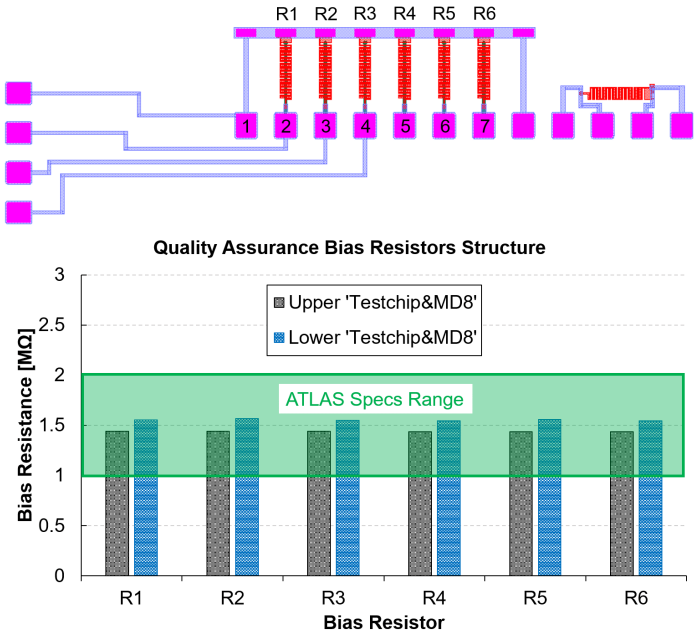


Fig. 5.34: Bias resistance measured in the polysilicon bias resistor structure included in the QA Test Chip.

Figure 5.34(b) shows the bias resistance measured in the six bias resistors of the two QA Test Chips tested. Both test chips show values within the 1.5 ± 0.5 MΩ range established for production. However, a variation of around 7% is observed between both test chips. As the QA Test Chip is replicated and distributed across the wafer, and these test chips are located in the upper and lower sides of the wafer (Figure 5.31), this deviation could be attributed to a variation of the polysilicon sheet resistance across the wafer.

Coupling Capacitor:

A square coupling capacitor, with a total area similar to the strips of the Main sensor, is also included in the test chip to monitor the coupling capacitance between the strip implant and the strip metal during QA tests.

The QA measurement procedure of the coupling capacitance using this test structure is identical to the method used during the Market Survey, testing the capacitance between the implant and the metal at 1 kHz in RC-parallel mode. The values obtained for both test chips are in agreement with the lower limit of 20 pF/cm established for production.

Metal-Oxide-Semiconductor Capacitor:

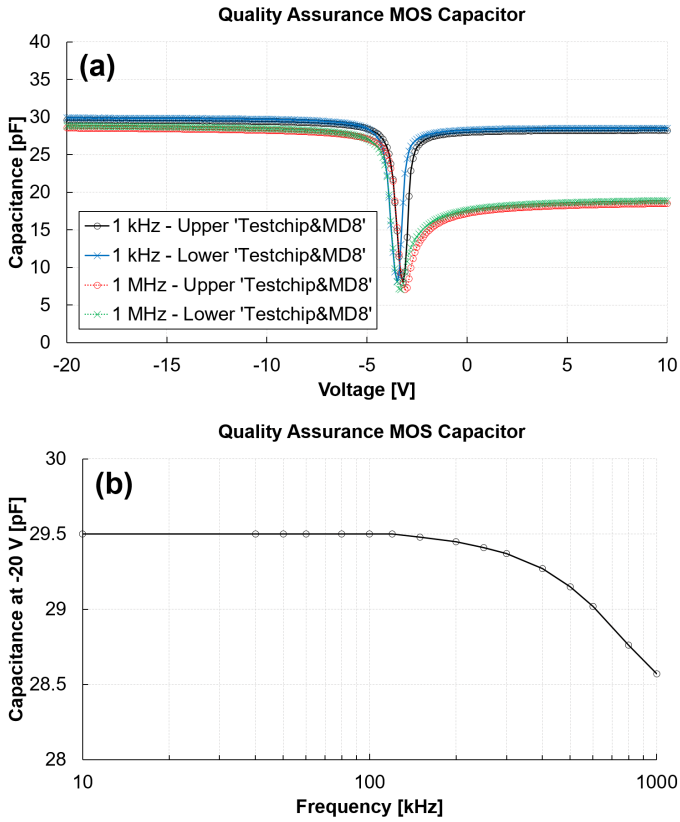


Fig. 5.35: CV measurements at different frequencies (a) and accumulation capacitance dependence with frequency at -20 V (b) of the field oxide MOS structure included in the QA Test Chip.

As detailed in Section 5.4.5, MOS structures can provide a detailed study of the field oxide used in the Main sensors with a simple CV test, obtaining parameters such as the flat band voltage, the oxide capacitance, the equivalent oxide thickness or the oxide charge density. Since the limits for each of these field oxide parameters are not defined in the QA programme at the time of writing this thesis, this study provides first reference values for the measurement of MOS structures during production.

It is well known that CV characteristics obtained with MOS structures exhibit strong frequency dependence. This frequency dependence occurs primarily in inversion (high positive voltages for a p-substrate MOS) since a certain time is needed to generate the minority carriers in the inversion layer, obtaining higher capacitance values in inversion when a low frequency is applied (quasi-static measurement). Figure 5.35 shows CV measurements of the MOS structure, included in the QA Test Chip (Figure 4.13(i)), showing a quasi-static behaviour even for high frequencies such as 1 MHz (Figure 5.35(a)). This behaviour can be associated with accumulated charge in the oxide at the vicinity of the capacitor [108].

Nevertheless, the flat band voltage and the capacitance of the field oxide are obtained from the behaviour in accumulation (low negative voltages for p-substrate MOS). In particular, the flat band voltage is associated with the transition from depletion to accumulation phases, and the oxide capacitance corresponds to the plateau value obtained in strong accumulation. Figure 5.35(b) presents the oxide capacitance measured at -20 V (strong accumulation) for different frequencies, showing a reduction for frequencies higher than 100 kHz, due to the appearance of series resistance effects. Then, any frequency below 100 kHz can be used for the study of the field oxide during production.

Figure 5.35(c) presents measurements of the MOS structures of both QA Test Chips at 1 kHz, showing a similar behaviour. A field oxide capacitance of 29.5 pF is extracted from the plateau in strong accumulation. Then, an equivalent oxide thickness of 645.7 $\pm$ 3.1 nm is obtained from Equation 5.1. Additionally, from Equations 5.2 and 5.3, and using the effective doping concentration previously calculated from the CV measurements of the monitor diodes (Section 5.5.2), a flat band capacitance of 15.7 pF, corresponding to a flat band voltage of -3.7 V.

5.6 Summary of Market Survey Evaluation and Test Structures Results

Tables 5.2 and 5.3 summarize all the results presented in this chapter, with the aim to facilitate their comparison and reference. The different parameters are divided in groups (rows), i.e. *Global Parameters*, *Inter-strip Parameters*, *Single Strip Parameters* and *Technological Parameters*, similarly to the classification used in the different sections. Table 5.2 shows the results of the characterization carried out on prototypes fabricated by Infineon and Hamamatsu, as candidates on the production Market Survey, arranged in columns. Similarly, Table 5.3 shows the results obtained from the different test structures designed, i.e. for the development of strip technologies and for the Quality Assurance during production also arranged in columns. All values, before and after maximum radiation fluence, can be compared with the specifications established by the ATLAS collaboration for the production of the strip sensors for the HL-LHC upgrade [REF], highlighting the parameters with values close to the limit (orange colour), and the ones not fulfilling the requirements (red colour). The results obtained for the Market Survey evaluation of Infineon (Section 5.2) and Hamamatsu (Section 5.3), as candidates to produce the strip sensors for the ATLAS upgrade, were presented by the collaboration on the Final Design Review (FDR) at CERN.

		ATLAS Specifications	Market Survey Prototypes	
			Infineon Barrel Long-Strip Main Sensors (Section 5.2)	*Hamamatsu 1x1 cm^2 Miniature Sensors (Section 5.3)*
Global Parameters	***Leakage Current ($\mu A/cm^2$)***	<0.1 at 700 V (Pre-irrad) <100 at 700 V (Post-irrad)	$8.92 \cdot 10^{-3}$ (Pre-irrad) 5.87 (Proton $5.1 \cdot 10^{14}$ n_{eq}/cm^2) 9.10 (Neutron $5.1 \cdot 10^{14}$ n_{eq}/cm^2)	$6.35 \cdot 10^{-5}$ (Pre-irrad) $3.69 \cdot 10^{-4}$ (Gamma 70 Mrad)
	Breakdown Voltage (V)	>700 (Pre-irrad) No Criteria (Post-irrad)	915 (Pre-irrad) >1000 (Proton $5.1 \cdot 10^{14}$ n_{eq}/cm^2) >700 (Neutron $5.1 \cdot 10^{14}$ n_{eq}/cm^2)	>1000 (Pre-irrad) >1000 (Gamma 70 Mrad)
	Full Depletion Voltage (V)	<330 (Pre-irrad) No Criteria (Post-irrad)	290 (Pre-irrad)	300 (Pre-irrad) 270 (Gamma 70 Mrad)
Inter-strip Parameters	***Inter-strip Capacitance (pF/cm)***	<1 at 300 V (Pre-irrad) <1 at 400 V (Post-irrad)	0.81 at 400 V (Pre-irrad) 0.82 at 400 V (Proton $5.1 \cdot 10^{14}$ n_{eq}/cm^2) 0.82 at 400 V (Neutron $5.1 \cdot 10^{14}$ n_{eq}/cm^2)	0.81 at 400 V (Pre-irrad) 0.88 at 400 V (Gamma 70 Mrad)
	Inter-strip Resistance (GΩ)	$>1.5 \cdot 10^{-2}$ at 300 V (Pre-irrad) $>1.5 \cdot 10^{-2}$ at 400 V (Post-irrad)	122.20 at 300 V (Pre-irrad) 0.02 at 400 V (Proton $5.1 \cdot 10^{14}$ n_{eq}/cm^2) 0.64 at 400 V (Neutron $5.1 \cdot 10^{14}$ n_{eq}/cm^2)	38.15 at 400 V (Pre-irrad) 0.06 at 400 V (Gamma 70 Mrad)
Single Strip Parameters	***Coupling Capacitance (pF/cm)***	≥ 20 (Pre-irrad) No Criteria (Post-irrad)	29.09 (Pre-irrad) 28.50 (Proton $5.1 \cdot 10^{14}$ n_{eq}/cm^2) 29.82 (Neutron $5.1 \cdot 10^{14}$ n_{eq}/cm^2)	25.49 (Pre-irrad) 26.29 (Gamma 70 Mrad)
	Strip Implant Resistance (kΩ/cm)	<50 (Pre-irrad) No Criteria (Post-irrad)	35.77 (Pre-irrad) 32.90 (Proton $5.1 \cdot 10^{14}$ n_{eq}/cm^2) 35.85 (Neutron $5.1 \cdot 10^{14}$ n_{eq}/cm^2)	8.80 (Pre-irrad) 16.20 (Gamma 70 Mrad)
	Strip Metal Resistance (Ω/cm)	<30 (Pre-irrad) No Criteria (Post-irrad)	10.61 (Pre-irrad) 7.69 (Proton $5.1 \cdot 10^{14}$ n_{eq}/cm^2) 17.97 (Neutron $5.1 \cdot 10^{14}$ n_{eq}/cm^2)	8.84 (Pre-irrad) 8.71 (Gamma 70 Mrad)
	Bias Resistance (MΩ)	1.5 ± 0.5 (Pre-irrad) 1.5 ± 0.5 (Post-irrad)	3.06 (Pre-irrad) 2.45 (Proton $5.1 \cdot 10^{14}$ n_{eq}/cm^2) 3.03 (Neutron $5.1 \cdot 10^{14}$ n_{eq}/cm^2)	1.89 (Pre-irrad) 1.80 (Gamma 70 Mrad)
	Punch-through Voltage (V)	No Criteria	-7.40 (Pre-irrad) -18.40 (Proton $5.1 \cdot 10^{14}$ n_{eq}/cm^2) -30.60 (Neutron $5.1 \cdot 10^{14}$ n_{eq}/cm^2)	-10.60 (Pre-irrad) -10.80 (Gamma 70 Mrad)

Tab. 5.2: Summary of the results obtained on the evaluation of Infineon and Hamamatsu for the ATLAS ITk strip sensor Market Survey. Characterization performed at 20°C before irradiation, and at -20°C after irradiation. Results before irradiation, and at maximum fluence, are compared with the ATLAS specifications for production (ATLAS18 designs), highlighting the parameters that are out of specifications (red).

		ATLAS Specifications	Test Structures: *Infineon Technology Development (Section 5.4)*	Test Structures: *Hamamatsu Production Quality Assurance (Section 5.5)*
Global Parameters	***Leakage Current*** ***($\mu A/cm^2$)***	<0.1 at 700 V (Pre-irrad) <100 at 700 V (Post-irrad)	$8.02 \cdot 10^{-3}$ (Pre-irrad) 16.15 (Proton $1.2 \cdot 10^{15}$ n_{eq}/cm^2) 0.36 (Gamma 70 Mrad)	$2.59 \cdot 10^{-3}$ (Pre-irrad)
	Breakdown Voltage ***(V)***	>700 (Pre-irrad) No Criteria (Post-irrad)	>1000 (Pre-irrad) >1000 (Proton $1.2 \cdot 10^{15}$ n_{eq}/cm^2) >1000 (Gamma 70 Mrad)	>1000 (Pre-irrad)
	Full Depletion Voltage ***(V)***	<330 (Pre-irrad) No Criteria (Post-irrad)	310 (Pre-irrad) 250 (Gamma 70 Mrad)	325 (Pre-irrad)
Inter-strip Parameters	***Inter-strip Capacitance*** ***(pF/cm)***	<1 at 300 V (Pre-irrad) <1 at 400 V (Post-irrad)	-	Short-Strip: 0.86 at 200 V (Pre-irrad) Long-Strip: 0.86 at 200 V (Pre-irrad)
	Inter-strip Resistance ***(GΩ)***	$>1.5 \cdot 10^{-2}$ at 300 V (Pre-irrad) $>1.5 \cdot 10^{-2}$ at 400 V (Post-irrad)	-	Short-Strip: $6.66 \cdot 10^{3}$ at 100 V (Pre-irrad) Long-Strip: $1.74 \cdot 10^{3}$ at 100 V (Pre-irrad)
Single Strip Parameters	***Coupling Capacitance*** ***(pF/cm)***	$\geq$ 20 (Pre-irrad) No Criteria (Post-irrad)	24.23 (Pre-irrad) 23.98 (Proton 1e16 neq/cm2) 24.35 (Gamma 70 Mrad)	22.59 (Pre-irrad)
	Strip Implant Resistance ***(kΩ/cm)***	<50 (Pre-irrad) No Criteria (Post-irrad)	34.91 (Pre-irrad) 46.12 (Proton $1 \cdot 10^{16}$ n_{eq}/cm^2) 35.60 (Gamma 70 Mrad)	-
	Strip Metal Resistance ***(Ω/cm)***	<30 (Pre-irrad) No Criteria (Post-irrad)	6.45 (Pre-irrad) 5.25 (Proton $1 \cdot 10^{16}$ n_{eq}/cm^2) 5.25 (Gamma 70 Mrad)	-
	Bias Resistance ***(MΩ)***	1.5 ± 0.5 (Pre-irrad) 1.5 ± 0.5 (Post-irrad)	2.44 (Pre-irrad) 6.05 (Proton $1 \cdot 10^{16}$ n_{eq}/cm^2) 4.23 (Gamma 70 Mrad)	1.49 (Pre-irrad)
	Punch-through Voltage ***(V)***	No Criteria	-	-
Technological Parameters	***Effective Doping Concentration*** ***(cm^{-3})***	No Criteria	$4.13 \cdot 10^{12}$ (Pre-irrad) $3.41 \cdot 10^{12}$ (Gamma 70 Mrad)	$5.39 \cdot 10^{12}$ (Pre-irrad)
	Field Oxide Capacitance ***(pF/cm^2)***	No Criteria	$6.94 \cdot 10^{3}$ (Pre-irrad)	$5.35 \cdot 10^{3}$ (Pre-irrad)
	(Equivalent) Field Oxide Thickness ***(nm)***	No Criteria	497.16 (Pre-irrad)	645.72 (Pre-irrad)
	Flat Band Capacitance ***(pF/cm^2)***	No Criteria	$2.97 \cdot 10^{3}$ (Pre-irrad)	$2.81 \cdot 10^{3}$ (Pre-irrad)
	Flat Band Voltage ***(V)***	No Criteria	-0.44 (Pre-irrad)	-3.66 (Pre-irrad)
	Surface Generation Current ***($\mu A/cm^2$)***	No Criteria	$8.95 \cdot 10^{-4}$ (Pre-irrad) 2.10 (Gamma 70 Mrad)	-

Tab. 5.3: Summary of the results obtained on the characterization of microelectronic test structures for technology development and first measurements of test structures for production Quality Assurance. Characterization performed at 20°C before irradiation, and at -20°C after irradiation. Results before irradiation, and at maximum fluence, are compared with the ATLAS specifications for production (ATLAS18 designs), highlighting the parameters that are close to the limit (orange) and the ones that are out of specifications (red).

6

Additional Studies and Developments for Advanced Silicon Strip Detectors

This chapter presents several additional studies carried out during this PhD thesis for the development of new large area strip sensors. In contrast to the results shown in the previous chapter, focused on the evaluation of the new ATLAS Inner-Tracker (ITk) strip sensors, the investigations presented here were developed with the objective to improve the performance of the devices, and, in general, can be applied to strip sensor technologies, not only for the ATLAS experiment.

Section 6.1 presents a complete study of the device breakdown voltage degradation observed in large area strip sensors in the presence of high humidity. Several observations and dedicated studies are presented, introducing hypotheses for the mechanisms responsible for the sensitivity and deducing implications that should be taken into account during the production, assembly and operation of large area strip sensors. Next, Section 6.2 presents a study of the damage that can be induced in strip sensors by an accidental beam-loss in the forthcoming High-Luminosity Large Hadron Collider (HL-LHC). The experiment is focused on the effectiveness of the Punch-Through Protection (PTP) included in the new ITk strip sensors, and extracts conclusions on the effects that can be produced in the strip coupling capacitance and readout ASICs. On the other hand, the different designs of Embedded Pitch Adapters (EPAs), introduced in Chapter 4 to improve the sensor-readout inter-connection in strips with variable pitch, are investigated in Section 6.3. Five different EPA structures are evaluated with the aim to find the optimal design and technology in order to minimize the introduction of undesired effects in the sensor performance, such as the increase of the module noise or the loss of efficiency due to signal pick-up/cross-talk by the EPA structures. Finally, Section 6.4 presents a complete characterization of the first strip sensors fabricated at Centro Nacional de Microelectrónica (IMB-CNM) in 6-inch wafers with the future objective to develop the technology to fabricate large area strip sensors at the cleanroom of the institute.

6.1 Humidity Sensitivity of Large Area Silicon Sensors

This section presents the findings of the ATLAS ITk strip sensor community, for sensor prototypes fabricated by Hamamatsu Photonics K.K. [74] and Infineon Technologies AG [73], investigating the mechanisms and evaluating the incidence and implications of the humidity sensitivity in the ATLAS strip sensor production in particular, and in large area silicon sensors in general [109].

6.1.1 Humidity Sensitivity Observations

Breakdown Voltage Dependence:

Measurements on early prototypes of the new large area silicon strip sensors for ATLAS, assembled in modules [110], showed first indications of breakdown voltage (V_{bd}) dependence on relative humidity (RH). Current vs. voltage (IV) measurements made on bare ATLAS End-Cap (ATLAS12EC) and Barrel (ATLAS17LS) large area strip sensor prototypes, fabricated by Hamamatsu [68] and Infineon [70], confirmed the relative humidity influence on the sensor's breakdown behaviour. Figure 6.1 presents two examples of progressive breakdown voltage reduction when the relative humidity increases. Sensors showing good performance at low humidity values (<5%), without breakdown below 1 kV, show a clear deterioration of their performance when the relative humidity reaches values around 50%, inducing breakdown voltages well below the minimum of 700 V established in the ATLAS specifications for the ITk strip sensors (see Table 5.1).

Miniature strip sensors of different dimensions, from 1x1 cm^2 to 5x1 cm^2 (die area), were also tested to evaluate the influence of humidity in smaller devices. Figure 6.2 presents the leakage current of three different miniature sensors, showing a clear reduction of the breakdown voltage at 50% RH, similarly to the results obtained for the large area sensors. However, a smaller fraction of the miniature sensors showed a clear dependence on humidity variations than large sensors, revealing less incidence of humidity sensitivity on smaller devices.

Leakage Current Stability:

The stability of the sensor leakage current is also one of the main characteristics to be controlled to ensure the proper performance of the devices during the lifetime of High Energy Physics (HEP) experiments. Even assuming that the sensors in the HL-LHC detectors will be working in dry conditions, the devices will be exposed to different

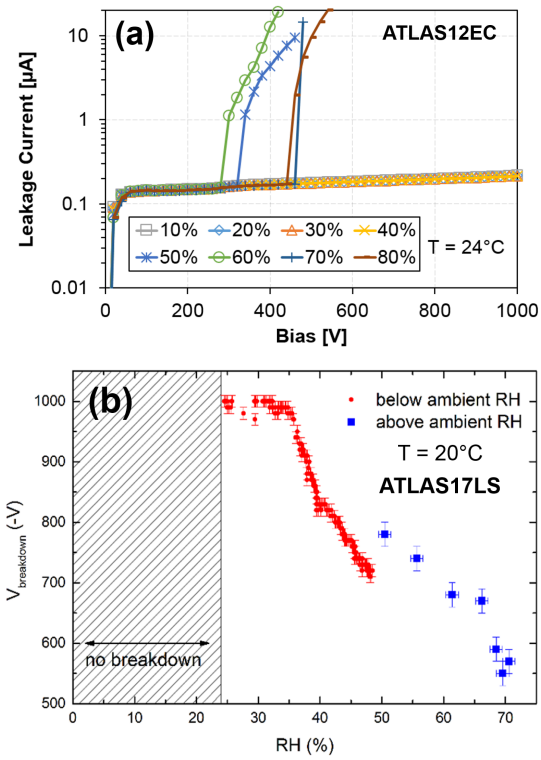


Fig. 6.1: (a) Reverse leakage current of an End-cap R0 large area prototype (ATLAS12EC) at different humidity conditions, and (b) breakdown voltage dependence with humidity of a Barrel Long-strip prototype (ATLAS17LS).

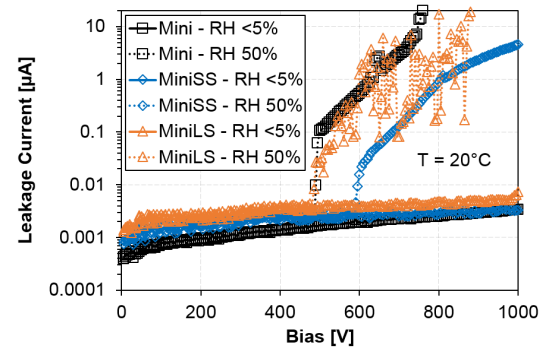


Fig. 6.2: Reverse leakage current of miniature sensors with a die area of 1x1 cm^2 (Mini), 2.6x1 cm^2 (MiniSS) and 5x1 cm^2 (MiniLS) at different humidity conditions.

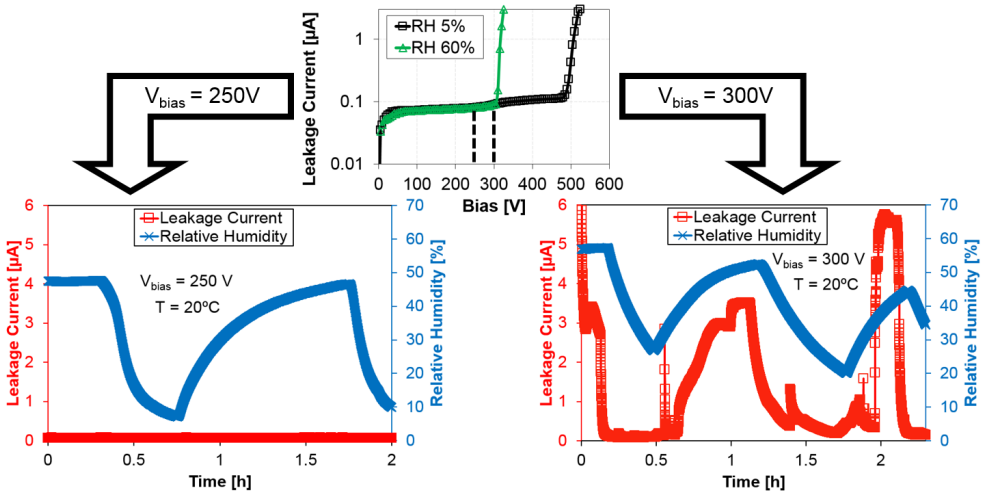


Fig. 6.3: Variability of leakage current for a sensor biased near the breakdown voltage at high humidity.

humidity levels during the sensor Quality Control (QC), module assembly, detector installation and maintenance.

The upper plot in Figure 6.3 shows the leakage current of a large area ATLAS17LS sensor, with breakdown voltages around 500 V and 300 V for low and high humidity, respectively. Applying a fixed bias of 250 V (bottom left plot in Figure 6.3), the sensor shows a stable baseline current while the RH varies from 10 to 50%. However, for a fixed bias of 300 V (bottom right plot in Figure 6.3) the leakage current quickly responds to RH variations, due to the proximity of the applied bias to the breakdown voltage at high humidity ($V_{bias} \approx V_{bd} \approx 300$ V).

Dry Storage and Baking Effects:

A large area ATLAS17LS sensor, which showed a premature breakdown voltage at low humidity, decreasing by 150 V at 50% RH, was used to evaluate the effect of prolonged exposure to dry environment. After several measurements at 50% RH, the sensor was kept in dry storage for 2 hours, with RH below 5%. The sensor fully recovered the breakdown voltage prior to the high humidity tests (Figure 6.4).

Next, the sensor was baked at 150ºC for 24 hours with low humidity. Figure 6.4 shows a significant recovery of the breakdown voltage at low RH (from 420 V to more than 1 kV). However, the performance at high humidity remains unchanged, showing no influence of the baking process on the humidity sensitivity of the device. On the other hand, the baseline leakage current improved after the baking treatment, showing a reduction of 23 nA (37% less) in this case, under both low and high humidity conditions.

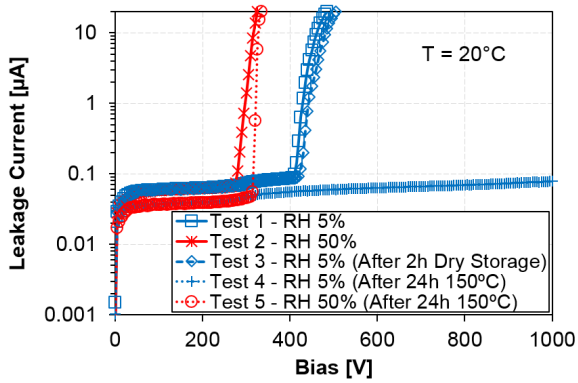


Fig. 6.4: Influence of dry storage (dashed line) and baking (dotted lines) on humidity sensitivity of a large area strip sensor.

6.1.2 Detailed Studies of Humidity Effects

Time-dependent Degradation under Humidity Exposure:

In order to study in detail the progressive degradation of the breakdown voltage, an experimental study was carried out exposing a large area ATLAS17LS sensor to a high humidity atmosphere, measuring the IV periodically with a fast voltage sweep (10 V/s). Figure 6.5 presents the results of this experiment, showing the evolution of the current-voltage characteristic during 48 hours of experiment. Although with some variability, the breakdown voltage remains above the ATLAS specifications in the first 24 hours (V_{bd} > 700 V). After 30 hours of high humidity exposure, the sensor experiences a clear reduction of the breakdown voltage, only dropping from 500 V after 48 hours. Finally, the sensor was exposed to low humidity (<5%) in a dry storage for 2 hours (dotted line in Figure 6.5), recovering the performance observed prior to the humidity exposure. A similar experiment was performed applying a fixed bias for a long period, with the sensor exposed to high humidity, resulting in a leakage current with a high variability (Figure 6.6), reaching increments of two orders of magnitude, due to a decrease of the breakdown voltage below the applied bias.

After these experiments, the sensors exposed to high humidity levels and only biased for short IV measurements of less than two minutes (10 V/s), recover their initial breakdown behaviour after only 2-3 hours in low humidity, confirming the benefits of a dry and controlled storage. In contrast, the sensor biased for a long period in high humidity irreversibly lowered its breakdown voltage, even after several days in dry storage or after baking treatments. These results were observed in different large area and miniature sensors, proving the importance of avoiding sensor biasing under prolonged exposures to high humidity.

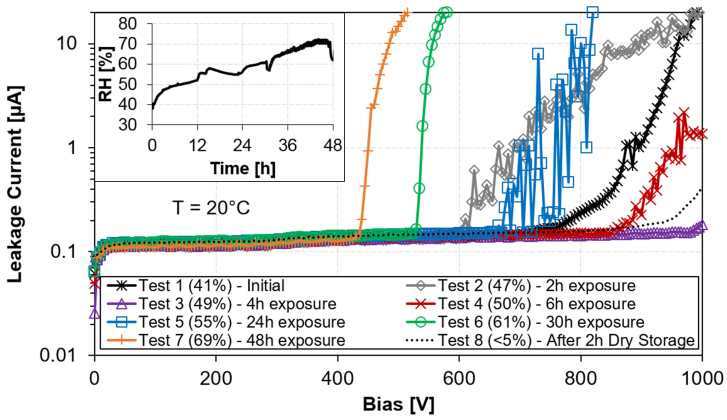


Fig. 6.5: Breakdown voltage degradation of a large area strip sensor exposed to high humidity (inner plot) for 48 hours.

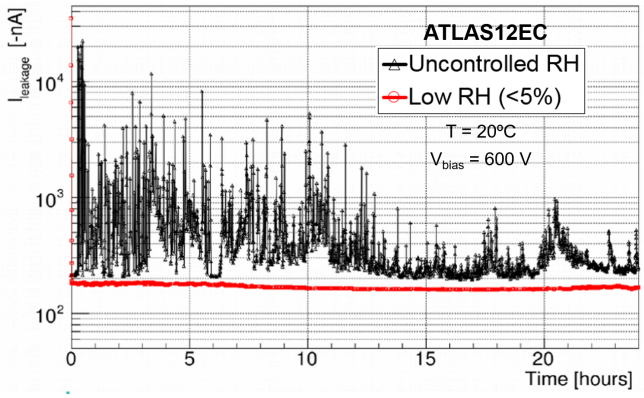


Fig. 6.6: Leakage current versus time of a large area strip sensor biased at 600 V, and exposed to uncontrolled humidity (black) and exposed to low humidity (red).

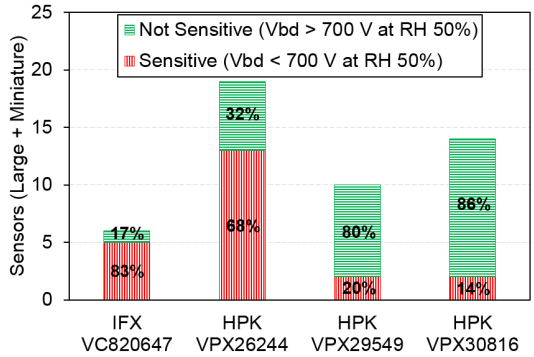


Fig. 6.7: Study of humidity sensitivity incidence in large area and miniature strip sensors of four different fabrication batches from Hamamatsu (HPK) and Infineon (IFX).

Incidence:

An extensive study was carried out to evaluate the incidence of the humidity sensitivity in different ATLAS17LS fabrication batches, three from Hamamatsu (VPX26244, VPX29549 and VPX30816) and one from Infineon (VC820647). Hamamatsu fabricated the batch VPX29549 with a "special" passivation[1] dedicated to humidity sensitivity studies.

With the aim to classify the influence of humidity on the sensor performance, devices showing a reduction of the breakdown voltage below the ATLAS specifications (700 V), at a relative humidity of 50%, were labelled as *sensitive*. On the other hand, devices fulfilling the specifications, even at a relative humidity of 50%, were classified as *not sensitive*. Figure 6.7 shows a summary of the results obtained for ATLAS17LS large area and miniature sensors.

The first batches fabricated by both foundries show a high degree of sensitivity, with 83% of the Infineon devices (VC820647) and 68% of the Hamamatsu sensors (VPX26244) showing a breakdown voltage out of the ATLAS specifications at an RH of 50%. In contrast, the Hamamatsu batch with a "special" passivation (VPX29549) shows a clear improvement, with only 20% sensitive sensors, indicating the key role played by the passivation in the humidity sensitivity phenomenon. However, it is worth mentioning that the passivation layer used for this batch is only for research purposes, not for sensor production. Finally, the last batch fabricated by Hamamatsu (VPX30816) shows the best response to humidity, with only 14% of the sensors tested with a breakdown below 700 V at high humidity.

[1]The detailed composition of this passivation layer is proprietary information of the manufacturer, and it is not disclosed to the collaboration.

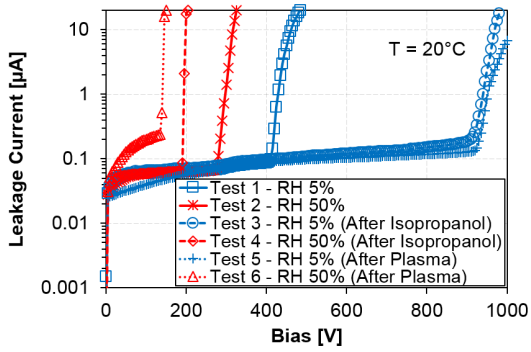


Fig. 6.8: Influence of isopropanol (dashed lines) and plasma (dotted lines) cleaning in humidity sensitivity of a large area strip sensor.

6.1.3 Investigation of Mechanisms

Surface Cleanliness:

With the aim of investigating the mechanisms behind the humidity sensitivity, a large area ATLAS17LS prototype, showing clear reduction of the breakdown voltage at high humidity, was subjected to different cleaning techniques to evaluate the influence of surface contaminants on the performance degradation.

Figure 6.8 shows IV curves at low and high humidity, with a decrease of the breakdown voltage (from 410 V to 275 V) at an RH of 50%. After these initial measurements, the large area sensor was cleaned by submerging the device 5 minutes in isopropanol while applying ultrasounds, followed by 5 minutes in deionized water and 10 minutes at 100ºC, with low humidity, to dry the sensor surfaces. A clear improvement of the breakdown voltage at low humidity is observed, from 410 V to 920 V, after the isopropanol cleaning, probably associated to the removal of contaminants in the surface. However, the breakdown voltage in high humidity is still degraded, showing no influence of the isopropanol cleaning on the humidity sensitivity of the device.

A second cleaning technique was also tried, removing organic compounds from the sensor surface by applying plasma cleaning for 5 minutes, with a power of 500 W and an O_2 flow of 200 ml/minute. The sensor shows a high breakdown voltage at low humidity after plasma cleaning (dotted lines in Figure 6.8) but no improvement either on the humidity sensitivity.

The isopropanol and plasma cleaning clearly improved the performance of the large area sensor in dry conditions, but no significant influence was observed at high humidity. Thus, the mechanisms responsible for the humidity sensitivity seem not to be related to the cleanness of the device surface.

Sensor Edge Configuration:

Large area ATLAS12EC and ATLAS17LS sensors, showing breakdown degradation at high humidity, were characterized using the Lock-in Infrared Thermography (LIT) technique developed by the Power Devices Group of IMB-CNM [111]. The LIT characterization technique uses an infrared camera with an internal lock-in module and microscopic lens to acquire thermal images that can locate hotspots in the sensor. Figure 6.9 presents a thermal image, with a lock-in AC signal of 20 V at a frequency of 101 Hz, of an ATLAS17LS large area sensor biased to 320 V, near the breakdown of the sensor at high humidity (60%), showing several hotspots located in the sensor edge. The presence of hotspots in the edge region of ATLAS12EC and ATLAS17LS large area sensors in breakdown behaviour at high humidity was confirmed by different ATLAS institutes using different hotspot imaging techniques. Thus, these measurements can locate the origin of the humidity sensitivity at the edge of the devices.

As previously explained in Section 3.2.6, the configuration of the sensor edge in the new large area devices, so-called *slim-edge* [112], is one of the features of the new ATLAS ITk strip sensors. The slim-edge configuration (Figure 6.9) reduces the distance between the active area and the silicon physical edge by more than 50% (from 1.1 mm to 0.45 mm on the narrowest side) compared to the configuration used in the sensors currently installed [14], with the aim to minimize the inactive areas of the tracking sensors. In order to achieve this reduction, the separation between the guard ring and the edge ring is reduced, whilst the separation between the bias and guard rings is similar to the previous LHC sensor designs.

With this sensor edge configuration, the maximum bias voltage (V_{max}) that this sensor region can withstand can be calculated as

$$V_{max} = DS_{air} + 2hS_{passiv} \tag{6.1}$$

where D is the separation between the guard ring metal and the edge ring metal (defined in Figure 6.9), h is the passivation thickness, S_{air} is the dielectric strength of air and S_{passiv} is the dielectric strength of the passivation layer. Taking the literature values for S_{air} and S_{passiv}, assuming a SiO_2 passivation layer, of 3 V/μm and 10^3 V/μm respectively, the minimum passivation thickness needed to avoid breakdowns below 1 kV in the sensor edge should be in the range of 300-350 nm, for both HPK and IFX designs.

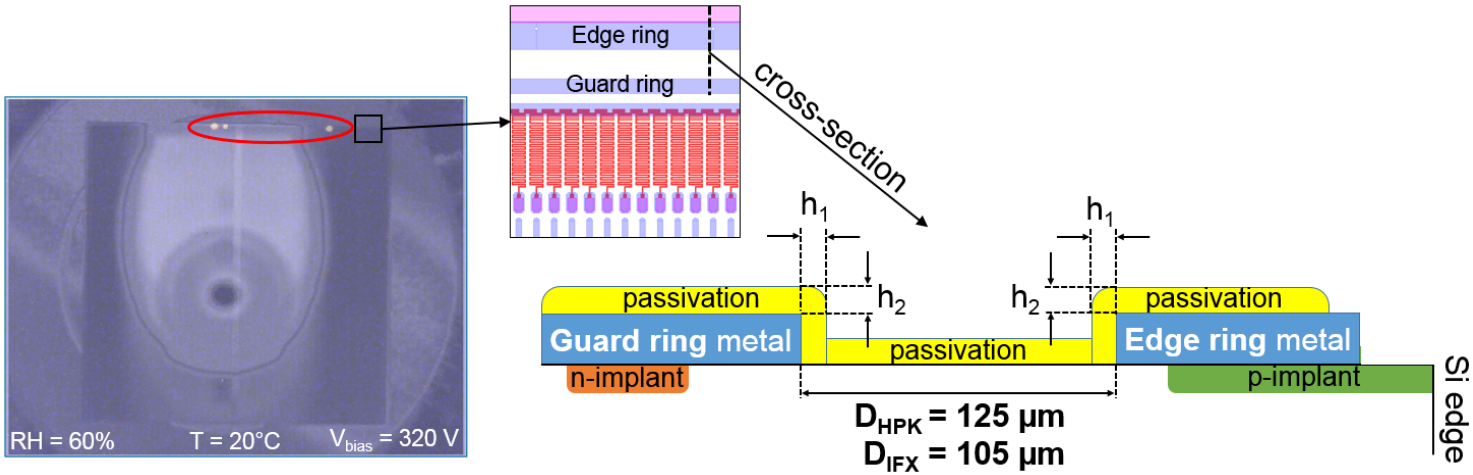


Fig. 6.9: Lock-in Infrared Thermography image of an ATLAS17LS large area strip sensor, in breakdown behaviour at high humidity (60%), showing several hotspots in the sensor edge region. A schematic cross-section of the sensor edge configuration is also shown, including layout distances for Hamamatsu and Infineon designs.

The good performance of the large area sensors at low humidity validates the slim-edge design in operating conditions. However, in the presence of humidity, the dielectric strength of air and the SiO_2 may decrease [113] along with the sheet resistance of the passivation-air interface [108]. In these conditions, and under high applied bias, thin conducting channels can be created in weak spots of the passivation and/or in the passivation-air interface, generating high current densities in these areas. These weak points could be also related to trapped charges during the deposition of the passivation, e.g. because of hydrogen rich atmospheres (*built-in positive charges*). At low relative humidity the charges are inert due to the low oxide conductivity, but at high relative humidity these trapped charges may become mobile and give rise to currents. This would be compatible with the hotspot observations and with the reversibility of the observed effect. When these high current densities are kept in the passivation layer exposed to high humidity, a permanent degradation of the dielectric can be induced in these areas, triggering an irreversible reduction of the sensor breakdown voltage. Consequently, the lower incidence observed on miniature sensors could be attributed to a reduced edge perimeter (90% less than large area sensors) that reduces the probability of weak spots.

On the other hand, in a different breakdown mechanism, positive ions (H^+) present in the air due to the high humidity can accumulate in the SiO_2-air interface depending on the bias configuration. Consequently, the accumulation of positive ions in the surface will increase the electron inversion layer already present in the Si-SiO_2 interface due to the built-in positive charges [114]. This leads to the formation of a conducting electron inversion layer which would extend the guard ring potential towards the edge [108] (see Figure 6.10). The extension of the electron inversion layer depends on the surface sheet resistance which decreases with relative humidity. Eventually the electric field at the p-n junction might exceed the breakdown field strength, locally, depending on the intensities of the positive charges in the interfaces of Si-SiO_2 and SiO_2-air. Additionally, a similar process, but with opposite charge, can happen at the edge ring where the ions charging the SiO_2-air interface would be negative [115] and a conducting hole accumulation layer might form at the edge ring side. In these conditions, and in the presence of high humidity, a large voltage drop likely happens in a very short channel between the edge of the electron inversion layer and the hole accumulation layer at the edge ring (Figure 6.10), leading to breakdown in the high field in the bulk near the Si-SiO_2 interface.

Passivation Thickness:

In order to try and correlate the mechanism responsible of humidity sensitivity with the sensitivity differences observed between batches with identical layout designs (Figure 6.7), the passivation thickness was measured in miniature sensors from the four ATLAS17LS prototype batches studied in Section 6.1.2. The thickness values

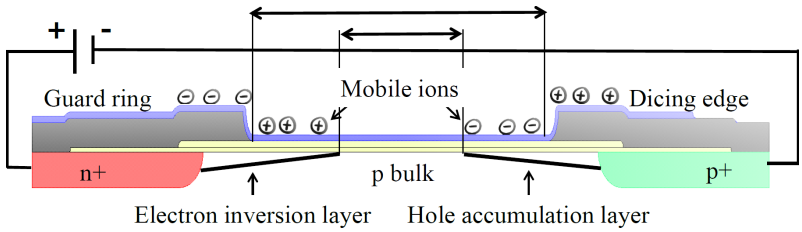


Fig. 6.10: Formation of electron inversion layer and hole accumulation layer at the guard ring and edge ring, respectively, due to the appearance of mobile surface ions in the presence of humidity.

obtained, using different techniques in several ATLAS institutes, were in the range of 350 to 750 nm, showing, in some batches, values close to the critical range of 300-350 nm, extracted from Equation 6.1. Additionally, the vertical (h_1) and horizontal (h_2) metal step coverages (defined in Figure 6.9) were measured to assess the passivation conformality:

- Hamamatsu batch VPX26244 shows *less conformal metal step coverage* ($h_1 < h_2$) in guard and edge rings, and *high humidity sensitivity*
- Hamamatsu batch VPX30816 shows *thicker and conformal passivation* ($h_1 \approx h_2$) and *no humidity sensitivity*
- Hamamatsu batch VPX29549, with special passivation, shows *less conformal metal step coverage* ($h_1 < h_2$), but *no sensitivity* probably related to the different passivation materials
- Infineon batch VC820647 with *thicker and conformal passivation* ($h_1 \approx h_2$), but showing *high humidity sensitivity* probably associated to a reduced separation between guard ring and edge ring metals

The high sensitivity of batch VPX26244 could be partially associated to a less conformal passivation, combined with a passivation thickness close to the critical range calculated above. Similarly, the absence of humidity sensitivity of batch VPX30816 could be attributed to a thicker and conformal passivation coverage. Thus, this shows indications that with the new slim-edge design the passivation has to be thick and conformal enough to cover the guard and edge ring metal layers, in order to properly isolate the edge structure from external humidity and prevent low breakdown voltages. Thick and conformal oxide layers should be beneficial in reducing the humidity dependence since the capacitance of this layer, and therefore the charge density at the Si-SiO_2 interface, depends on its thickness [115]. Accordingly, thicker passivation layers should be more efficient in avoiding inversion/accumulation layers in high humidity environments.

After the studies presented in this section, ATLAS established procedures in the sensor handling to keep low humidity conditions for reception, routine testing and storage during the production of the new ITk large area sensors, ensuring also the clean conditions during module and detector assembly, and minimizing the time the devices are biased and exposed to high/uncontrolled humidity. In addition, at the time of writing this thesis, the ATLAS collaboration has agreed with Hamamatsu to extend the humidity sensitivity studies fabricating a dedicated ATLAS17LS batch composed of five wafers with thicker passivation, and five wafers with different p-spray[2] doses for surface isolation. The results obtained with the new batch will provide valuable information to correlate the hypotheses presented above with the actual mechanisms behind the humidity sensitivity observed in large area silicon sensors.

6.2 Beam-Loss Damage Experiment on Silicon Strip Modules

One of the most adverse situations in the HL-LHC could be a position loss of the particle beam, hitting the sensors of the new full-silicon ITk system directly or indirectly through a beam-splash. In 2006, a complete study of the damage induced by a beam-loss was performed using pixel sensors from the current ATLAS Semiconductor Tracker (SCT) [116]. The future HL-LHC requires similar studies to ensure the survival of the new silicon sensors, even in the worst scenario.

Even though current ATLAS SCT p-on-n strip sensors have implemented a beam-loss protection based on the punch-through (reach-through) effect ([117], [118]), several studies concluded that the strips can still be damaged when a large amount of charge is injected ([44], [119]). As previously explained in Section 3.2.7, the future ATLAS n-on-p strip sensors will have implemented an optimized version of the Punch-Through Protection (PTP), with a separation of 20 μm between the strip implant and the grounded bias implant [120], that should be evaluated under these adverse conditions and for the n-on-p technology.

This section presents a study of the damages induced by a beam-loss failure on ITk-like miniature strip sensors with and without PTP structure [57]. A beam-loss accident was recreated focusing proton beams with different intensities, extracted from the CERN Super Proton Synchrotron (SPS) [121], over the surface of strip sensors assembled in a prototype module. Results on the evolution of the module leakage current, effect on readout channels and strip integrity are presented.

[2] P-spray technique explained in Section 3.2.3.

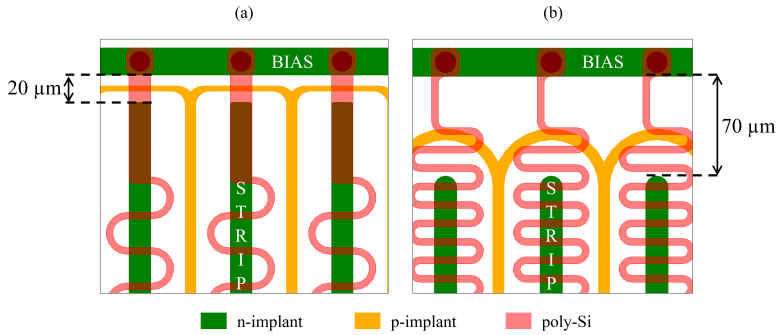


Fig. 6.11: Layout detail of the ITk prototype strip sensors used in this study: (a) PTP sensor with optimal strip-to-bias distance (20 μm) and polysilicon full-gate structure. (b) Non-PTP sensor with an increased strip-to-bias distance (70 μm) and without polysilicon gate.

Module	Sensor Size	Sensor Type	Sensor Thickness	Read-out Chip	Channels (Pitch)	Strip Length	Strip-to-Bias Distance
PTP	0.7 x 2.6 cm^2	n$^+$-on-p	300 μm	ABC130	64 (77 μm)	23862 μm	20 μm
Non-PTP	1 x 1 cm^2	n$^+$-on-p	300 μm	ABC130	128 (74.5 μm)	9981 μm	70 μm

Tab. 6.1: Characteristics of the sensors and modules tested.

6.2.1 Devices Tested

In order to evaluate the functionality of the PTP during a beam-loss, two ATLAS-like strip sensors (Figure 6.11), designed and fabricated at IMB-CNM ([23], [122]), with and without PTP structure have been tested. The strip isolation is done via an individual p-stop surrounding each strip. Table 6.1 shows detailed information of the test devices. The sensors were wire-bonded to ABC130 readout chips [103], and assembled in two different ITk strip modules.

All data were multiplexed through the Hybrid Control Chip (HCC) [103] and routed via a custom designed PCB along with High Voltage (HV) and Low Voltage (LV) connections. The HCC interfaces the ABC130 ASICs on the hybrid to the End-of-Substructure (EoS) electronics.

6.2.2 Beam-Loss Experiment

High-Radiation to Materials (HiRadMat) facility:

HiRadMat is a users facility at CERN, designed to provide high-intensity pulsed beams to an irradiation area where material samples can be tested [123]. The facility uses a 440 GeV proton beam extracted from the CERN SPS with a maximum pulse length of 7.2 μs, to a maximum pulse energy of 3.4 MJ. For the present experiment, a variable

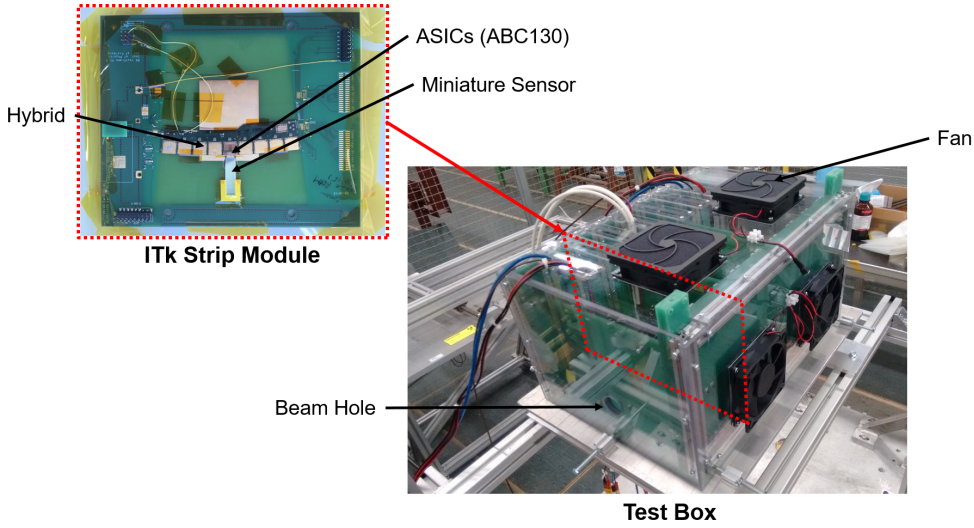


Fig. 6.12: Test box and ITk strip module used for the beam-loss experiment at HiRadMat facilities.

number of proton bunches with 10^{11} p/bunch were extracted, from 1 to 128 bunches, with tunable spacing and beam size (from 0.1 mm to 0.2 mm) for local or global approaches. Recent calculations indicate that future HL-LHC will produce proton bunches up to a range of 2.2-3.5·10^{11} p/bunch ([124], [125]). Thus, the scenario recreated for this experiment could be directly compared to the expected in a HL-LHC beam-loss failure.

Test box:

The test box was designed by the HiRadMat group, to host up to eight ATLAS prototype modules, oriented to be hit perpendicularly by the extracted proton beam (Figure 6.12). The modules inside the box are isolated from the light, and a cooling system composed of four fans allows air flow, keeping the temperature of the modules stable close to 40°C. Holders for aluminum foils are included at the front and back entrances to the box to provide beam positioning, and the box is placed on a remotely controlled table to put the modules in and out of the beam.

Test Routine:

A proton beam with a radius of 2 mm, focused to hit the center of the silicon strip sensor, was used to recreate the beam-loss failure. Table 6.2 summarizes the increasing number of bunches used in each irradiation, as well as the beam intensity and the total number of protons seen by the sensors at the end of the experiment. During the experiment, the module leakage current was continuously monitored with the sensor biased. A three-point gain test was performed before the tests, injecting three different

Beam Radius	Spacing	Bunches	Proton Intensity	Total Protons
2 mm	25 ns	1, 4, 12, 24, 36, 72, 144, 288	10^{11}	$1.16 \cdot 10^{13}$

Tab. 6.2: Test steps at the beam-loss experiment.

charges and varying the threshold value of the discriminator from zero to its maximum. The measured average hit rate versus threshold is fitted with a sigmoidal curve and the value at its 50% (V_{t50}) is extracted as well as its sigma. From a linear fit of charge versus V_{t50}, the module noise was obtained [126].

6.2.3 Effect on Module, Readout and Sensor

PTP Characterization:

In a first approach, as detailed in Section 2.4.3, the effectiveness of the PTP structure can be evaluated measuring the evolution of the resistance between the strip implant and the grounded bias rail when a voltage is applied to the strip implant. This characterization prior to the beam-loss experiment was done on a probe station at 20°C and in a dry environment (RH < 5%). The sensors, with a full depletion voltage of 35 V, were fully depleted applying a reverse bias voltage of 100 V to the backplane, leaving the bias ring grounded. A test voltage (V_{test}) was applied to the DC pad, and the induced current (I_{test}) was measured between the strip implant and the bias ring (see Figure 5.1(e)). The effective resistance (R_{eff}) can be calculated from the equivalent circuit composed by the bias resistance (R_{bias}) in parallel with the punch-through resistance (R_{PT}) [43], and consequently can be extracted from Equation 2.5.

Figure 6.13 shows measurements on both sensors, evidencing a drastic increase of the strip current at a certain punch-through voltage (around 20 V) on the device equipped with PTP and therefore a large decrease of the effective resistance (down to 50 kΩ) when the strip voltage increases above the PTP voltage. In contrast, the sensor without punch-through protection shows a lower increase of strip current at a higher voltage (around 25 V), and a lower decrease of effective resistance (down to 200 kΩ). This phenomenon, induced by the PTP structure, illustrates a better evacuation of the accumulated charge through the grounded bias, protecting the coupling capacitor from damages in the event of a beam-loss.

Beam-loss Effect on Modules:

During the beam-loss experiment, both sensors assembled on modules were fully depleted applying a reverse bias voltage of 150 V. Unfortunately, due to connectivity problems during the experiment, only the leakage current of the module equipped

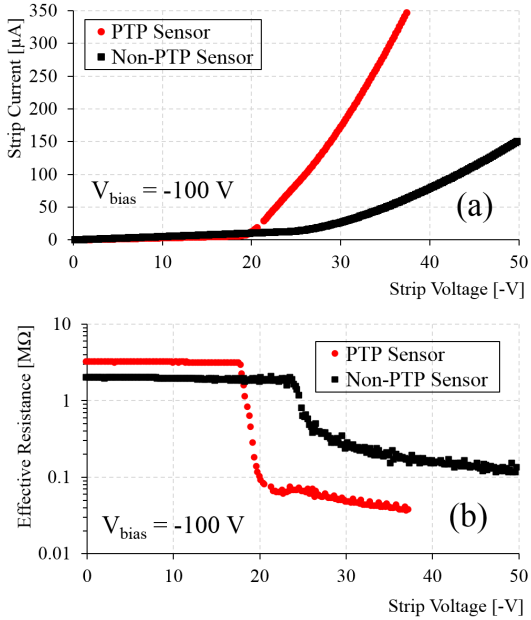


Fig. 6.13: Strip current at 20°C and dry environment (a), and calculated effective resistance (b) for sensors with and without PTP.

with the PTP sensor was monitored. Figure 6.14 shows the leakage current after each proton shot for the PTP module. The vertical dashed lines correspond to each beam shot and the color represents the different number of proton bunches per shot. A clear peak of the leakage current after each shot is observed, showing also the relaxation time needed to reach a new higher stable configuration.

Figure 6.15 shows a comparison of the module noise per channel, for both sensors, before and at the end of the beam-loss experiment. Figure 6.15(a) shows that 99% of the PTP module channels have been affected by the direct proton beam, showing abnormal (meaningless) low noise after the irradiation. On the other hand, Figure 6.15(b) indicates that more than 40% of the non-PTP module channels survived the beam-loss experiment, showing similar noise values before and after the irradiation. Noise variations between strips can be attributed to ionization damage induced by the intense proton beam, i.e. increase of strip capacitance or partial pinhole generation. A detailed study on the evolution of the number of damaged channels in the PTP module with the number of proton bunches in this experiment can be found in [126].

Beam-loss Effect on the Readout Electronics:

After the beam-loss experiment, the sensors were disassembled from the module and the noise of the ABC130 readout chips was tested without the sensors. Figure 6.15(a)

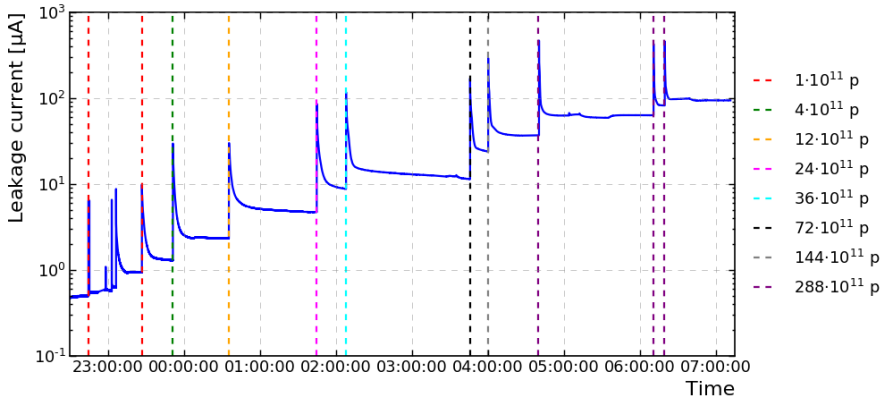


Fig. 6.14: Leakage current of the module assembled with the PTP sensor as a function of time at a constant temperature of 40°C.

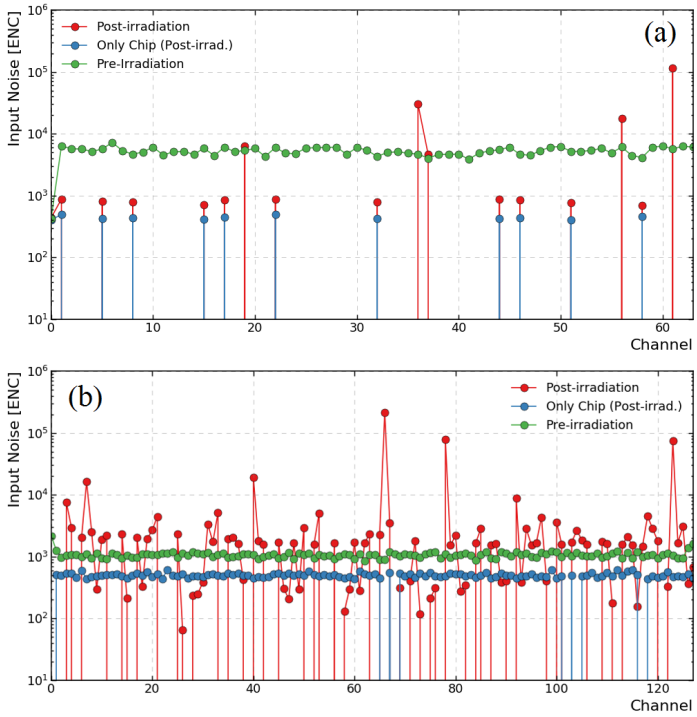


Fig. 6.15: PTP (a) and non-PTP (b) module noise measurements: pre-irradiation (green) and post-irradiation (red). Noise measurements of ABC130 read-out chip (blue) post-irradiation, with the sensor disassembled, also represented to show the chip performance after beam-loss.

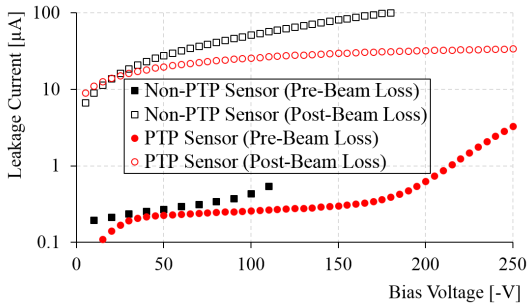


Fig. 6.16: Influence of beam-loss experiment on sensor leakage current.

shows a similar percentage of operative readout channels after irradiation (less than 1%) for the chip assembled to the PTP sensor, than seen in the assembled module.

On the other hand, more than 95% of the readout channels show unaltered noise values (Figure 6.15(b)) for the chip that was connected to the non-protected sensor, in contrast with the results of the assembled module. In a first approach, this result can be taken as an indication that the beam-loss damage was done directly on the non-PTP sensor strips, and not on the readout chip.

Beam-loss Effect on the Silicon Strip Sensors:

With the sensors disassembled from the readout chips and modules, both devices were characterized in a probe station. Figure 6.16 shows the leakage current before and after the beam-loss experiment for the sensor with and without PTP structures. Since the irradiation received by the sensors during the experiment was performed using a proton beam with a radius of 2 mm, and the sensor thickness is 300 μm, the radiation damage will be located only in a volume of 3.77 mm^3. As detailed in Table 6.2, the total number of 440 GeV protons received by each sensor at the end of the experiment was $1.16{\cdot}10^{13}$ that, given the beam radius of 2 mm, corresponds to a total fluence of $9.23{\cdot}10^{13}$ protons/cm^2. Using Equation 2.1, the fluence can be converted to 1-MeV neutron equivalent (n_{eq}) fluence, assuming a hardness factor of 0.57 for protons with 440 GeV [34], obtaining a total fluence per sensor of $5.29{\cdot}10^{13}$ n_{eq}/cm^2. Then, from Equation 2.2, and assuming a related damage factor α between 4 and $5{\cdot}10^{-17}$ A/cm ([36], [37]), the expected increase in leakage current (ΔI) on the sensors tested will be between 8 and 10 μA, in line with the observed in the sensor after the beam-loss experiment (Figure 6.16).

In order to evaluate the strip integrity after the experiment, the current across the coupling capacitor was measured for the PTP and non-PTP strips. Figure 6.17(a) shows the capacitor current for the PTP and non-PTP strips at 1 V. All the 64 punch-through protected strips present functional values of current (less than 0.1 nA), indicating that

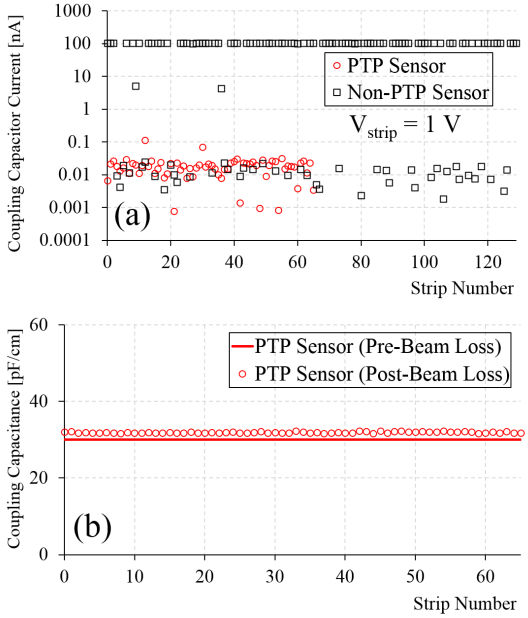


Fig. 6.17: Current across the strip coupling capacitor for both sensors (a) and strip coupling capacitance of the PTP sensor before and after the beam-loss (b).

there is no electrical continuity across the coupling oxide. On the other hand, more than 60% of the 128 non-PTP strips show abnormally high currents, limited by the equipment compliance (100 nA), indicating that the corresponding coupling capacitors were damaged by the beam-loss, creating irreversible conduction channels by dielectric rupture. As a second check, the coupling capacitance of the PTP strips was measured. Figure 6.17(b) shows no influence of the beam-loss on the coupling capacitance values, and no variation across the PTP sensor.

Hence, this characterization indicates that PTP structure effectively protected the sensor from a beam-loss scenario, unlike in the sensor without this protection that suffered irreversible damage of the coupling oxide in most of its strips. This damage can be attributed to high voltages or charges reaching the front-end stage of the readout electronics through the wire-bonds and when the strip coupling capacitor is damaged. A new readout chip called ABCStar [127], with ESD protection at the input pads, is currently under evaluation. Further beam-loss damage studies will be needed to evaluate the performance of the new ABCStar readout chip wire-bonded to a PTP sensor.

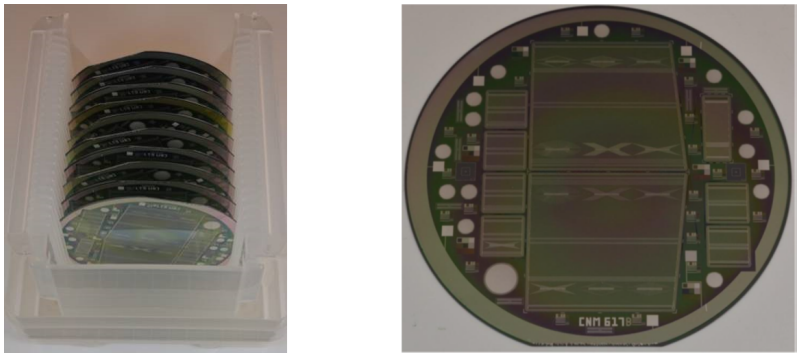


Fig. 6.18: Picture of the Petalet Top sensors wafers fabricated at IMB-CNM, including five different EPA structures.

6.3 Optimization of Embedded Pitch Adapters

A solution was proposed to facilitate the interconnection between the sensors and the readout chips when the pitch of the strips is larger than the pitch of the ASIC channels, or when it is variable, as in the new End-cap sensor designs. This solution, called *Embedded Pitch Adapters* (EPA) and previously introduced in Section 4.4, consists of routing the strips with metal tracks, using an additional metal layer to a new set of bonding pads with a pitch identical to the readout chip.

A first fabrication of End-cap prototype sensors (*Petalet Top sensors*) with EPAs was carried out at the IMB-CNM cleanroom. Initially, the strip metals with variable pitch were routed using a first EPA design called *Basic* (see Figure 4.22), showing no indication of undesired signal coupling from the strip to crossing EPA tracks (*cross-talk*) or signal coupling directly from the bulk (*pick-up*) from laser tests[3] [63]. However, an expected increase in noise, and noise variability, was observed on sensors assembled in modules (Figure 4.23), probably associated with the contribution of the EPA to the inter-strip capacitance.

With the aim to minimize the module noise and reduce its variability, four new EPA structures were designed[4]: *Equalized*, *Varying*, *Rectangular-A* and *Rectangular-B*. The new EPA designs, along with the Basic structure, were implemented in the Petalet Top sensors and a new batch was fabricated at IMB-CNM (Figure 6.18) to study their influence in the sensor performance [91].

[3]Detailed information on these phenomena can be found in Section 4.4.1.
[4]Detailed information on the different EPA structure designs can be found in Section 4.4.2.

6.3.1 Fabrication Challenges

A total of twelve wafers were fabricated with the five different EPA designs implemented in the Petalet Top sensors (Figure 4.26), using as substrate high-resistivity, p-type, 300 μm thick wafers with 4-inch diameter. Each EPA design was implemented in two different structures each with a different track width (10 and 20 μm). The inter-metal oxide layer was deposited by a low-temperature Plasma Enhanced Chemical Vapor Deposition (PECVD) processing step. With the objective to study the influence of the inter-metal oxide layer in the performance of strip sensors with the strips routed with EPA structures, four different thicknesses were deposited (1, 2, 3 and 4 μm) in sets of three wafers for each one.

Due to the different thermal expansion coefficients of silicon oxide and silicon, the inter-metal oxide layer creates stress inducing wafer bowing which can affect subsequent fabrication steps, e.g. photolithographic mask alignment, or even compromising the module assembly or the tracking resolution. In consequence, the bowing of the different wafers was monitored during the fabrication. The bow is defined here, according to standards [128], as the distance between a point at wafer center, and a reference plane defined by three points at the wafer edges. In this case, the stress introduced by the inter-metal oxide is compressive, so a positive bow is expected, i.e. wafer edge is raised with respect to the wafer center when devices are on the top surface. Figure 6.19 shows the bowing results obtained for the wafers with different inter-metal oxide thicknesses. As it can be seen, the bowing is already very significant (roughly 300 μm) with 3 μm thick oxide, and although the photolithography could be realized, this bowing would be too large for the proper assembly of the modules, and for particle tracking resolution. In the case of 4 μm oxide thickness, the bowing of the wafers already generated difficulties in the processing, so this option is discarded for technological reasons.

The quality of the via contact between the first metal (strip metal) and the second metal (EPA metal) (Figure 6.20) was also checked to evaluate if this could affect the yield of good channels in the sensors fabricated with different inter-metal oxide thicknesses. For this purpose, *Daisy-chain* structures were implemented in the periphery of the wafers. This test structure consists of a set of vias connected in series such that the first via goes from second metal (EPA metal) to first metal (strip metal), then a short line of first metal connects to the next via which goes from first metal to second metal, then a short line of second metal connects to the next via which goes from second metal to first metal, and so forth for a total of 200 via contacts. Figure 6.21 shows a layout image of the Daisy-chain test structure and the single via resistance values obtained when different numbers of vias are measured in series. As it can be seen, the via resistance measured is high when a few number of vias are tested, due to the influence of parasitic contact resistances from the measurement setup. However, as

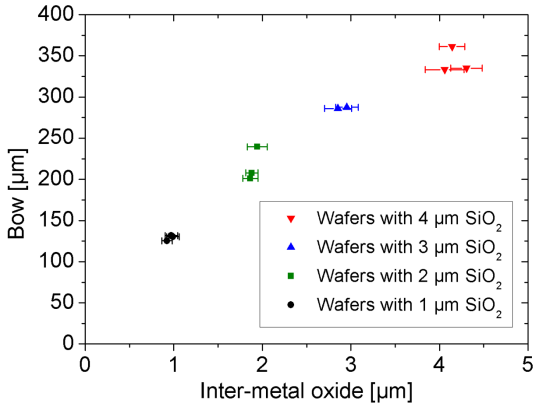


Fig. 6.19: Wafer bowing measured on eleven wafers fabricated with different inter-metal oxide thicknesses.

expected, this influence becomes negligible when a high number of vias are tested in series, showing a plateau value of about 0.18 Ω/via, compatible with a good ohmic contact between metals. On the other hand, no measurable differences were observed in the via resistance for different inter-metal oxide thicknesses, indicating a very good coverage of the via with the metal.

6.3.2 Inter-strip Capacitance

In strip sensor technologies the inter-strip capacitance (C_{int}) is directly related to the noise measured in the modules with the strip sensors assembled [29]. Since the introduction of second metal tracks (EPA metals) on top of the standard strip metals contribute to the increase of the total inter-strip capacitance, this parameter should be studied in detail to evaluate the performance of the different EPA structures. On the other hand, as the EPA tracks cross on top of several of the first metal tracks, the inter-strip capacitance must take into account more than the first neighbours. In fact, for some EPA designs, many tracks cross on top of almost a quarter of the strips contacted by this EPA. At IMB-CNM a specific setup was made to be able to measure the inter-strip capacitance taking into account all the strip neighbours contacted by the EPA.

Figure 6.22 shows a schematic cross-section of a strip sensor, with EPA tracks, indicating the different contributions expected for the total inter-strip capacitance. As it can be seen, an increase in the capacitance is expected due to the appearance of new capacitances between the strips and the EPAs and also between EPA tracks. Consequently, besides the standard (STD) capacitance between strips $C_{int,STD}$, the inter-strip capacitance of the strip i (C^i_{int}) in presence of EPA structures will get two new contributions:

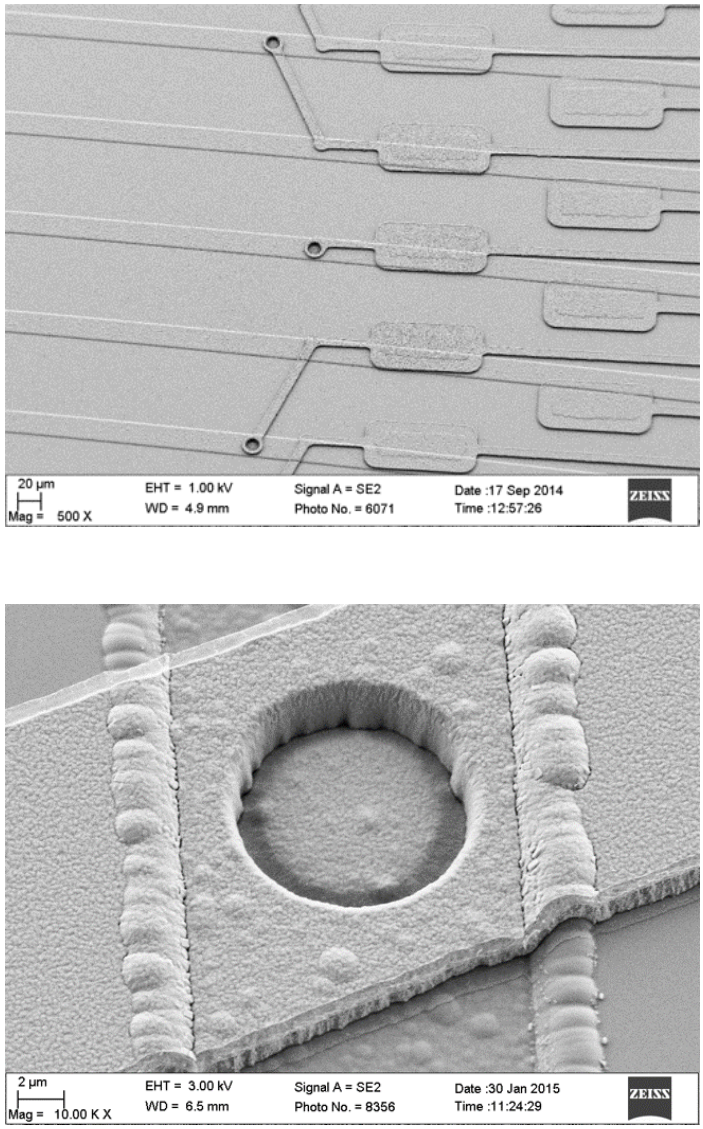


Fig. 6.20: Scanning Electron Microscopy (SEM) images of the 12 μm diameter inter-metal vias used to contact the strip metal with the EPA metal.

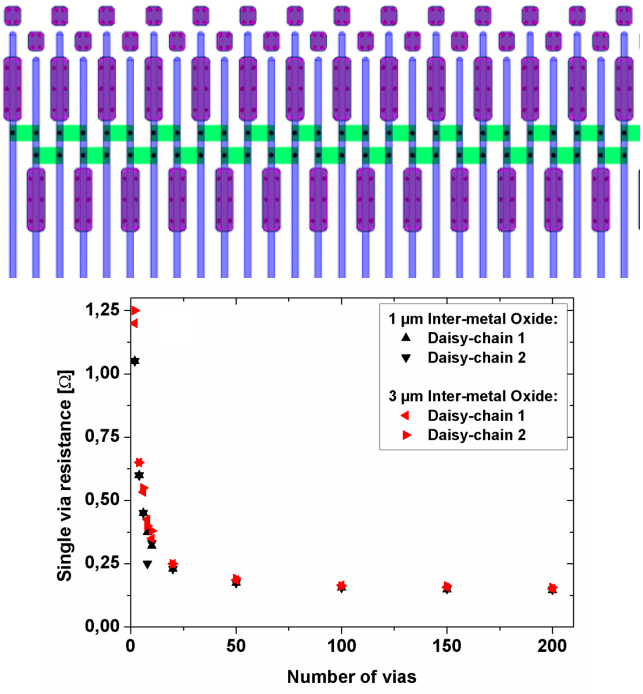


Fig. 6.21: Daisy-chain test structure (top) used to evaluate the via contact resistance (bottom) between the strip metal and the EPA metal.

the capacitance between EPA metal (M2) tracks $C^i_{int,M2}$ and the capacitance between the strip metals (M1) and the EPA metals (M2) $C^i_{int,M2-M1}$, and will be expressed as

$$C^i_{int} = C^i_{int,STD} + C^i_{int,M2} + C^i_{int,M2-M1} \tag{6.2}$$

One specific feature of the EPA structures is that the second metal channels (EPA tracks) cross on top of many of the first metal channels (strip metals), increasing the coupling between channels that are far from each other in the sensor. In particular, $C_{int,M2-M1}$ will receive contributions from all the EPA tracks (second metals) crossing on top of the metal of the strip tested (first metal), and also from the strips (first metal) crossing below the second metal of the strip tested. Additionally, $C^i_{int,M2}$ will also be influenced by distant channels due to the high density of second metal tracks in some EPA structures (specially for higher track widths). On the other hand, $C_{int,STD}$ will have a negligible contribution from the distant channels due to the high separation between strips. Consequently, in order to properly deduce the channel noise variability from the inter-strip capacitance in sensors with EPA, the measurement should be done taking into account all the 128 channels routed by the EPA structure. Thus, the three additive parameters in Equation 6.2 can be expressed as

$$C^i_{int,STD} = C^i_{Bulk} + \sum_{j=i-1}^{j=i+1} (C^{i,j}_{Implant} + C^{i,j}_{M1-Implant} + C^{i,j}_{M1-M1}) \tag{6.3}$$

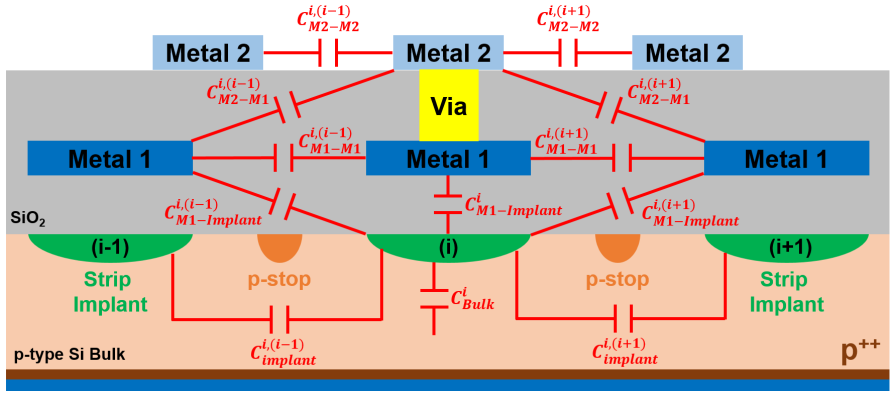


Fig. 6.22: Schematic cross-section of a strip sensor with embedded pitch adapter, indicating the different contributions to the total inter-strip capacitance.

$$C^{i}_{int,M2} = \sum_{j=1}^{127} C^{i,j}_{M2-M2} \tag{6.4}$$

$$C^{i}_{int,M2-M1} = \sum_{j=1}^{127} C^{i,j}_{M2-M1} \tag{6.5}$$

where, as represented in Figure 6.22, C_{Bulk} is the capacitance between the strip implant and the silicon bulk, $C_{Implant}$ is the capacitance between strip implants, $C_{M1-Implant}$ is the capacitance between the strip metal (first metal) and the strip implant, C_{M1-M1} is the capacitance between strip metals (first metals), C_{M2-M2} is the capacitance between EPA metals (second metals) and C_{M2-M1} is the capacitance between the EPA metals (second metal) and the strip metals (first metals).

For this purpose, a probe-card with 128 needles (Figure 6.23) has been used to measure the inter-strip capacitance. Only this way, the correct capacitance measurement can be done between the strip under tests and all the rest of the channels that are purposely grounded. In practice, the IMB-CNM switching matrix has only 24 input channels, therefore the strips are measured in groups of 20 (red channels in Figure 6.23(left)) using the central needles, whilst the rest (54 at both sides of the probe-card) are short-circuited and grounded. Then, the measurement of the 128 channels is done moving the probe-card across the EPA pads in 6 steps of 20 channels and a last step of 8 channels (20 channels x 6 steps = 120 + 8 channels = 128). In this way, with the use of the 128 probe-card, can be assured that all the channels crossing the strips under test are grounded during the measurement.

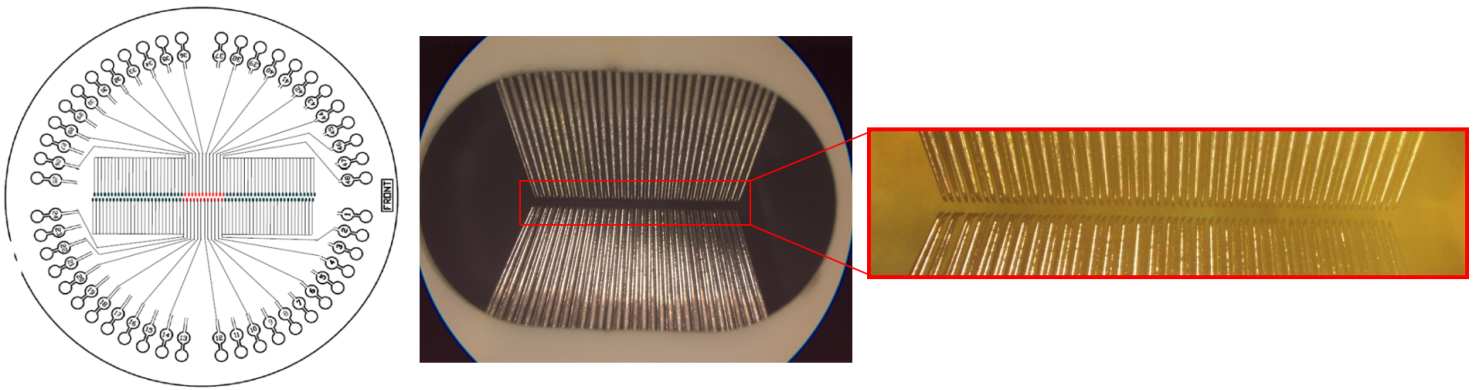


Fig. 6.23: Probe-card with 128 needles to test the inter-strip capacitance, of strip sensors with embedded pitch adapters, taking into account the contribution of all the neighbouring channels.

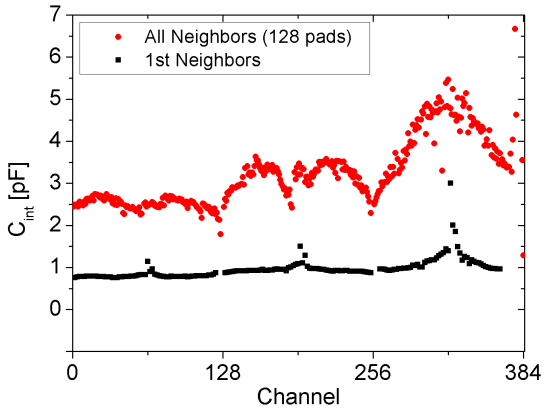


Fig. 6.24: Inter-strip capacitance, of a strip sensor with three embedded pitch adapters, measured only for the first neighbours (black) and measured with a probe-card with 128 needles (red) taking into account the contribution of all the neighbouring channels.

The inter-strip capacitance tests to study the different EPA structures were performed using an Agilent 4284A LCR meter at 100 kHz, with a signal amplitude of 100 mV and with RC-parallel configuration. Before probing the pads, a capacitance measurement is performed in the 20 active probes (central needles) without connecting the probe-card, in order to measure the parasitic capacitance introduced by the needles (*Open* correction). Then, the value obtained for each probe was subtracted for every individual capacitance measurement that is taken with this particular probe. Figure 6.24 shows the inter-strip capacitance, measured in 384 strips connected by three EPA structures, using the standard method taking into account only the first neighbours and, on the other hand, using the probe-card with 128 channels. These results clearly illustrate the importance of the use of the probe-card, showing a high influence of the far neighboring channels in the inter-strip capacitance of sensors with EPA structures.

The inter-strip capacitance, obtained using the characterization method described above, for the five EPA designs with a 10 and 20 μm track width (Figure 6.25) and 1 μm thick inter-metal oxide can be seen in Figure 6.26. Additionally, the inter-strip capacitance was also measured on identical Petalet Top sensors but without EPA structures and using the standard procedure taking into account only the first neighbouring strips (Figure 6.26(f)), with the objective to obtain only the contribution of $C_{int,STD}$ in Equation 6.2.

The EPA structures that show lower values and less variability of inter-strip capacitance are the Basic (Figure 6.26(a)) and the Rectangular-A (Figure 6.26(b)) structures, with average values around only 2 times higher than the measured on the standard sensor (Figure 6.26(f)). The Basic structure presents some variability along the structure, showing higher values of inter-strip capacitance on strips 30 and 95, magnified when for wider metal tracks (20 μm). These EPA tracks have a higher number of neighbouring

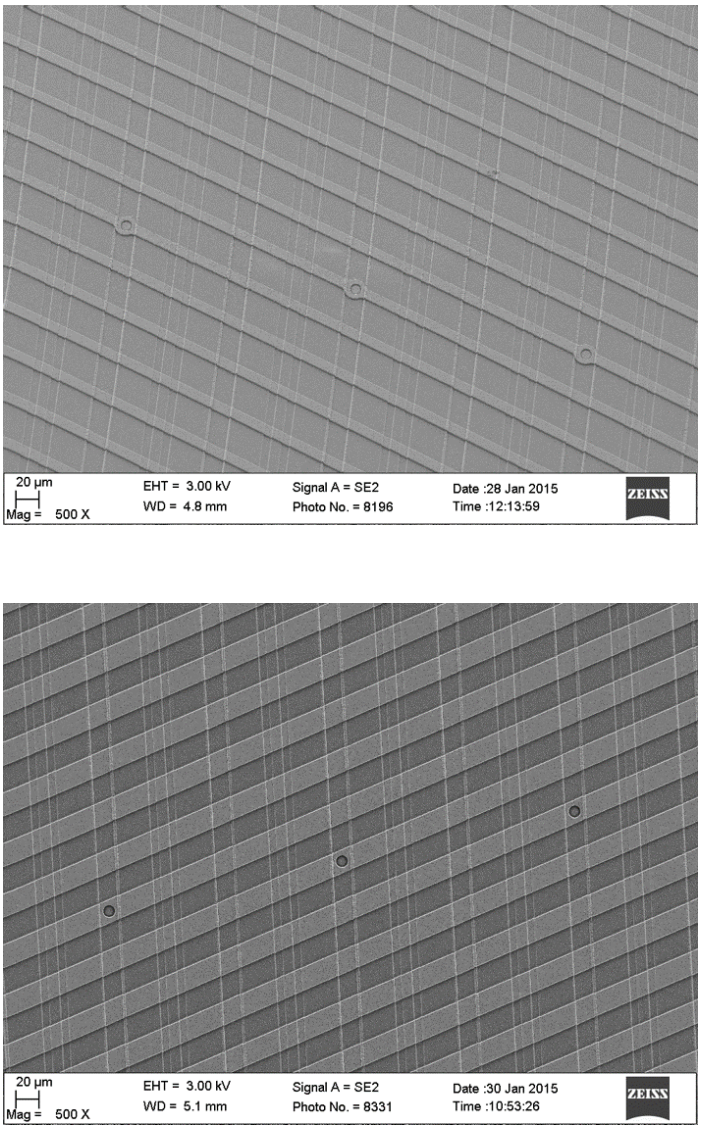


Fig. 6.25: Scanning Electron Microscopy (SEM) images of the embedded pitch adapter with two different metal track widths: 10 (left) and 20 μm (right).

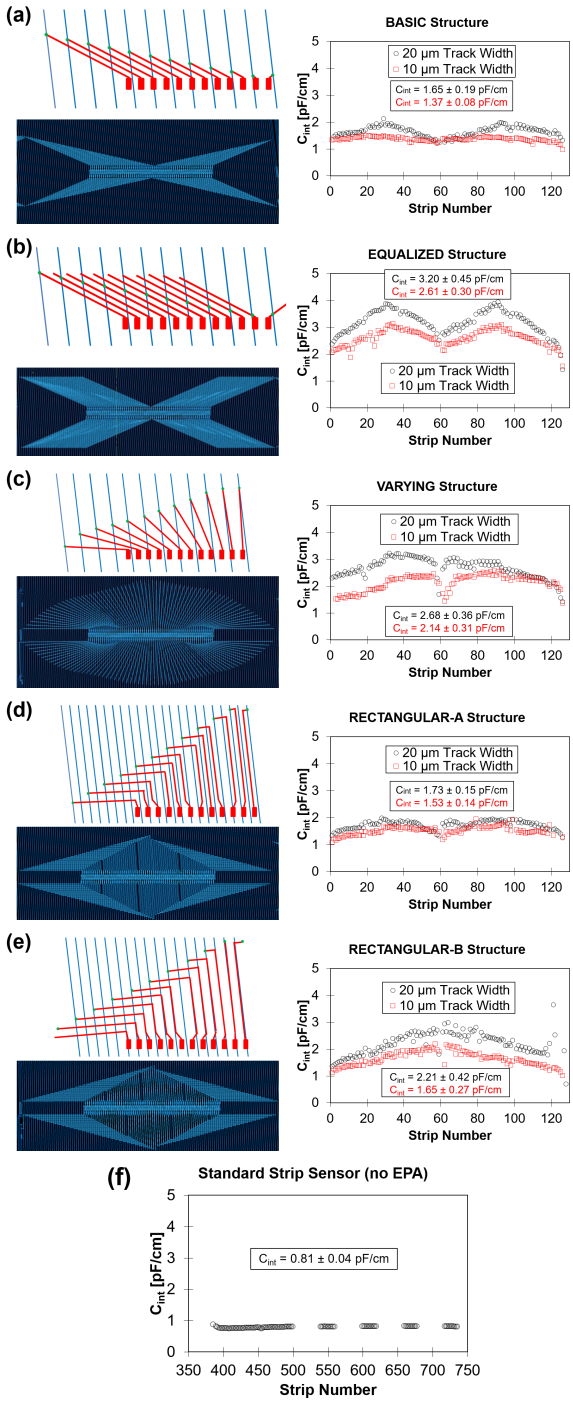


Fig. 6.26: Inter-strip capacitance results for the five embedded pitch adapter designs with 10 and 20 μm track width using a probe-card with 128 channels: Basic (a), Equalize (b), Varying (c), Rectangular-A (d) and Rectangular-B (e). Inter-strip capacitance of a strip sensor without EPA structures, measured taking into account only the first neighbours, is also shown for reference (f).

EPA tracks with longer lengths, increasing the contribution of $C_{int,M2}$ and showing an expected reduction when the track width is narrower (10 μm). On the other hand, the Rectangular-A structure, with EPA tracks going between strip metals (on top of p-stops), presents the lowest values of capacitance in the central region, where a low number of strip metals are crossed and the separation between EPA tracks is higher, minimizing the parameters $C_{int,M2-M1}$ and $C_{int,M2}$, respectively. In this case, only a small improvement can be observed for the narrowest track width, corresponding to the outermost channels, where the separation between EPA tracks (second metals) is the lowest and the maximum number of strip metals (first metals) are crossed.

The Varying and Rectangular-B structures present worse inter-strip capacitance results. On the one hand, the Varying structure has the highest separation between EPA tracks, minimizing the value and variability of $C_{int,M2}$. However, the variability of $C_{int,M2-M1}$ will be high due to the high number of strip metals crossed by the outermost EPA tracks, compared to the low number of strip metals crossed by the innermost EPA tracks, inducing larger variations on the total inter-strip capacitance. Rectangular-B structure, on the other hand, shows lower capacitance values, but similar degree of variability. In this case, the EPA tracks run on top of the strip metals in the central channels, reducing the $C_{int,M2}$ contribution due to the high separation between tracks, but increasing the $C_{int,M2-M1}$.

Finally, the EPA structure showing the worst response, with the highest inter-strip capacitance values and the highest variability, is the Equalized (Figure 6.26(b)). Since the number of strip metals crossed by the different EPA tracks is identical for all the channels, the $C_{int,M2-M1}$ parameter will be constant along the structure. However, similarly to the Basic structure, the strips 30 and 95 present a peak associated to a variation on $C_{int,M2}$, due to the high number of neighbouring EPA tracks, and because they are longer. In this sense, the improvement observed for the narrower EPA tracks will be associated with a higher separation between tracks, reducing the $C_{int,M2}$ but without remarkable influence on $C_{int,M2-M1}$.

Table 6.3 presents a summary of the results obtained for the different EPA structures and track widths, indicating which parameters vary in each case and presenting the average values obtained, the increase factor with respect to the standard sensor and the variability observed along the structure. As presented above, the lowest value and lowest variability of inter-strip capacitance is observed in the Basic and Rectangular-A structures, showing a remarkable improvement for narrower EPA track widths.

With the aim to reduce the capacitive contribution of the EPA structures, some wafers were fabricated with larger inter-metal oxide thickness. In particular, a reduction in the $C_{int,M2-M1}$ is expected when thicker oxides between the EPA tracks and the strip metals are fabricated. However, as explained in the previous Section 6.3.1, the wafer

EPA Structure	EPA Track Width (μm)	Average C_{int} (pF/cm)	Increase Factor Respect Standard	Variance (pF^2/cm^2)
None	-	0.81 ± 0.06	-	0.004
Basic	10	1.37 ± 0.08	1.69	0.01
	20	1.65 ± 0.19	2.04	0.04
Equalized	10	2.61 ± 0.30	3.22	0.09
	20	3.20 ± 0.45	3.95	0.20
Varying	10	2.14 ± 0.31	2.64	0.10
	20	2.68 ± 0.36	3.31	0.13
Rectangular-A	10	1.53 ± 0.14	1.89	0.02
	20	1.73 ± 0.15	2.14	0.02
Rectangular-B	10	1.65 ± 0.27	2.04	0.07
	20	2.21 ± 0.42	2.73	0.18

Tab. 6.3: Summary of average inter-strip capacitance values measured on five different EPA structures with two different track widths, showing the increase factor respect the standard sensors and its variance along the structure channels.

bowing induced by inter-metal oxide thicknesses of 3 and 4 μm discarded these options for technological reasons. On the other hand, the wafers fabricated with 2 μm thick oxide showed bowings around 200 μm (Figure 6.19), within the ATLAS specifications. As the best results for an inter-metal oxide of 1 μm were obtained for an EPA track width of 10 μm (Table 6.3), the study of the oxide thickness influence focused on the EPA structures with this track width. Figure 6.27 shows the inter-strip capacitance measured in the five different EPA designs, comparing the results obtained for an inter-metal oxide of 1 and 2 μm.

EPA structures Basic (Figure 6.27(a)) and Rectangular-A (Figure 6.27(d)) show no improvement for thicker oxides. In comparison, these structures have the lowest number of strip metals crossed by EPA tracks, so the total C_{int} value will be dominated by the contribution of $C_{int,M2}$, and not by $C_{int,M2-M1}$.

On the other hand, the only EPA designs showing an improvement of the inter-strip capacitance for thicker oxides were the ones with the highest number of strips crossed by EPA tracks, the Varying and the Equalized structures. In particular, as the Varying structure is dominated by $C_{int,M2-M1}$, due to the high separation between EPA tracks, the structure shows a reduction of the total C_{int} and less variability. In contrast, for the Equalized structure, the higher contribution will be expected for the $C_{int,M2}$ due to the length and proximity of the neighbouring EPA tracks, so a reduction of the total C_{int} is observed, but keeping its high variability along the structure.

In conclusion, the results obtained for the different EPA designs and configurations proposed showed that the lowest values of inter-strip capacitance, and with the lowest variability, can be obtained with the Basic and Rectangular-A EPA structures, with 10 μm track width and 1 μm thick inter-metal oxide. Both structures show similar results, with an inter-strip capacitance around 1.8 times higher than a standard strip sensor

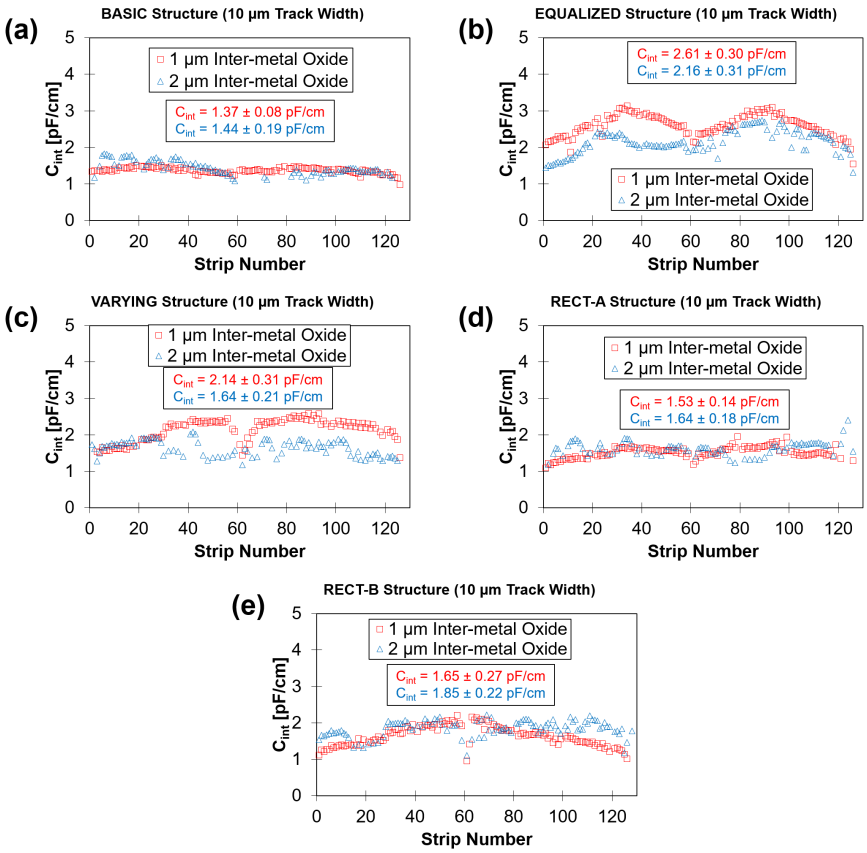


Fig. 6.27: Inter-strip capacitance results for the five embedded pitch adapter designs with 10 μm track width and different inter-metal oxide thicknesses using a probe-card with 128 channels: Basic (a), Equalize (b), Varying (c), Rectangular-A (d) and Rectangular-B (e).

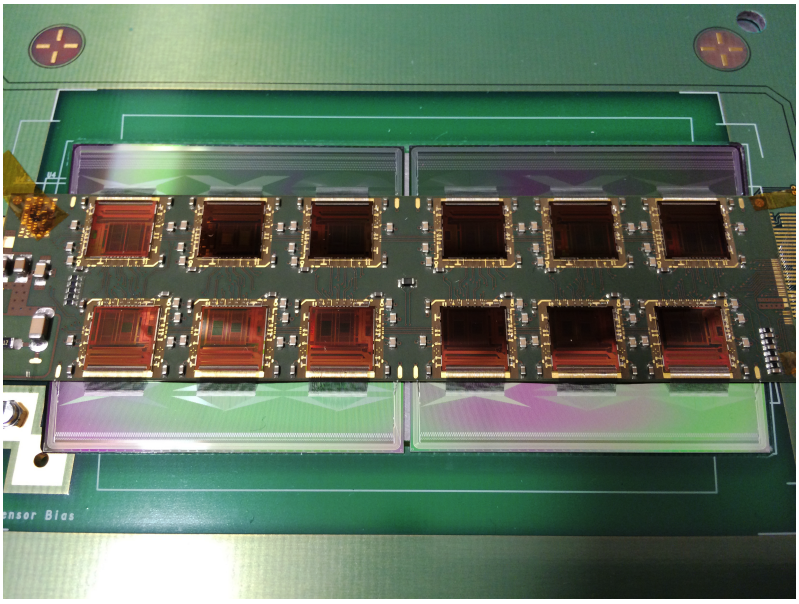


Fig. 6.28: Top Left and Top Right End-cap prototype (Petalet) strip sensors assembled in a prototype module. The readout connection is done using five different embedded pitch adapter designs with 10 and 10 and 20 μm track width.

and a variance of less than 0.02 pF^2/cm^2, that could be associated to an optimal noise measured on a module with the sensors assembled.

6.3.3 Module Noise

Two Petalet Top sensors, fabricated with 1 μm thick inter-metal oxide, were assembled in a prototype module [129] using ABCN-25 ASICs [94] (Figure 6.28), at Deutsches Elektronen-Synchrotron (DESY-Zeuthen) [130] with the objective to measure the noise of strip sensors with EPAs. For the noise measurements, 2 fC charges are injected into all channels, then 200 triggers are sent into each channel and the ASICs are read out repeatedly with increasing thresholds. From the resulting *S-curve*, all characteristics of each channel, such as noise, are determined in a fit. The readout was done connecting the module to a HSIO (High Speed Input Output) board [131] developed by the ITk collaboration, and read out with a root software called SCTDAQ [132] developed at Rutherford Appleton Laboratory (RAL) [133].

Figure 6.29 shows the input noise obtained per channel, indicating which 128-channels readout chip corresponds to each EPA structure. The noise measured can be clearly correlated with the inter-strip capacitance results analysed above (Figure 6.26). This measurement validates the testing method using a 128-channels probe-card, including the contribution of far channels, to estimate the noise behaviour of the EPAs. As it can be seen, similar conclusions can be extracted from the module noise measurements:

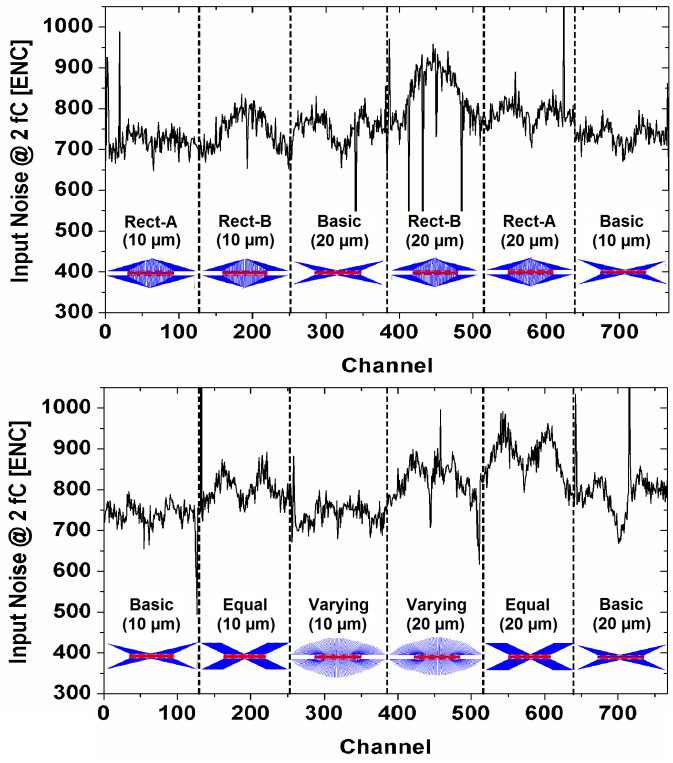


Fig. 6.29: Noise results for the different EPA structures, with 10 and 20 μm track width, measured on a module assembled with two Petalet Top sensors.

the EPA structures showing the lowest and least variable input noise values are the Basic and the Rectangular-A structure with 10 μm track width.

6.3.4 Signal Pick-up

As explained in Section 4.4.1, the implementation of EPA structures can introduce undesired effects in the sensor electrical performance that should be studied to find the optimal configuration. One of these effects is the *pick-up* phenomena [92]. Charges created in the bulk, when a particle crosses the sensor, can induce spurious signals in the EPA metal tracks directly from the bulk. Thus, the pick-up phenomenon can induce signals in channels not hit and loss of efficiency in the hit channels. Then, the signal pick-up is expected to be higher in regions without strip implant between the bulk and the EPA tracks. Consequently, this phenomena will depend strongly on the design of the pitch adapter, e.g. density of EPA tracks and their width.

The module assembled for the noise measurements presented above (Figure 6.28) was also used for the pick-up study. In particular, as a worst-case scenario, the Equalized structure with 20 μm track width was selected for this study. This structure has EPA

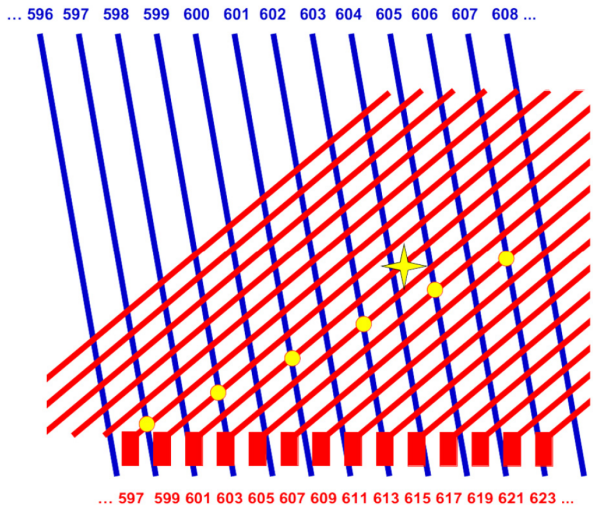


Fig. 6.30: Schematic representation of a particular area of the Equalized structure where the EPA tracks (red) cross on top of the strips (blue), showing the via contacts between them (yellow circle) and an example of the position where a particle hits the device (yellow star).

tracks that are not parallel to the strips, that minimize the chances to shield the signal pick-up, and particular regions of the structure have a high density of EPA tracks, that maximize the probability to pick-up signals directly from the bulk. Thus, considering all the EPA designs available, the Equalized structure with 20 μm track width is the structure with the highest probability to present pick-up.

Figure 6.30 shows a schematic representation of a particular area covered by the Equalized EPA tracks (in red), crossing over the standard strips (in blue) that are connected with the corresponding EPA track with via contacts (yellow circles). Ideally, the signal generated by a particle hitting the sensor (yellow star) near the strip 604 should be fully collected by the same strip implant. However, if the signal is picked up by the EPA track present in this region, the signal will be routed to the channel 601, and a fake hit in strip 601 will be recorded. Thus, in order to evaluate the pick-up phenomena in strip sensors with EPA structures, an investigation of the charge loss in the hit channel, and the fake signals induced in EPA tracks corresponding to channels not hit, was carried out.

The experiment was performed at the Diamond Light Source [134] in the UK, using a micro-focused 15 keV X-ray beam with a beam spot of 2 x 3 μm^2. A total area of 200 x 300 μm^2 was scanned, in the region of the EPA tracks (orange box in Figure 6.31), in steps of 10 x 15 μm^2, covering a total of four strips (from 603 to 606) and eight EPA tracks (corresponding to strips from 591 to 605). Since a binary readout system with ABCN-25 ASICs [94] was equipped in the module tested, a *hit* can be considered as the measured quantity exceeding a given discriminator threshold in a given readout

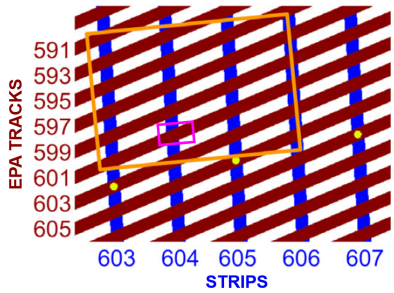


Fig. 6.31: Schematic representation of the area scanned with the micro-focused X-ray beam (orange box) and the area used to generate the hitmaps for the study of the pick-up phenomena (pink box).

channel. For each beam position in this area 4,500 randomly triggered events were recorded for 9 threshold steps between 54.4 and 80 mV. Due to the limited beam time, a threshold range was selected to be lower than the typical operating threshold of 100 mV, since the signal pick-up is expected to be higher for lower thresholds. It should be mentioned that the analysis presented below was performed by the DESY-Zeuthen group in close collaboration with IMB-CNM.

With this experimental setup, hitmaps for every threshold step can be generated, showing the number of hits (number of times the threshold is exceeded) in a given channel as a function of the beam position. Thus, a hitmap of a channel corresponding to a strip outside of the area scanned will show only noise background in absence of pick-up. Figure 6.32(a) shows the hitmap at an example threshold of 67.2 eV, obtained in a particular area indicated by a pink box in Figure 6.31, for channel 604. As expected, the region corresponding to the strip implant collects the highest number of hits, whilst the regions in the periphery of the strip implant present less hits, and the regions far from the implant show only noise background. On the other hand, Figure 6.32(b) shows a hitmap of the same area for the same threshold, but this time showing the hits observed in channel 601 (instead of channel 604). Since channel 601 is outside of the area hit by the beam, the positions showing hits will be caused by a signal pick-up carried out by the EPA track corresponding to channel 601. Consequently, the charge picked up by the EPA track 601 will not be collected by the strip 604, inducing a loss of efficiency in the strip 604 and a possible fake hit in the region of the strip 601. However, It is worth noting that in the central region of the effective area of the strip implant (solid line box in Figure 6.32) the signal is not picked up by the EPA track.

This first study revealed the appearance of the undesired pick-up phenomena in a sensor with an EPA structure, but in order to evaluate its real effect on the sensor performance, the threshold dependence and the hit position dependence should be studied in detail. With this objective, the central area of the strip (solid line box in Figure 6.32) and the peripheral areas (dashed line boxes in Figure 6.32) were selected to understand the

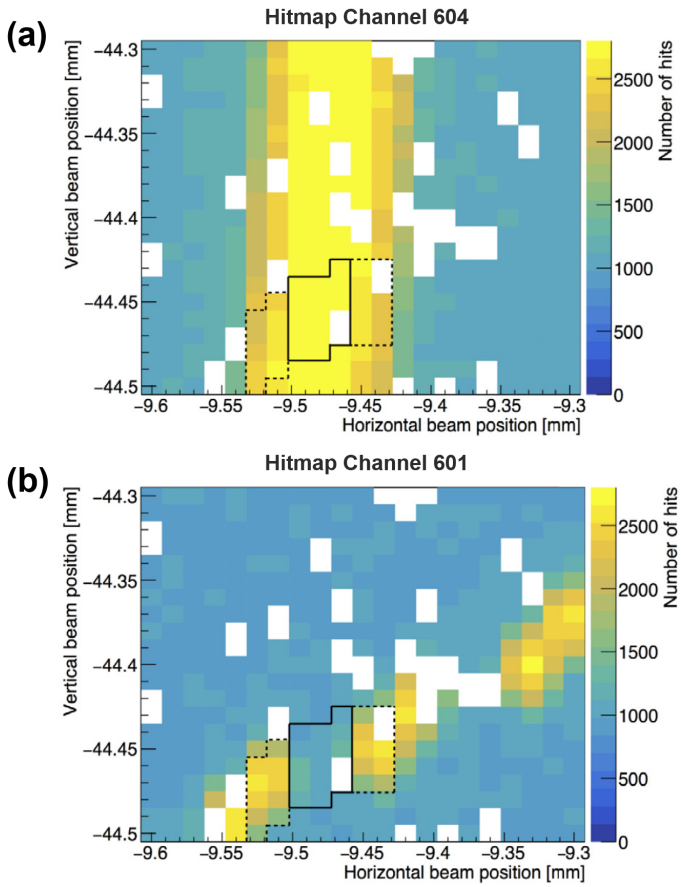


Fig. 6.32: Hitmaps of a particular area of the EPA structure (pink box in Figure 6.31) for channels 604 (a) and 601 (b). The areas enclosed by a solid line (strip center) and dashed lines (strip periphery) are used for the study of the threshold and centrality dependences on the appearance of signal pick-up.

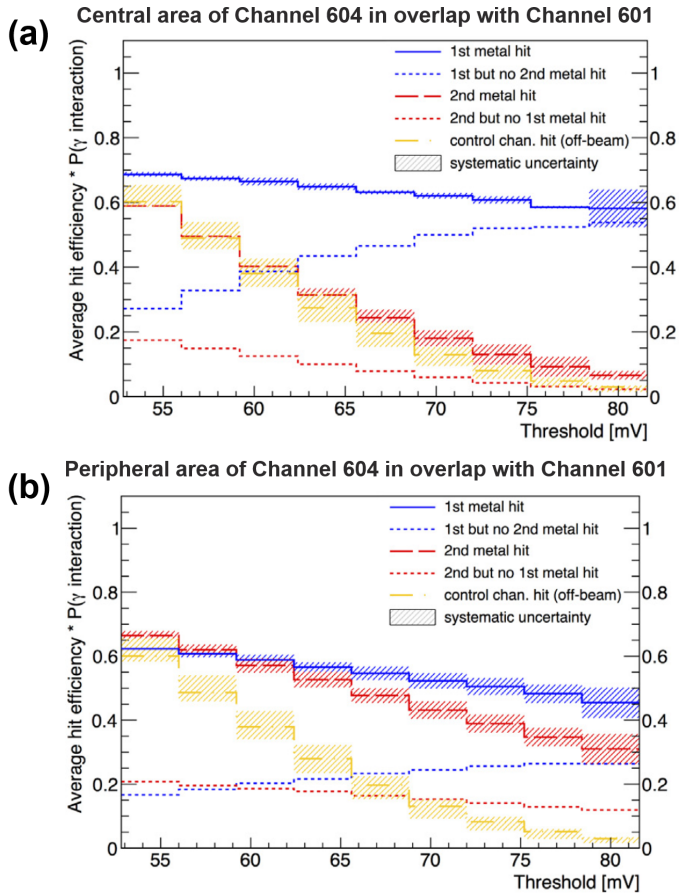


Fig. 6.33: Product of average hit efficiency and photon interaction probability for the response of a strip (solid blue line) and a pick-up channel (dashed red line) in a region where the EPA track of channel 601 overlaps with the central area of strip 604 (a) and with the peripheral area of strip 604 (b), along with their systematic uncertainties obtained from comparisons with overlap regions with different EPA tracks.

threshold and hit position dependences. Figure 6.33 shows the product of the average hit efficiency and the photon interaction probability determined over all beam positions belonging to the area under study. In the central area (Figure 6.33(a)) the response of channel 601, corresponding to the EPA (second metal), is in the order of the noise (yellow dashed line, corresponding to a channel far from the studied area) at low threshold, and similar to the strip response (first metal). However, the EPA response decreases rapidly with increasing threshold. On the other hand, in the peripheral area (Figure 6.33(b)) the EPA response is well above the noise, but also dependent on the threshold, although less pronounced.

Due to the limited testbeam time, the pick-up study was focused on the best conditions to detect the pick-up phenomena, using low thresholds for the study of the EPA structure with the highest density of EPA tracks (worst-case scenario). The results obtained hence

provide a qualitative insight in the behaviour of pick-up effect. It is expected that EPA structures with a lower density of channels, such as Basic or Rectangular-A, operating at a threshold of 100 mV can minimize the unwanted signal pick-up. Additionally, it is worth noting that pick-up can occur only in the regions covered by EPA tracks, that represent, for the Equalized structure, less than 8% of the total active area of the full-size ITk strip sensors with 4 strip rows, and less than 4% in sensors with 2 strip rows. Thus, even in the worst-case scenario, the pick-up effect would be very small in the actual large area sensor designs.

6.3.5 Signal Cross-talk

Similarly to the signal pick-up phenomena studied above, where the signal is directly coupled from the bulk, a coupling between the strip metal and the EPA track, so-called *cross-talk*, can also produce a loss of tracking efficiency on strip sensors with EPA structures implemented. With the objective to study this phenomenon, a testbeam was performed at Deutsches Elektronen-Synchrotron (DESY-Hamburg) [130] using an electron beam of 4.4 GeV. EPA structure Rectangular-B (10 μm track width) was selected for this study, as its EPA tracks partially run over the strips (Figure 4.24(e)) maximizing the possibilities to find cross-talk between both metals. The study was performed using an unirradiated sensor and a 10^{15} n_{eq}/cm^2 proton irradiated sensor, in order to evaluate the EPA performance at a fluence similar to the expected at the end of the HL-LHC lifetime. Similarly to the pick-up study, it should be mentioned that the analysis presented below was performed by the DESY-Zeuthen group in close collaboration with IMB-CNM.

Figure 6.34 shows the sensor area studied (blue box), partially including the area covered by the Rectangular-B EPA structure. All the results presented below were performed with the unirradiated and proton irradiated sensors fully depleted at 100 V and 300 V, respectively. The unirradiated sensor was kept at -10ºC during the experiment, and the proton irradiated sensor at -21ºC, both in a dry environment.

A cut-off was applied for the calculation of the efficiency, discarding events with a difference between the actual particle track and the hit recorded (*residual*, Figure 6.35) higher than 200 μm. Then, the number of hits fulfilling this condition was divided by the total number of tracks to obtain the tracking efficiency. Figure 6.36 presents the efficiencies calculated as a function of the threshold (*S-curve*), with a V_{t50} of 3.87 fC and 3.36 fC for the unirradiated sensor and for the proton irradiated one, respectively, and showing an efficiency decrease in the irradiated sensor.

In order to evaluate possible variations in efficiency induced by the EPA structure, efficiency maps were generated at a fixed threshold. Figure 6.37 presents the beam

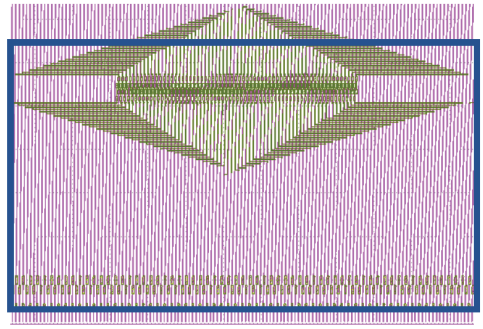


Fig. 6.34: Layout image of a strip sensor area with EPA structure Rectangular-B (10 μm track width) showing the area studied (blue box).

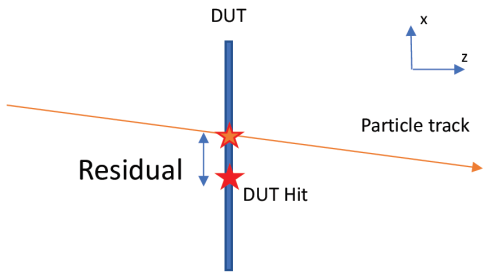


Fig. 6.35: Schematic representation of residual between track and strip (DUT) hit. Events with residual higher than 200 μm are discarded.

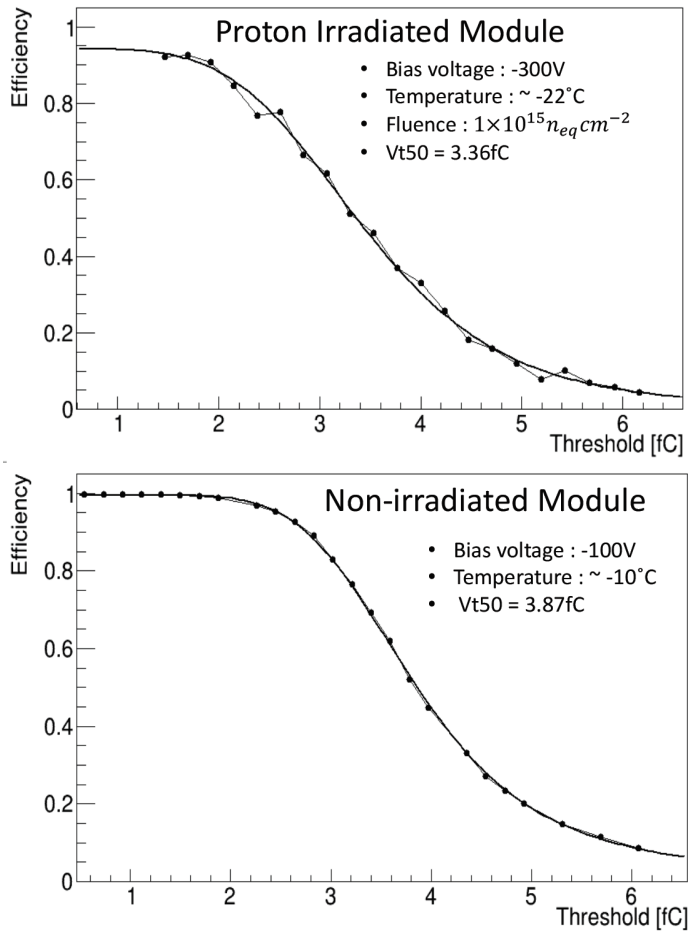


Fig. 6.36: Efficiency as a function of threshold (*S-curve*) of a sensor area with EPA structure Rectangular-B (10 μm track width) before (top) and after (bottom) 10^{15} n_{eq}/cm^2 proton fluence.

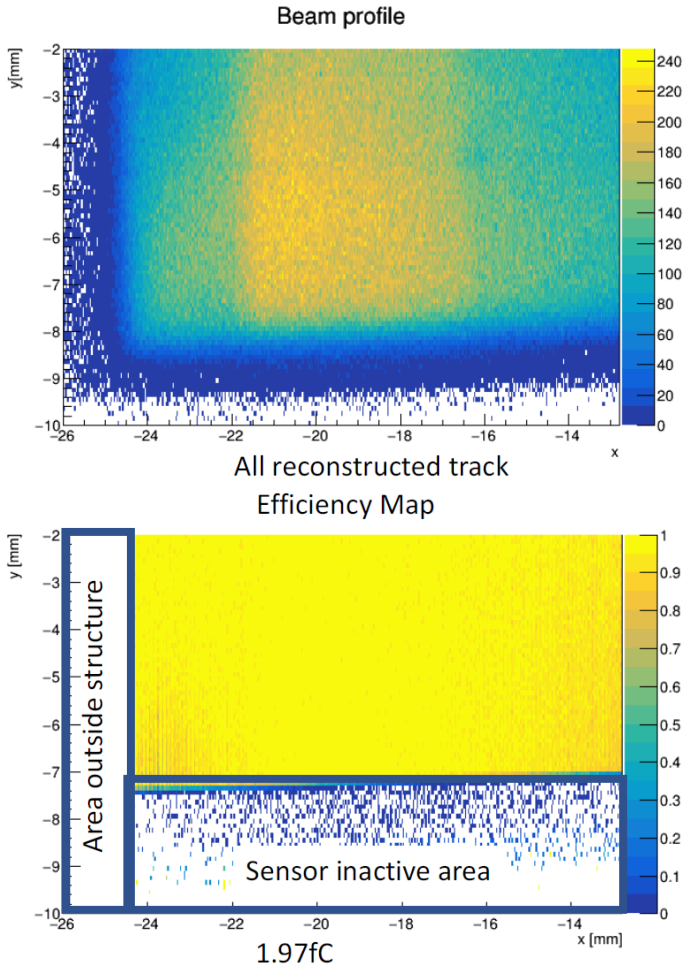


Fig. 6.37: Beam profile (top) and efficiency map (bottom) at a threshold of 1.97 fC of an unirradiated sensor area with EPA structure Rectangular-B (10 μm track width).

profile received by the unirradiated sensor (left) and the calculated efficiency map (right), showing no influence of the EPA structure. On the other hand, Figure 6.38 presents the results obtained for the irradiated sensor, presenting an efficiency loss in the area covered by the EPA structure. It is worth noting that the efficiency loss is observed in the regions where the EPA tracks run perpendicular to the strips and where the EPA pads (bonding pads) are located, so the signal loss can be attributed to a pick-up phenomena since this regions have low overlap between EPA tracks and strips (cross-talk).

To understand better how a particular channel lost part of its signal, reducing its efficiency, maps of track location when a single channel recorded a hit were also generated. Figure 6.39 presents track location maps, for the unirradiated (left) and irradiated (right) sensor, when the channel 35 records a hit. As can be seen, the

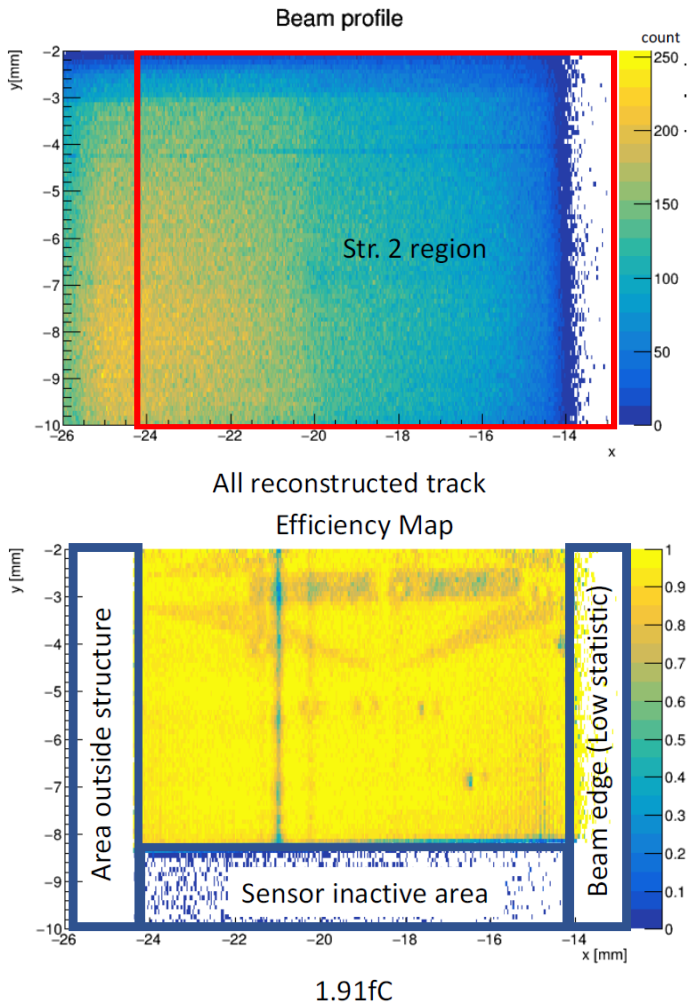


Fig. 6.38: Beam profile (top) and efficiency map (bottom) at a threshold of 1.91 fC of a 10^{15} n_{eq}/cm^2 proton irradiated sensor area with EPA structure Rectangular-B (10 μm track width).

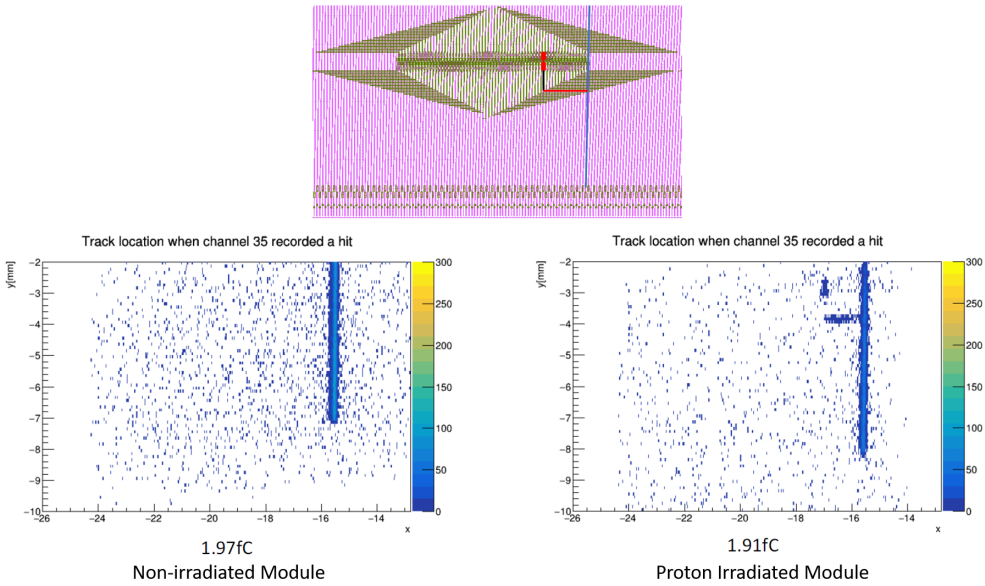


Fig. 6.39: Track position maps of an unirradiated (left) and 10^{15} n_{eq}/cm^2 proton irradiated (right) sensor area with EPA structure Rectangular-B (10 μm track width) when a signal in channel 35 is recorded. Upper layout image showing the sensor area studied, indicating the channel 35 (blue line), EPA track corresponding to channel 35 perpendicular to strips (red line) and on top of a strip (black line), and EPA pads (red boxes).

non-irradiated sensor shows signal only in the channel hit, without signs of signal coupling with the EPA tracks. On the other hand, in the irradiated sensor, the EPA track corresponding to the channel 35 presents signal at the region running perpendicular to the strips and at the EPA pads. Similarly to the observed in the efficiency maps, only the irradiated sensor presents a loss of signal, that could be associated to signal coupled by the EPA track directly from the bulk (pick-up), since the regions showing this behaviour only overlap partially with the strip metals, i.e. EPA tracks perpendicular to strips. In contrast, regions where the EPA track corresponding to the channel 35 overlap with a strip not hit do not present signal sharing, indicating that no cross-talk is produced.

6.4 Characterization of First IMB-CNM Strip Sensors Fabricated in 6-inch Wafers

As shown in Section 4.5.1, a test fabrication of strip sensors in 6-inch (150 mm) substrate wafers, called *Petalet150* prototype, was carried out for the first time at IMB-CNM, with the objective to test the capability of the institute to fabricate large area strip sensors. A total of ten 6-inch wafers were fabricated using 4-inch masks corresponding to the *Big sensor* of the End-cap Petalet prototype ([23], [135]) (Figure 4.30). Each

of these wafers contains one Big Sensor (trapezoidal shape with a total active area of 33.92 cm^2), three 1x1 cm^2 (die area) miniature sensors and several microelectronic test structures.

6.4.1 Devices Tested and Characterization Methods

For this first study, three of the ten wafers fabricated were selected and the leakage current was measured in all the devices. One wafer (W07) was fully diced and the complete characterization of the different inter-strip and single strip parameters was performed in one of the miniature sensors, testing 12 of the 128 strips available. All the tests were performed manually in a probe station, following the characterization methods used for the ATLAS Market Survey (see Figure 5.1), at 20ºC and in a dry environment. The results presented below correspond to this preliminary characterization. Further measurements are ongoing at IMB-CNM to increase statistics and to obtain definitive results and final conclusions. Moreover, it is worth mentioning that this first fabrication in 6-inch wafers with 4-inch photolithographic masks corresponds to a proof-of-concept experiment, with the objective to fabricate in the near future devices making use of the maximum area available in 6-inch wafers.

6.4.2 Global Performance Evaluation

Figure 6.40(a) shows the leakage current per unit area of the Big sensors and miniature sensors before dicing, using the test methods previously described in Section 2.4.1. Most of the devices present early breakdown voltages, especially the Big sensors (100 V), except the miniature sensor B2 from wafer 7 (W07) that presents a breakdown voltage around 700 V, fulfilling the ATLAS specifications. The premature breakdown voltage is currently being studied at IMB-CNM, performing new tests on more wafers of the same Petalet150 fabrication. Fortunately, the bulk capacitance measurements (Figure 6.40(b)) indicate that the full depletion voltage of these devices is 90 V, so all the devices can be tested fully depleted at a bias below the breakdown voltage. However, due to time constraints, only the miniature sensor showing better results (B2 from W07) was used for the inter-strip and single strip characterization.

6.4.3 Inter-strip Characterization

Figure 6.41 shows the results obtained for the main inter-strip parameters measured in a miniature sensor, using the test methods previously described in Section 2.4.2. The device presents a good isolation between strips, with an average inter-strip resistance value of 247.56 GΩ (Figures 6.41(a) and (b)) well above the minimum of 20 MΩ at 400 V established for the strip sensors in the ATLAS ITk (Table 5.1).

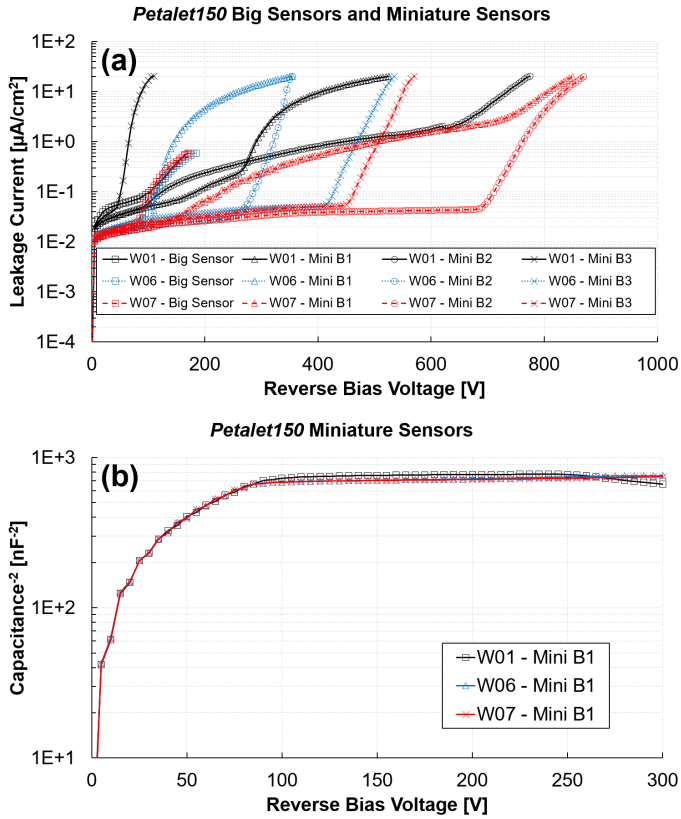


Fig. 6.40: Leakage current (a) and bulk capacitance (b) of prototype strip sensors (Petalet150) fabricated at IMB-CNM in 6-inch wafers.

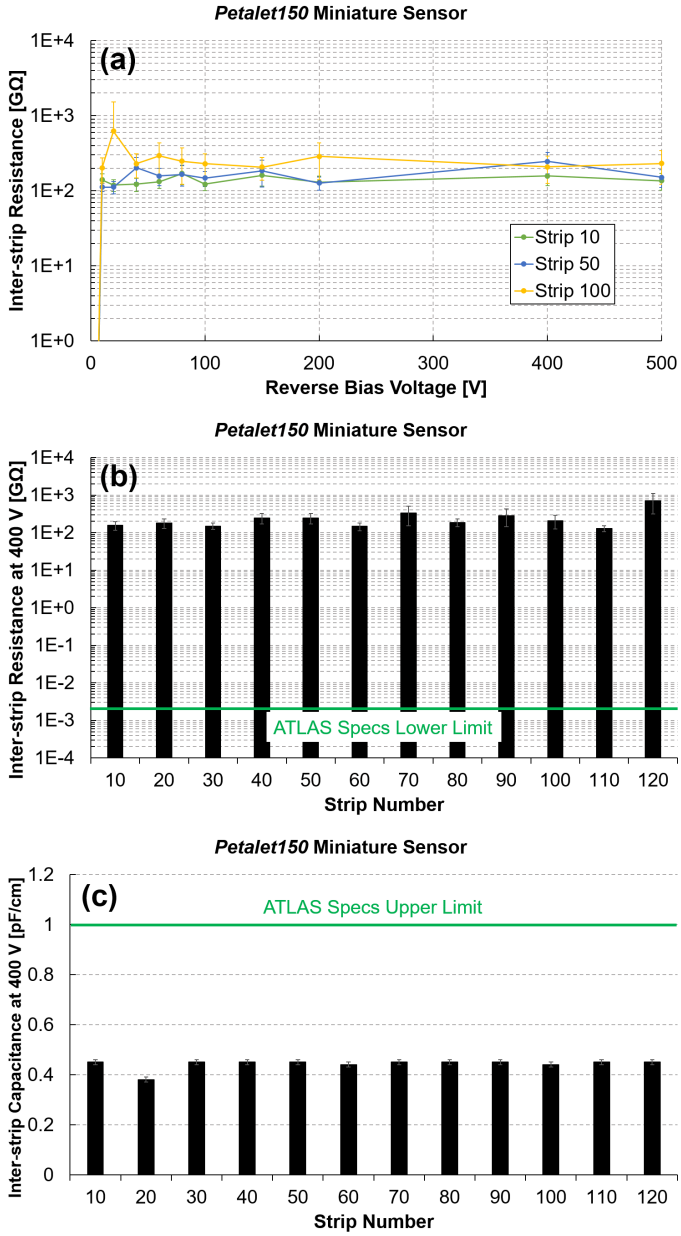


Fig. 6.41: Inter-strip resistance (a, b) and inter-strip capacitance (c) of a miniature strip sensor (Petalet150) fabricated at IMB-CNM in 6-inch wafers.

On the other hand, Figure 6.41(c) presents the values obtained for the inter-strip capacitance per strip length at 400 V, showing good uniformity between strips and also within the ATLAS specifications, with an average value of 0.44 pF/cm.

6.4.4 Single Strip Characterization

Similarly to the characterization carried out to evaluate the sensors from Infineon and Hamamatsu during the Market Survey (see Sections 2.4.3 and 5.1), four different tests were done to evaluate the performance of the single strips fabricated in 6-inch wafers at IMB-CNM. Figure 6.42 shows the results obtained for the characterization of the coupling capacitance, strip implant resistance, strip metal resistance and bias resistance. All these parameters show good uniformity between strips and are in agreement with the ITk specifications. However, it is worth mentioning that some of the strips present a metal resistance close to the upper limit of 30 Ω/cm. In consequence, the sheet resistance of the metal layer deposited in 6-inch wafers should be controlled in future fabrications.

Finally, a PTP characterization was also performed to evaluate the effective resistance present between the strip implant and the bias implant. In contrast to the ATLAS ITk strip sensors, the Petalet prototype sensors have a larger separation between the implants (70 μm), corresponding to the standard separation used in the previous generation of strip sensors currently installed in the ATLAS SCT, when punch-through protection was still not included. Figure 6.43 shows the strip current and the effective resistance measured in twelve strips, with the sensor fully depleted at 100 V. An average punch-through voltage of 31 V can be extracted from Figure 6.43(b) applying the condition R_{eff}=R_{bias}/2 to the Equation 2.5.

Table 6.4 summarizes the results obtained for the characterization of the first strip sensors fabricated in 6-inch wafers at the cleanroom of the IMB-CNM. Beside the premature breakdown voltages observed in most of the devices tested, all the parameters are in good agreement with the specifications established for the ATLAS ITk strip sensors, showing promising results for the fabrication of large area prototype strip sensors at IMB-CNM.

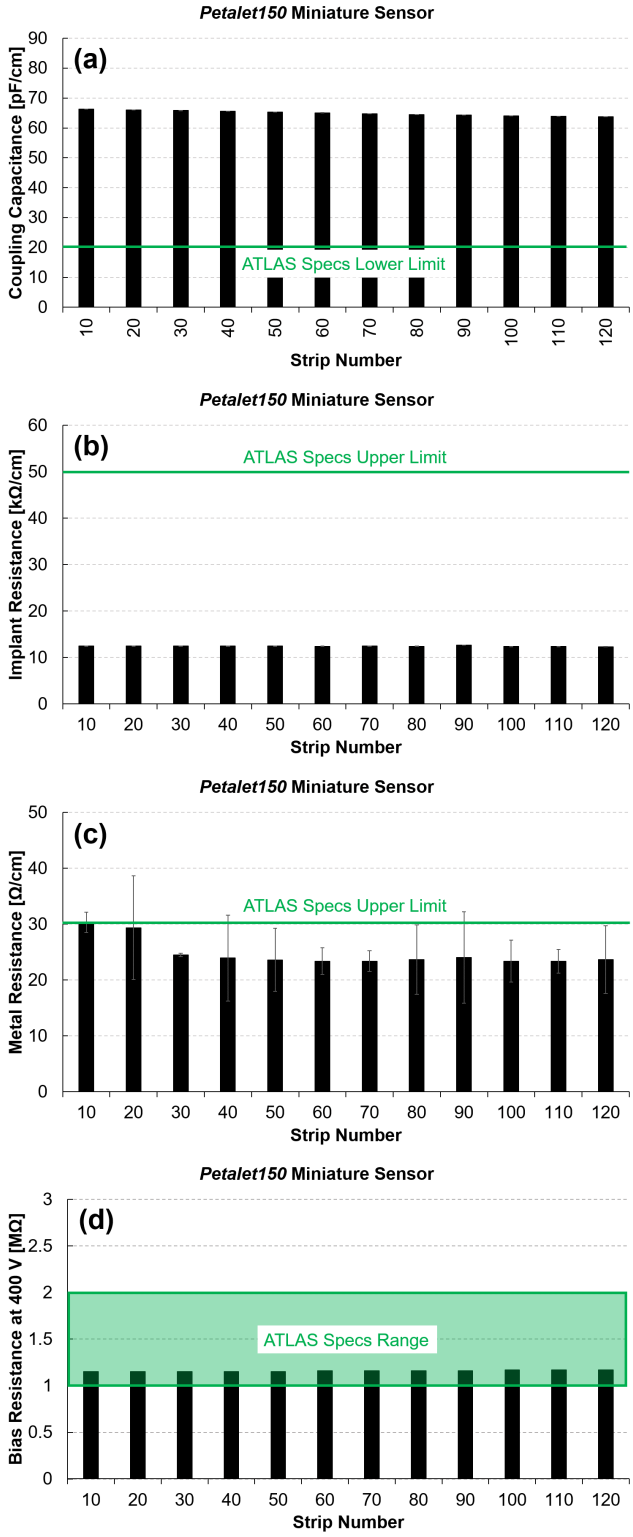


Fig. 6.42: Coupling capacitance (a), strip implant resistance (b), strip metal resistance (c) and bias resistance (d) of a miniature strip sensor (Petalet150) fabricated at IMB-CNM in 6-inch wafers.

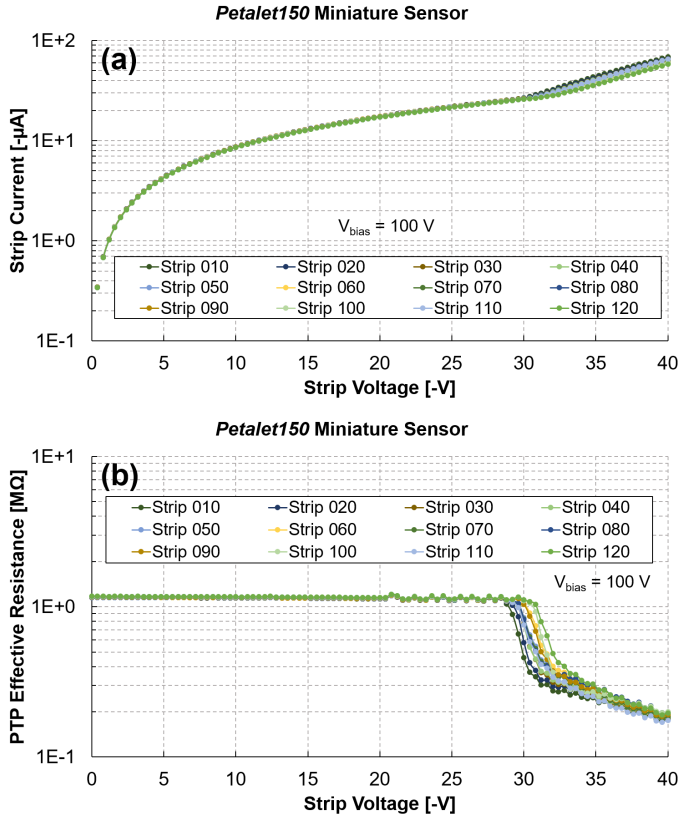


Fig. 6.43: Study of the punch-through performance of a miniature strip sensor (Petalet150) without PTP.

		ATLAS Specifications	IMB-CNM Petalet150 Miniature Sensor
Global Parameters	***Leakage Current*** ***($\mu A/cm^2$)***	<0.1 at 700 V (Pre-irrad) <100 at 700 V (Post-irrad)	0.06 at 700 V
	Breakdown Voltage ***(V)***	>700 (Pre-irrad) No Criteria (Post-irrad)	700
	Full Depletion Voltage ***(V)***	<330 (Pre-irrad) No Criteria (Post-irrad)	90
Inter-strip Parameters	***Inter-strip Capacitance*** ***(pF/cm)***	<1 at 300 V (Pre-irrad) <1 at 400 V (Post-irrad)	0.44
	Inter-strip Resistance ***(GΩ)***	$>1.5{\cdot}10^{-2}$ at 300 V (Pre-irrad) $>1.5{\cdot}10^{-2}$ at 400 V (Post-irrad)	247.56
Single Strip Parameters	***Coupling Capacitance*** ***(pF/cm)***	$\geq$ 20 (Pre-irrad) No Criteria (Post-irrad)	64.94
	Strip Implant Resistance ***(kΩ/cm)***	<50 (Pre-irrad) No Criteria (Post-irrad)	12.44
	Strip Metal Resistance ***(Ω/cm)***	<30 (Pre-irrad) No Criteria (Post-irrad)	24.71
	Bias Resistance ***(MΩ)***	1.5 ± 0.5 (Pre-irrad) 1.5 ± 0.5 (Post-irrad)	1.16
	Punch-through Voltage ***(V)***	No Criteria	31 (no PTP)

Tab. 6.4: Summary of the characterization performed on a miniature sensor from the first fabrication of strip sensors in 6-inch wafers at IMB-CNM, and comparison with the ATLAS specifications.

Conclusions

This thesis investigates the optimization and verification of a new generation of silicon strip sensors for the Inner-Tracker (ITk) of the ATLAS detector, able to withstand the severe operating conditions expected for the High-Luminosity Large Hadron Collider (HL-LHC) upgrade. Devices fabricated by Infineon Technologies AG, Hamamatsu Photonics K.K. and Centro Nacional de Microelectrónica (IMB-CNM) were studied before and after proton, neutron and gamma irradiation, contributing to the development of the new devices.

The layout design of the different elements was studied in detail, considering its impact on the device performance, proposing also a wide range of microelectronic test structures for the development phase of the technology and for the Quality Assurance (QA) during the forthcoming massive production. A new python-based Automatic Layout Generation Tool (ALGT) was developed to address the need for large area prototypes of strip detectors at the R&D stages of the ITk strip system upgrade. This versatile tool, able to efficiently design sensors with different dimensions and characteristics only modifying the input parameters, was used for the layout design of a full-size sensor, miniature sensors and test structures for the participation of Infineon in the ATLAS strip sensor Market Survey. The ALGT was also used to generate an initial layout design of the first 6-inch strip sensor adapted to the IMB-CNM design rules, based on a basic-principles study of the capability of the IMB-CNM cleanroom to fabricate large area strip detectors. In addition, several designs of Embedded Pitch Adapters (EPA) were presented with the aim to facilitate the connection of the readout electronics, minimizing the possible drawbacks associated with the introduction of a second metal layer in the device structure.

In the frame of the ATLAS strip sensor Market Survey, a complete characterization of devices fabricated by the two candidate foundries, Infineon and Hamamatsu, was carried out contributing to the performance evaluation of the prototype sensors fabricated by both companies to evaluate their capability to produce the strip sensors for the ITk upgrade. The large area sensors fabricated by Infineon, and designed with the ALGT, were irradiated with protons and neutrons, up to $5.1{\cdot}10^{14}$ n_{eq}/cm^2,

and extensively tested to evaluate their fulfillment of the requirements established by ATLAS. The prototype showed very good agreement with the ATLAS specifications, with only small deviations in the polysilicon bias resistance values, showing also promising results once assembled in a module. At this stage the technology was very close to be ready for the production of strip sensors for the ATLAS ITk. However, the management of Infineon Technologies AG decided, based on the business case, to discontinue the developments of strip sensors for HEP experiments. On the other hand, miniature sensors and diodes fabricated by Hamamatsu were irradiated with gammas, up to 70 Mrad, and characterized to evaluate their radiation hardness to the TID levels expected at the ATLAS ITk. In general terms, the results obtained fulfilled the requirements established by ATLAS. The characterization revealed values close to the limit for the voltage needed to fully deplete the devices, and an increase of the polysilicon bias resistance at the highest radiation fluences. However, besides these small deviations within the specifications, Hamamatsu passed the Market Survey evaluation, becoming the company in charge of the strip sensor production for the upgrade of the ATLAS ITk.

A characterization of the test structures designed for the development of strip sensor technologies, and fabricated by Infineon, was also carried out after proton and gamma irradiations up to $1.01{\cdot}10^{16}$ n_{eq}/cm^2 and 70 Mrad, respectively. The study of these structures allowed a deep investigation of specific device structures and technological parameters, such as the limits on the edge dimensions or the analysis of the surface currents on irradiated devices. In addition, a first study of the test structures designed for the QA during production, and fabricated by Hamamatsu, was presented. The characterization was carried out to validate the design and performance of the structures, and to help to establish some of the reference values to be used during production. The results obtained from the characterization of the test structures fabricated by both foundries were also compared with the ATLAS specifications, confirming the results of the Market Survey evaluation.

A set of additional studies and developments for the new generation of silicon strip detectors was also presented. A study was carried out on large area sensors, fabricated by Hamamatsu and Infineon, showing indications of breakdown voltage degradation in the presence of humidity. Several palliative treatments were attempted, observing a fast recovery of the breakdown voltage in dry atmosphere, and a clear improvement of the sensor performance at low humidity after baking or cleaning treatments. However, these treatments did not improve early breakdown voltages at high humidity. Thermal images of the large area sensors in breakdown conditions at high humidity revealed the presence of hotspots in the edge region of the devices. Possible mechanisms responsible of the humidity sensitivity were proposed, relating the separation between the guard ring and the edge ring metals, and the passivation thickness and conformity, with the appearance of premature reversible breakdown at high humidity. Several further

experimental and simulation studies are currently ongoing within the ITk collaboration to get deeper insight on these mechanisms of humidity sensitivity in the edge region of large area silicon sensors, in addition to possible mitigation techniques. ATLAS has established procedures in the sensor handling to keep low humidity conditions for reception, routine testing and storage during the production of the new ITk large area sensors, ensuring also the clean conditions during module and detector assembly, and minimizing the time the devices are biased while exposed to high/uncontrolled humidity.

A beam-loss scenario was recreated at the HiRadMat facility at CERN, focusing proton beams with different intensities directly on ATLAS-like strip sensors assembled in modules. Two different strip sensors fabricated by IMB-CNM were tested, one of them protected with PTP structure and a second one without protection. An initial characterization of the PTP structure verified its effectiveness to evacuate the current through the grounded bias rail when an excess voltage is developed at the strip coupling oxide. A comparative study of the readout chip noise and strip integrity indicated that all the strips protected with PTP effectively withstand the beam-loss experiment, but the readout chip channels were damaged. On the other hand, less than 40% of the strips without punch-through protection presented a functional performance after the experiment, but the readout chip appeared mostly unaltered. Hence, this study revealed that the PTP effectively protects strip sensors from the large amount of charge induced by a beam-loss, but the ABC130 readout electronics still might be damaged. This damage can be attributed to high voltages or charges reaching the front-end stage of the readout electronics through the wire-bonds and when the strip coupling capacitor is damaged. A new readout chip called ABCStar, with ESD protection at the input pads, is currently under evaluation and further beam-loss damage studies will be needed to evaluate the performance of the new ABCStar read-out chip wire-bonded to a PTP sensor.

A complete investigation of the Embedded Pitch Adapters (EPA) performance was also presented. The monitoring of the fabrication process revealed that the use of thick oxides between the strips and the EPA structures can compromise the fabrication process by increasing the sensor bowing. Inter-metal oxides with a thickness higher than 2 μm could induce a wafer bowing above the limit of 200 μm recommended by the ATLAS collaboration. On the other hand, an extensive characterization and analysis of the inter-strip capacitance considering all strip neighbours showed a clear dependence on the EPA design. In particular, minimum track widths and lengths, and maximum separation between tracks, can significantly reduce the total inter-strip capacitance along the EPA structure. In this sense, the designs called Basic and Rectangular-A provided the best response, showing also the lowest and least variable module noise. In addition, in order to evaluate the appearance of the unwanted bulk signal pick-up by the EPA structures, the Equalized structure with 20 μm track width was studied as

a 'worst-case' scenario. The study was carried out generating hitmaps using a micro-focused X-ray beam. The results obtained showed that a detectable amount of signal can be collected at the second metal by this structure at low thresholds, increasing the probability of fake signals in other channels and reducing the collection efficiency of the strip being hit. However, the structure studied can be considered the most favorable for a signal pick-up, due to the high area covered by the structure and its high density of EPA tracks, so this phenomena will be minimized with the use of Basic or Rectangular-A structures with 10 μm track width. Additionally, a clear reduction of the signal pick-up was observed for thresholds up to 80 mV, closer to the 100 mV used in working conditions. Finally, the fake signals induced by signal coupling between EPA tracks and strip metals, known as cross-talk, were also investigated. In this case, the Rectangular-B structure was selected as a 'worst-case' scenario for the appearance of cross-talk phenomena, since it is the structure with the highest overlap between strip and EPA metals. Two sensors were studied, one unirradiated and one irradiated with protons up to 10^{15} n_{eq}/cm^2, only showing indications of pick-up in the irradiated one, but no signs of cross-talk.

Finally, preliminary results obtained for the characterization of the first strip sensors fabricated in 6-inch wafers at the cleanroom of the IMB-CNM were also presented. Besides the premature breakdown voltages observed in the large devices tested, attributed to the unusual design of these sensors, the results obtained on standard miniature sensors show that all the characteristics were in good agreement with the specifications established for the ATLAS ITk strip sensors, showing promising results for the fabrication of large area prototype strip sensors at IMB-CNM.

Bibliography

[1] *The Large Hadron Collider*, 2020. [Online]. Available: https://home.cern/science/accelerators/large-hadron-collider.

[2] ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider", *Journal of Instrumentation*, vol. 3, S08003, 2008. DOI: 10.1088/1748-0221/3/08/S08003.

[3] CMS Collaboration, "The CMS experiment at the CERN LHC", *Journal of Instrumentation*, vol. 3, S08004, 2008. DOI: 10.1088/1748-0221/3/08/S08004.

[4] LHCb Collaboration, "LHCb detector performance", *International Journal of Modern Physics A*, vol. 7, p. 1 530 022, 2015. DOI: 10.1142/S0217751X15300227.

[5] ALICE Collaboration, "The ALICE experiment at the CERN LHC", *Journal of Instrumentation*, vol. 3, S08002, 2008. DOI: 10.1088/1748-0221/3/08/S08002.

[6] F. Kahlhoefer, "Review of LHC dark matter searches", *International Journal of Modern Physics A*, vol. 32, no. 13, p. 1 730 006, 2017. DOI: 10.1142/S0217751X1730006X.

[7] ATLAS Collaboration, "Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC", *Physics Letters B*, vol. 716, pp. 1–29, Aug. 2012. DOI: 10.1016/j.physletb.2012.08.020.

[8] CMS Collaboration, "Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC", *Physics Letters B*, vol. 716, pp. 30–61, Aug. 2012. DOI: 10.1016/j.physletb.2012.08.021.

[9] *The High-Luminosity Large Hadron Collider*, 2020. [Online]. Available: https://home.cern/science/accelerators/high-luminosity-lhc.

[10] ATLAS Collaboration, "Technical Design Report for the ATLAS Inner Tracker Strip Detector", CERN, Geneva, Tech. Rep. CERN-LHCC-2017-005. ATLAS-TDR-025, Apr. 2017. [Online]. Available: https://cds.cern.ch/record/2257755.

[11] *ATLAS Experiment*, 2020. [Online]. Available: https://atlas.cern/.

[12] E. Ros, "ATLAS inner detector", *Nuclear Physics B - Proceedings Supplements*, vol. 120, pp. 235–238, Jun. 2003. DOI: 10.1016/S0920-5632(03)01908-X.

[13] C. Gemme, "The ATLAS pixel detector", *Nuclear Instruments and Methods in Physics Research A*, vol. 501, pp. 87–92, Mar. 2003. DOI: 10.1016/S0168-9002(02)02015-6.

[14] Y. Unno, "ATLAS silicon microstrip Semiconductor Tracker (SCT)", *Nuclear Instruments and Methods in Physics Research A*, vol. 453, pp. 109–120, Oct. 2000. DOI: 10.1016/S0168-9002(00)00615-X.

[15] J.N. Jackson, "The ATLAS semiconductor tracker (SCT)", *Nuclear Instruments and Methods in Physics Research A*, vol. 541, pp. 89–95, Apr. 2005. DOI: 10.1016/j.nima.2005.01.043.

[16] ATLAS TRT Collaboration, "The ATLAS TRT Barrel Detector", *Journal of Instrumentation*, vol. 3, P02014, Feb. 2008. DOI: 10.1088/1748-0221/3/02/P02014.

[17] ATLAS TRT Collaboration, "The ATLAS TRT end-cap detectors", *Journal of Instrumentation*, vol. 3, P10003, Oct. 2008. DOI: 10.1088/1748-0221/3/10/P10003.

[18] ATLAS Collaboration, "Technical Design Report for the ATLAS Inner Tracker Pixel Detector", CERN, Geneva, Tech. Rep. CERN-LHCC-2017-021. ATLAS-TDR-030, Sep. 2017. [Online]. Available: https://cds.cern.ch/record/2285585.

[19] J.S. Keller, on behalf of the ATLAS Collaboration, "The ATLAS ITk strip detector system for the High Luminosity LHC upgrade", *Nuclear Instruments and Methods in Physics Research A*, vol. 958, p. 162 053, Apr. 2020. DOI: 10.1016/j.nima.2019.04.007.

[20] Y. Unno, A.A. Affolder, P.P. Allport, et al., "Development of n-on-p Silicon Sensors for Very High Radiation Environments", *Nuclear Instruments and Methods in Physics Research A*, vol. 636, S24–S30, Apr. 2011. DOI: 10.1016/j.nima.2010.04.080.

[21] J. Bohm, M. Mikestikova, A.A. Affolder, et al., "Evaluation of the bulk and strip characteristics of large area n-in-p silicon sensors intended for a very high radiation environment", *Nuclear Instruments and Methods in Physics Research A*, vol. 636, S104–S110, Apr. 2011. DOI: 10.1016/j.nima.2010.04.093.

[22] *Science and Technology Facilities Council (STFC) - Particle Physics Department*. [Online]. Available: https://www.ppd.stfc.ac.uk/.

[23] V. Benítez, M. Ullán, D. Quirion, et al., "Sensors for the End-cap prototype of the Inner Tracker in the ATLAS Detector Upgrade", *Nuclear Instruments and Methods in Physics Research A*, vol. 833, pp. 226–232, Oct. 2016. DOI: 10.1016/j.nima.2016.07.023.

[24] R. Mori, P.P. Allport, M. Baca, et al., "Evaluation of the performance of irradiated silicon strip sensors for the forward detector of the ATLAS inner tracker upgrade", *Nuclear Instruments and Methods in Physics Research A*, vol. 831, pp. 207–212, Sep. 2016. DOI: 10.1016/j.nima.2016.04.044.

[25] C. Lacasta, Y. Abo, A.A. Affolder, et al., "Design of the first full size ATLAS ITk strip sensor for the endcap region", *Nuclear Instruments and Methods in Physics Research A*, vol. 924, pp. 137–141, Apr. 2019. DOI: 10.1016/j.nima.2018.06.047.

[26] S. Sze and M.-K. Lee, *Semiconductor devices: physics and technology*, 3rd ed. Hoboken, NJ: John Wiley and Sons, 2012, ISBN: 978-0-470-53794-7.

[27] F. Hartmann, *Evolution of silicon sensor technology in particle physics*, 2nd ed. Berlin, Germany: Springer, 2009, ISBN: 978-3540250944.

[28] S. Franssila, *Introduction to Microfabrication*, 2nd ed. Wiley, 2010, ISBN: 978-0470749838.

[29] H. Spieler, *Semiconductor Detector Systems*, 1st ed. Oxford, UK: Oxford University Press, 2005, ISBN: 978-0198527848.

[30] *Medipix*, 2020. [Online]. Available: https://medipix.web.cern.ch/.

[31] G. Aad, M. Ackers, F.A. Alberti, et al., "ATLAS pixel detector electronics and sensors", *Journal of Instrumentation*, vol. 3, P07007, Jul. 2008. DOI: 10.1088/1748-0221/3/07/p07007.

[32] V.A.J. Van Lint, T.M. Flanagan, R.E. Leadon, et al., *Mechanisms of radiation effects in electronic materials*, 1st ed. Hoboken, NJ: Wiley, 1980, ISBN: 978-0471041061.

[33] M. Moll, "Displacement Damage in Silicon Detectors for High Energy Physics", *IEEE Transactions on Nuclear Science*, vol. 65, no. 8, pp. 1561–1582, Aug. 2018. DOI: 10.1109/TNS.2018.2819506.

[34] A. Vasilescu and G. Lindström, *Displacement damage in silicon (on-line compilation)*, 2000. [Online]. Available: https://rd50.web.cern.ch/NIEL/.

[35] M. Moll, "Radiation Damage in Silicon Particle Detectors: Microscopic Defects and Macroscopic Properties", Ph.D. dissertation, Universität Hamburg, 1999.

[36] M. Moll, E. Fretwurst, G. Lindström, et al., "Leakage current of hadron irradiated silicon detectors - material dependence", *Nuclear Instruments and Methods in Physics Research A*, vol. 426, pp. 87–93, Apr. 1999. DOI: 10.1016/S0168-9002(98)01475-2.

[37] A.G. Bates and M. Moll, "A comparison between irradiated magnetic Czochralski and float zone silicon detectors using the transient current technique", *Nuclear Instruments and Methods in Physics Research A*, vol. 555, pp. 113–124, Dec. 2005. DOI: 10.1016/j.nima.2005.09.020.

[38] G. Kramberger, V. Cindro, I. Mandić, et al., "Charge collection studies on custom silicon detectors irradiated up to $1.6{\cdot}10^{17}$ n_{eq}/cm^2", *Journal of Instrumentation*, vol. 8, P08004, Jul. 2013. DOI: 10.1088/1748-0221/8/08/P08004.

[39] M.S. Tyagi, "Zener and avalanche breakdown in silicon alloyed p-n junctions - II: Effect of temperature on the reverse characteristics and criteria for distinguishing between the two breakdown mechanisms", *Solid-State Electronics*, vol. 11, pp. 117–128, Jan. 1968. DOI: 10.1016/0038-1101(68)90142-1.

[40] M. Havránek, T. Hemperek, H. Krüger, et al., "DMAPS: a fully depleted monolithic active pixel sensor - analog performance characterization", *Journal of Instrumentation*, vol. 10, P02013–P02013, Feb. 2015. DOI: 10.1088/1748-0221/10/02/p02013.

[41] A. Chilingarov, "Recommendations towards a standardisation of the macroscopic parameter measurements", Tech. Rep., 2003. [Online]. Available: https://rd50.web.cern.ch/rd50/.

[42] C. Fleta, "Tecnología de detectores de partículas de silicio resistentes a la radiación", Ph.D. dissertation, Universitat Autònoma de Barcelona (UAB), Barcelona, Spain, 2006.

[43] H.F.-W. Sadrozinski, C. Betancourt, A. Bielecki, et al., "Punch-through protection of SSDs", *Nuclear Instruments and Methods in Physics Research A*, vol. 699, pp. 31–35, Jan. 2013. DOI: 10.1016/j.nima.2012.04.062.

[44] H.F.-W. Sadrozinski, C. Betancourt, A. Bielecki, et al., "Punch-through protection of SSDs in beam accidents", *Nuclear Instruments and Methods in Physics Research A*, vol. 658, pp. 46–50, Dec. 2011. DOI: 10.1016/j.nima.2011.06.085.

[45] R. Norman, J. Last and I. Haas, “Solid-state micrologic elements”, *1960 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, pp. 82–83, Feb. 1960. DOI: 10.1109/ISSCC.1960.1157264.

[46] E.R. Hnatek, “Semiconductor memories: A review”, *Microprocessors*, vol. 1, pp. 85–98, Dec. 1976. DOI: 10.1016/0308-5953(76)90002-7.

[47] Y. Wada and K. Uehara, “Optical Limitation in Fine Pattern Photolithography”, *Japanese Journal of Applied Physics*, vol. 13, Dec. 1974. DOI: 10.1143/JJAP.13.2014.

[48] D.A. McGillis and D.L. Fehrs, “Photolithographic linewidth control”, *IEEE Transactions on Electron Devices*, vol. 22, pp. 471–477, Jul. 1975. DOI: 10.1109/T-ED.1975.18164.

[49] Narayan and K. Lalit, *Computer Aided Design and Manufacturing*. Prentice Hall India Learning Private Limited, 2008, ISBN: 978-8120333420.

[50] S.M. Rubin, *Computer Aids for VLSI Design*. R.L. Ranch Press, 2009, ISBN: 978-0972751421.

[51] M. Ullán, “Desarrollo y optimización de tecnologías bipolares avanzadas y BiCMOS”, Ph.D. dissertation, Universitat Autònoma de Barcelona (UAB), Barcelona, Spain, 1998.

[52] T.P. Ma and Paul V. Dressendorfer, *Ionizing radiation effects in MOS devices and circuits*, 1st ed. John Wiley and Sons, 1989, ISBN: 978-0471848936.

[53] G. Pellegrini, C. Fleta, F. Campabadal, et al., “Technology of p-type microstrip detectors with radiation hard p-spray, p-stop and moderated p-spray insulations”, *Nuclear Instruments and Methods in Physics Research A*, vol. 579, pp. 599–603, Sep. 2007. DOI: 10.1016/j.nima.2007.05.253.

[54] G. Lutz, *Semiconductor Radiation Detectors*, 1st ed. Springer-Verlag Berlin Heidelberg, 2007, ISBN: 978-3540716785.

[55] S. Díez, “Radiation hardness studies of microelectronic technologies for the atlas upgrade detector”, Ph.D. dissertation, Universitat Autònoma de Barcelona, Barcelona, Spain, 2010.

[56] Y. Unno, S.O. Edwards, S. Pyatt, et al., “Development of n^+-in-p large-area silicon microstrip sensor for very high radiation environments - ATLAS12 design and initial results”, *Nuclear Instruments and Methods in Physics Research A*, vol. 765, pp. 80–90, Nov. 2014. DOI: 10.1016/j.nima.2014.06.086.

[57] J. Fernández-Tejero, C. Bertella, C. Escobar, et al., “Beam-loss Damage Experiment on ATLAS-like Silicon Strip Modules Using an Intense Proton Beam”, *Nuclear Instruments and Methods in Physics Research A*, vol. 958, p. 162 838, Apr. 2020. DOI: 10.1016/j.nima.2019.162838.

[58] DELPHI Collaboration, “The DELPHI detector at LEP”, *Nuclear Instruments and Methods in Physics Research A*, vol. 303, pp. 233–276, Jun. 1991. DOI: 10.1016/0168-9002(91)90793-P.

[59] CDF Collaboration, “The Collider Detector at Fermilab (CDF)”, *IEEE Transcations on Nuclear Science*, vol. 33, pp. 39–45, Feb. 1986. DOI: 10.1109/TNS.1986.4337044.

[60] V. Chabaud, P. Collins, H. Dijkstra, et al., “The DELPHI silicon strip microvertex detector with double sided readout”, *Nuclear Instruments and Methods in Physics Research A*, vol. 368, pp. 314–332, Jan. 1996. DOI: 10.1016/0168-9002(95)00699-0.

[61] D. Amidei, P. Azzi, N. Bacchetta, et al., "The Silicon Vertex Detector of the Collider Detector at Fermilab", *Nuclear Instruments and Methods in Physics Research A*, vol. 350, pp. 73–130, Oct. 1994. DOI: 10.1016/0168-9002(94)91156-8.

[62] U. Parzefall, "LHCb silicon: VELO and inner tracker", *Nuclear Physics B - Proceedings Supplements*, vol. 120, pp. 230–234, Jun. 2003. DOI: 10.1016/S0920-5632(03)01907-8.

[63] M. Ullán, V. Benítez, G. Pellegrini, et al., "Embedded Pitch Adapters for the ATLAS Tracker Upgrade", *Nuclear Instruments and Methods in Physics Research A*, vol. 732, pp. 178–181, Dec. 2013. DOI: 10.1016/j.nima.2013.07.078.

[64] W. de Boer, A. Dierlamm, F. Hartmann, et al., "A fourfold segmented silicon strip sensor with read-out at the edges", *Nuclear Instruments and Methods in Physics Research A*, vol. 788, pp. 154–160, Jul. 2015. DOI: 10.1016/j.nima.2015.03.082.

[65] LHCb Collaboration, "LHCb Tracker Upgrade Technical Design Report", CERN, Geneva, Tech. Rep. CERN-LHCC-2014-001. LHCB-TDR-015, Feb. 2014. [Online]. Available: https://cds.cern.ch/record/1647400.

[66] M. Artuso, C. Betancourt, I. Bezshyiko, et al., "Signal coupling to embedded pitch adapters in silicon sensors", *Nuclear Instruments and Methods in Physics Research A*, vol. 877, pp. 252–258, Jan. 2018. DOI: 10.1016/j.nima.2017.09.039.

[67] A. Collaboration, "Technical Specification for the Supply of ATLAS17LS Strip Sensors", Tech. Rep., 2017.

[68] Y. Unno, Y. Abo, A.A. Affolder, et al., "ATLAS17LS - a large-format prototype silicon strip sensor for long-strip barrel section of ATLAS ITk strip detector", Apr. 2020, Submitted to Nuclear Instruments and Methods in Physics Research A.

[69] J. Fernández-Tejero, M. Ullán, C. Fleta, et al., "Technological Solutions for Large Area Microstrip Radiation Silicon Sensors for the LHC Upgrade", *IEEE - 2017 Spanish Conference on Electron Devices (CDE)*, Jan. 2017.

[70] J. Fernández-Tejero, U. Bartl, M. Döcke, et al., "Design and Evaluation of Large Area Strip Sensor Prototypes for the ATLAS Inner Tracker Detector", 2020, Submitted to Nuclear Instruments and Methods in Physics Research A.

[71] *Peardrop Design Systems - GLADE*. [Online]. Available: https://peardrop.co.uk/.

[72] ATLAS and CMS Collaborations, "Market Survey. Technical Description. Planar Silicon Sensors for the ATLAS and CMS Outer Tracker Upgrades", Tech. Rep., 2016. [Online]. Available: http://cds.cern.ch/record/2145271.

[73] *Infineon Technologies AG*. [Online]. Available: https://www.infineon.com/.

[74] *Hamamatsu Photonics K.K.* [Online]. Available: https://www.hamamatsu.com/.

[75] K. Hara, A.A. Affolder, P.P. Allport, et al., "Testing of bulk radiation damage of n-in-p silicon sensors for very high radiation environments", *Nuclear Instruments and Methods in Physics Research A*, vol. 636, S83–S89, Apr. 2011. DOI: 10.1016/j.nima.2010.04.090.

[76] K. Hara, K. Inoue, A. Mochizuki, et al., "Development of Radiation Hard N^{+}-on-p Silicon Microstrip Sensors for Super LHC", *IEEE Transactions on Nuclear Science*, vol. 56, pp. 468–473, Apr. 2009. DOI: 10.1109/TNS.2009.2014162.

[77] J. Fernández-Tejero, V. Fadeyev, C. Fleta, et al., "Microelectronic Test Structures for the Development of a Strip Sensor Technology for High Energy Physics Experiments", *Nuclear Instruments and Methods in Physics Research A*, vol. 969, p. 163 971, Jul. 2020. DOI: 10.1016/j.nima.2020.163971.

[78] M. Bhushan and M.B. Ketchen, *Microelectronic Test Structures for CMOS Technology*. New York: Ed. Springer Business Media, 2011, ISBN: 978-1441993762.

[79] D.K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. New Jersey: John Wiley and Sons, 2006, ISBN: 978-0471739067.

[80] C. Becker, C. Gössling, C. Lichau, et al., "Gate-controlled diodes for characterization of the Si-SiO_2 interface with respect to surface effects of silicon detectors", *Nuclear Instruments and Methods in Physics Research A*, vol. 444, pp. 605–613, Apr. 2000. DOI: 10.1016/S0168-9002(99)01177-8.

[81] G. Verzellesi, G.-F. Dalla Betta, M. Boscardin, et al., "Extraction of bulk generation lifetime and surface generation velocity in high-resistivity silicon by means of gated diodes", *Nuclear Instruments and Methods in Physics Research A*, vol. 477, pp. 220–225, Jan. 2002. DOI: 10.1016/S0168-9002(01)01885-X.

[82] M. Ullán, P. Allport, K. Dette, et al., "Quality Assurance methodology for the ATLAS ITk Strip Sensor Production", Feb. 2020, Submitted to Nuclear Instruments and Methods in Physics Research A.

[83] A.H. Landzberg, *Microelectronics Manufacturing Diagnostics Handbook*, 1st ed. Springer-Verlag New York Inc., 1993, ISBN: 978-1-4613-5840-4.

[84] C.T. Klein, L.B.A. Hommels, V. Fadeyev, et al., "Initial Tests of Large Format Sensors for the ATLAS ITk Strip Tracker", Feb. 2020, Submitted to Nuclear Instruments and Methods in Physics Research A.

[85] M.G. Buehler and W.R. Thurber, "An Experimental Study of Various Cross Sheet Resistor Test Structures", *Journal of the Electrochemical Society*, vol. 125, pp. 645–650, Apr. 1978. DOI: 10.1149/1.2131516.

[86] W. Versnel, "Analysis of the Greek Cross, a Van der Pauw Structure with Finite Contacts", *Solid-State Electronics*, vol. 22, pp. 911–914, Nov. 1979. DOI: 10.1016/0038-1101(79)90061-3.

[87] M. Ullán, M. Lozano, F. Campabadal, et al., "Pitch adaptors of the ATLAS-SCT Endcap detector modules", *Journal of Instrumentation*, vol. 2, T10001, Oct. 2007. DOI: 10.1088/1748-0221/2/10/T10001.

[88] M. Ullán, M. Lozano, F. Campabadal and et al., "High-Pitch Metal-On-Glass Technology for Pad Pitch Adaptation Between Detectors and Readout Electronics", *IEEE Transactions on Nuclear Science*, vol. 51, pp. 968–974, Jul. 2004. DOI: 10.1109/TNS.2004.829365.

[89] A. Abdesselam, P.J. Adkin, P.P. Allport, et al., "The ATLAS semiconductor tracker end-cap module", *Nuclear Instruments and Methods in Physics Research A*, vol. 575, pp. 353–389, Jun. 2007. DOI: 10.1016/j.nima.2007.02.019.

[90] C. Lacasta, *Presentation at the ATLAS Upgrade Week (AUW)*, CERN, Switzerland, Feb 2009.

[91] M. Ullán, P.P. Allport, M. Baca, et al., "Embedded pitch adapters: A high-yield interconnection solution for strip sensors", *Nuclear Instruments and Methods in Physics Research A*, vol. 831, pp. 221–228, Sep. 2016. DOI: 10.1016/j.nima.2016.04.019.

[92] L. Rehnisch, I. Bloch, A. Blue, et al., "Testbeam studies on pick-up in sensors with embedded pitch adapters", *Nuclear Instruments and Methods in Physics Research A*, vol. 924, pp. 120–124, Apr. 2019. DOI: 10.1016/j.nima.2018.06.079.

[93] V. Benítez, "Design, fabrication and characterization of semiconductor radiation sensors for future high energy physics experiments", Ph.D. dissertation, Universitat Autònoma de Barcelona, Barcelona, Spain, 2018.

[94] W. Dabrowsky, et al., "Design and performance of the ABCN-25 readout chip for the ATLAS inner detector upgrade", *Nuclear Science Symposium (NSS-MIC)*, Oct. 2009.

[95] *Fondazione Bruno Kessler*, Via Sommarive, 18, 38123 Povo TN, Italy. [Online]. Available: https://www.fbk.eu/.

[96] *Cyclotron and Radioisotope Center (CYRIC)*, Tohoku University, Aramaki-Aoba 6-3, Aoba-ku, Sendai-shi 980-8578, Japan. [Online]. Available: https://www.cyric.tohoku.ac.jp/.

[97] B. Gkotse, M. Glaser, P. Lima, et al., "A New High-intensity Proton Irradiation Facility at the CERN PS East Area", *Proceedings of Science (Technology and Instrumentation in Particle Physics 2014)*, p. 354, Jun. 2014. DOI: 10.22323/1.213.0354.

[98] P. Dervan, R. French, P. Hodgson, et al., "The Birmingham Irradiation Facility", *Nuclear Instruments and Methods in Physics Research A*, pp. 101–104, Dec. 2013. DOI: 10.1016/j.nima.2013.05.156.

[99] *Reactor Infrastructure Centre, Institut Jožef Stefan (IJS)*, Jamova 39, 1000 Ljubljana, Slovenia. [Online]. Available: https://www.ijs.si/ijsw/JSI.

[100] B. Smodis and L. Snoj, "Utilization and Application of the Slovenian TRIGA Reactor", *Proceedings (International Conference on Research Reactors: Safe Management and Effective Utilization 2011)*, 2012.

[101] L. Barbot, C. Domergue, S. Bréaud, et al., "Neutron field characterization of irradiation locations applied to the slovenian TRIGA reactor", *Proceedings (3rd International Conference on Advancements in Nuclear Instrumentation, Measurements Methods and their Applications (ANIMMA) 2013)*, pp. 1–5, Jun. 2013. DOI: 10.1109/ANIMMA.2013.6727954.

[102] *60Co irradiation facility*, UJP Praha a.s. company, Prague, Czech Republic.

[103] L. Poley, C. Sawyer, S. Addepalli, et al., "The ABC130 barrel module prototyping programme for the ATLAS strip tracker", Jun. 2020, Submitted to Journal of Instrumentation.

[104] L. Poley, A. Blue, I. Bloch, et al., "Mapping the depleted area of silicon diodes using a micro-focused X-ray beam", *Journal of Instrumentation*, vol. 14, P03024, Mar. 2019. DOI: 10.1088/1748-0221/14/03/P03024.

[105] L. Poley, A.J. Blue, C. Buttar, et al., "Mapping the in-plane electric field inside irradiated diodes", Feb. 2020, Submitted to Nuclear Instruments and Methods in Physics Research A.

[106] J.M. Rafí, G. Pellegrini, D. Quirion, et al., "10 μm-thick four-quadrant transmissive silicon photodiodes for beam position monitor application: electrical characterization and gamma irradiation effects", *Journal of Instrumentation*, vol. 12, p. C01004, Jan. 2017. DOI: 10.1088/1748-0221/12/C01004.

[107] A.S. Grove and D.J. Fitzgerald, "Surface effects on p-n junctions: Characteristics of surface space-charge regions under non-equilibrium conditions", *Solid-State Electronics*, vol. 9, pp. 783–806, Aug. 1966. DOI: 10.1016/0038-1101(66)90118-3.

[108] A.S. Grove, *Physics and Technology of Semiconductor Devices*, 1st ed. New York: Wiley, 1967, ISBN: 978-0471329985.

[109] J. Fernández-Tejero, P.P. Allport, O. Aviñó, et al., "Humidity Sensitivity of Large Area Silicon Sensors: Study and Implications", Feb. 2020, Submitted to Nuclear Instruments and Methods in Physics Research A.

[110] C. Helling, P. Allport, A.A. Affolder, et al., "Strip Sensor Performance in Prototype Modules Built for ATLAS Inner-Tracker", Feb. 2020, Submitted to Nuclear Instruments and Methods in Physics Research A.

[111] M. Vellvehi, X. Perpiñà, J. León, et al., "Lock-in infrared thermography: a tool to locate and analyse failures in power devices", *IEEE - 2017 Spanish Conference on Electron Devices (CDE)*, pp. 1–4, 2017. DOI: 10.1109/CDE.2017.7905234.

[112] Y. Unno, Y. Ikegami, S. Terada, et al., "Development of n-in-p silicon planar pixel sensors for flip-chip modules for very high radiation environments", *Nuclear Instruments and Methods in Physics Research A*, vol. 650, pp. 129–135, Sep. 2011. DOI: 10.1016/j.nima.2010.12.191.

[113] C. Osburn, D. Ormond, et al., "Dielectric Breakdown in Silicon Dioxide Films on Silicon", *Journal of the Electrochemical Society: Solid-State Science and Technology*, vol. 119, pp. 591–597, May 1972. DOI: 10.1149/1.2404268.

[114] E.H. Nicollian and J.R. Brews, *MOS Physics and Technology*. New York: Wiley-Interscience, 1982, ISBN: 978-0471430797.

[115] W. Shockley, W.W. Hooper, H.J. Queisser, et al., "Mobile electric charges on insulating oxides with application to oxide covered silicon p-n junctions", *Surface Science*, vol. 2, pp. 277–287, 1964. DOI: 10.1016/0039-6028(64)90067-6.

[116] A. Andreazza, K. Einsweiler, C. Gemme, et al., "Effect of accidental beam losses on the ATLAS pixel detector", *Nuclear Instruments and Methods in Physics Research A*, vol. 565, pp. 50–54, Sep. 2006. DOI: 10.1016/j.nima.2006.04.086.

[117] J. Chu, G. Persky, S. Sze, et al., "Thermionic injection and space-charge-limited current in reach-through p^+np^+ structures", *Journal of Applied Physics*, vol. 43, p. 3510, Nov. 1972. DOI: 10.1063/1.1661745.

[118] J. Lohstroh, J. Koomen, A.V. Zanten, et al., "Punch-through currents in P^+NP^+ and N^+PN^+ sandwich structures", *Solid-State Electronics*, vol. 24, pp. 805–814, Sep. 1981. DOI: 10.1016/0038-1101(81)90095-2.

[119] K. Hara, T. Kuwano, G. Moorhead, et al., "Beam splash effects on ATLAS silicon microstrip detectors evaluated using 1-w Nd:YAG laser", *Nuclear Instruments and Methods in Physics Research A*, vol. 541, pp. 15–20, Apr. 2005. DOI: 10.1016/j.nima.2005.01.033.

[120] Y. Unno, S. Mitsui, R. Hori, et al., "Evaluation of test structures for the novel n^+-in-p pixel and strip sensors for very high radiation environments", *Nuclear Instruments and Methods in Physics Research A*, vol. 731, pp. 183–188, 2013. DOI: 10.1016/j.nima.2013.04.075.

[121] *The Super Proton Synchrotron (SPS)*, CERN. [Online]. Available: https://home.cern/science/accelerators/super-proton-synchrotron.

[122] M. Ullán, V. Benítez, D. Quirion, et al., "Low-resistance strip sensors for beam-loss event protection", *Nuclear Instruments and Methods in Physics Research A*, vol. 765, pp. 252–257, Nov. 2014. DOI: 10.1016/j.nima.2014.05.089.

[123] H. Gaillard, C. Theis, H. Vincke, et al., "HiRadMat: A New Irradiation Facility for Material Testing at CERN", Tech. Rep., 2011, pp. 1665–1667.

[124] E. Metral, S. Antipov, F. Antoniou, et al., "Update of the HL-LHC operational scenarios for proton operation", Tech. Rep., Jan. 2018. [Online]. Available: https://cds.cern.ch/record/2301292.

[125] L. Medina, R. Tomás, G. Arduini, et al., "Assessment of the performance of High-Luminosity LHC operational scenarios: integrated luminosity and effective pile-up density", *Canadian Journal of Physics*, vol. 97, pp. 498–508, Jul. 2018. DOI: 10.1139/cjp-2018-0291.

[126] C. Bertella, C. Escobar, J. Fernández-Tejero, et al., "Study of damages induced on ATLAS silicon by fast extracted and intense proton beam irradiation", *Proceedings of Science (The 27th International Workshop on Vertex Detectors - Vertex2018)*, vol. 348, 2019. DOI: 10.22323/1.348.0016.

[127] W. Lu, F. Anghinolfi, L. Cheng, et al., "Development of the ABCStar front-end chip for the ATLAS silicon strip upgrade", *Journal of Instrumentation*, vol. 12, p. C04017, Apr. 2017. DOI: 10.1088/1748-0221/12/04/C04017.

[128] ASTM F534-02a, *Standard test method for bow of silicon wafers*. West Conshohocken, PA: ASTM International, 2002. DOI: 10.1520/F0534-02A.

[129] S. Kuehn, V. Benítez, J. Fernández-Tejero, et al., "Prototyping of Hybrids and Modules for the Forward Silicon Strip Tracking Detector for the ATLAS Phase-II Upgrade", *Journal of Instrumentation*, vol. 12, May 2017. DOI: 10.1088/1748-0221/12/05/P05015.

[130] *Deutsches Elektronen-Synchrotron (DESY), German's national electron synchrotron facility*, Notkestrasse 85, 22607 Hamburg. Platanenallee 6, 15738 Zeuthen. Germany. [Online]. Available: https://www.desy.de/.

[131] D. Nelson, *HSIO development users guide*, 2010. [Online]. Available: http://www.slac.stanford.edu/djn/Atlas/hsio/.

[132] L. Eklund, et al., *ATLAS SCT Test DAQ Online Documentation*, 2002. [Online]. Available: http://scttestdaq.home.cern.ch/sct-testdaq/sctdaq/sctdaq.html.

[133] *Science and Technology Facilities Council (STFC) - Rutherford Appleton Laboratory (RAL)*, Harwell Campus, Didcot, OX11 0QX. [Online]. Available: https://stfc.ukri.org/about-us/where-we-work/rutherford-appleton-laboratory/.

[134] *Diamond Light Source, UK's national synchrotron light source science facility*, Diamond House, Harwell Science and Innovation Campus, Fermi Ave, Didcot OX11 0DE, United Kingdom. [Online]. Available: https://www.diamond.ac.uk/.

[135] S. Kuehn, V. Benítez, J. Fernández-Tejero, et al., "Prototyping of petalets for the Phase-II upgrade of the silicon strip tracking detector of the ATLAS experiment", *Journal of Instrumentation*, vol. 13, Jan. 2018. DOI: 10.1088/1748-0221/13/03/T03004.

List of Publications

- L.B.A. Hommels, P.P. Allport, M. Baca, et al., "Detailed studies of full-size ATLAS12 sensors", *Nuclear Instruments and Methods in Physics Research A*, vol. 831, pp. 167-173, March 2016.

- M. Ullán, P.P. Allport, M. Baca, et al., "Embedded pitch adapters: A high-yield interconnection solution for strip sensors", *Nuclear Instruments and Methods in Physics Research A*, vol. 831, pp. 221-228, April 2016.

- R. Mori, P.P. Allport, M. Baca, et al., "Evaluation of the performance of irradiated silicon strip sensors for the forward detector of the ATLAS Inner Tracker Upgrade", *Nuclear Instruments and Methods in Physics Research A*, vol. 831, pp.207-212, April 2016.

- L. Poley, A. Blue, R. Bates, et al., "Characterisation of strip silicon detectors for the ATLAS Phase-II Upgrade with a micro-focused X-ray beam", *Journal of Instrumentation*, vol. 11, p. P07023, June 2016.

- S. Kuehn, V. Benítez, J. Fernández-Tejero, et al., "Prototyping of Hybrids and Modules for the Forward Silicon Strip Tracking Detector for the ATLAS Phase-II Upgrade", *Journal of Instrumentation*, vol. 12, p. P05015, April 2017.

- S. Kuehn, V. Benítez, J. Fernández-Tejero, et al., "Prototyping of Petalets for the Phase-II Upgrade of the Silicon Strip Tracking Detector of the ATLAS Experiment", *Journal of Instrumentation*, vol. 13, p. T03004, January 2018.

- L. Rehnisch, I. Bloch, A. Blue, et al., "Testbeam Studies on Pick-up in Sensors with Embedded Pitch Adapters", *Nuclear Instruments and Methods in Physics Research A*, vol. 924, pp. 120-124, June 2018.

- R.F.H. Hunter, S.H. Abidi, A.A. Affolder, et al., "First Bulk and Surface Results for the ATLAS ITk Strip Stereo Annulus Sensors", *Nuclear Instruments and Methods in Physics Research A*, vol. 924, pp. 142-146, August 2018.

- A. Blue, A.A. Affolder, X. Ai, et al. "Test-beam Evaluation of Silicon Strip Modules for ATLAS Phase-II Strip Tracker Upgrade", *Nuclear Instruments and Methods in Physics Research A*, vol. 924, pp. 108-111, September 2018.

- L. Poley, A. Blue, I. Bloch, et al., "Mapping the Depleted Area of Silicon Diodes Using a Micro-focused X-ray Beam", *Journal of Instrumentation*, vol. 14, p. P03024, March 2019.

- C. Bertella, C. Escobar, J. Fernández-Tejero, et al., "Damages Induced on ATLAS IBL Modules by Fast Extracted and Intense Proton Beam Irradiation", *Journal of Instrumentation*, vol. 14, p. C05024, May 2019.

- C. Bertella, C. Escobar, J. Fernández-Tejero, et al., "Study of Damages Induced on ATLAS Silicon by Fast Extracted and Intense Proton Beam Irradiation", *Proceedings of Science*, vol. 016, 2019.

- J. Fernández-Tejero, C. Bertella, C. Escobar, et al., "Beam-Loss Damage Experiment on ATLAS-like Silicon Strip Modules Using an Intense Proton Beam", *Nuclear Instruments and Methods in Physics Research A*, vol. 958, p. 162838, September 2019.

- J. Fernández-Tejero, V. Fadeyev, C. Fleta, et al., "Microelectronic Test Structures for the Development of a Strip Sensor Technology for High Energy Physics Experiments", *Nuclear Instruments and Methods in Physics Research A*, vol. 969, p. 163971, April 2020.

- M. Mikestikova, J. Kroll, S.H. Abidi, et al., "Electrical Characterization of Surface Properties of the ATLAS17LS Sensors after Neutron, Proton and Gamma Irradiation", *Submitted to Nuclear Instruments and Methods in Physics Research A*, February 2020.

- L. Poley, A. Blue, C. Buttar, et al., "Mapping the In-plane Electric Field Inside Irradiated Diodes", *Submitted to Nuclear Instruments and Methods in Physics Research A*, February 2020.

- Y. Unno, Y. Abo, A.A. Affolder, et al., "ATLAS17LS – A Large-format Prototype Silicon Strip Sensor for Long-strip Barrel Section of ATLAS ITk Strip Detector", *Submitted to Nuclear Instruments and Methods in Physics Research A*, February 2020.

- M. Ullán, P.P. Allport, K. Dette, et al., "Quality Assurance Methodology for the ATLAS ITk Strip Sensor Production", *Submitted to Nuclear Instruments and Methods in Physics Research A*, February 2020.

- J. Fernández-Tejero, U. Bartl, M. Döcke, et al., "Evaluation of Large Area Strip Sensor Prototypes for the ATLAS Inner Tracker Detector", *Submitted to Nuclear Instruments and Methods in Physics Research A*, February 2020.

- J. Fernández-Tejero, P.P. Allport, O. Aviñó, et al., "Humidity Sensitivity of Large Area Silicon Sensors: Study and Implications", *Submitted to Nuclear Instruments and Methods in Physics Research A*, February 2020.

- L. Poley, C. Sawyer, S. Addepalli, et al., "The ABC130 Barrel Module Prototyping Programme for the ATLAS Strip Tracker", *Submitted to Journal of Instrumentation*, June 2020.

List of Conferences

- Inner Tracker (ITk) Week, Oral contribution (co-author), CERN, Geneva (Switzerland), September 2015.

- ATLAS Upgrade Week (AUW), Oral contribution (co-author), CERN, Geneva (Switzerland), November 2015.

- 2^{nd} Scientific Meeting of Barcelona Nanotechnology Cluster (BNC-b) Students, Poster contribution, Universitat Autònoma de Barcelona (UAB), Barcelona (Spain), June 2016.

- Inner Tracker (ITk) Week, Oral contribution (co-author), CERN, Geneva (Switzerland), February 2016.

- Inner Tracker (ITk) Week, Oral contribution (co-author), Institut de Física Corpuscular (IFIC), Valencia (Spain), September 2016.

- ATLAS Upgrade Week (AUW), Oral contribution (co-author), CERN, Geneva (Switzerland), November 2016.

- 11^{th} Spanish Conference on Electronic Devices, Oral contribution, Universitat de Barcelona (UB), Barcelona (Spain), February 2017.

- ATLAS Upgrade Week (AUW), Oral contribution (co-author), CERN, Geneva (Switzerland), March 2017.

- Inner Tracker (ITk) Week, Oral contribution, CERN, Geneva (Switzerland), June 2017.

- ATLAS Upgrade Week (AUW), Oral contribution, CERN, Geneva (Switzerland), November 2017.

- Inner Tracker (ITk) Week, Oral contribution, CERN, Geneva (Switzerland), February 2018.

- ATLAS Upgrade Week (AUW), Oral contribution (co-author), CERN, Geneva (Switzerland), April 2018.

- Inner Tracker (ITk) Week, Oral contribution (co-author), University of Oxford, Oxford (England), September 2018.

- ATLAS Upgrade Week (AUW), Oral contribution, CERN, Geneva (Switzerland), November 2018.

- 12^{th} Spanish Conference on Electronic Devices, Oral contribution, Universidad de Salamanca (USAL), Salamanca (Spain), November 2018.

- 15^{th} Vienna Conference on Instrumentation, Poster contribution, Technische Universität Wien (TU Wien), Vienna (Austria), February 2019.

- 14^{th} Trento Workshop on Advanced Silicon Radiation Detectors, Oral contribution, Fondazione Bruno Kessler (FBK), Trento (Italy), February 2019.

- ATLAS Upgrade Week (AUW), Oral contribution, CERN, Geneva (Switzerland), April 2019.

- Final Design Review (FDR) of the ATLAS Inner Tracker Strip Sensors, Oral contribution, CERN, Geneva (Switzerland), April 2019.

- 12^{th} International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors, Oral contribution, International Conference Center Hiroshima (ICCH), Hiroshima (Japan), December 2019.

List of Figures

List of Tables