

PhD Dissertation



International Doctorate School in Information and
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DISI - University of Trento

DEVELOPMENT OF ENHANCED DOUBLE-SIDED
3D RADIATION SENSORS FOR
PIXEL DETECTOR UPGRADES AT HL-LHC

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Abstract

The upgrades of High Energy Physics (HEP) experiments at the Large Hadron Collider (LHC) will call for new radiation hard technologies to be applied in the next generations of tracking devices that will be required to withstand extremely high radiation doses. In this sense, one of the most promising approaches to silicon detectors, is the so called 3D technology. This technology realizes columnar electrodes penetrating vertically into the silicon bulk thus decoupling the active volume from the inter-electrode distance. 3D detectors were first proposed by S. Parker and collaborators in the mid '90s as a new sensor geometry intended to mitigate the effects of radiation damage in silicon. 3D sensors are currently attracting growing interest in the field of High Energy Physics, despite their more complex and expensive fabrication, because of the much lower operating voltages and enhanced radiation hardness. 3D technology was also investigated in other laboratories, with the intent of reducing the fabrication complexity and aiming at medium volume sensor production in view of the first upgrades of the LHC experiments. This work will describe all the efforts in design, fabrication and characterization of 3D detectors produced at FBK for the ATLAS Insertable B-Layer, in the framework of the ATLAS 3D sensor collaboration. In addition, the design and preliminary characterization of a new batch of 3D sensor will also be described together with new applications of 3D technology.

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Keywords

[3D detectors, ATLAS IBL, TCAD simulations, Device characterization]

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Chapter 1

High Energy Physics at LHC

1.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is currently the largest and most powerful particle accelerator in the world. It was built at CERN between 1998 and 2008 and its primary objectives are the discovery of the Higgs boson and other particles predicted by supersymmetric theories. The accelerator is a two-ring superconducting proton-proton collider placed inside a 27 km long, 3.8 meters wide underground tunnel, formerly used by the Large Electron-Positron collider (LEP) [1, 2]. The machine is built at a depth between 50 and 175 meters beneath the French-Swiss border near Geneva, Switzerland.

The LHC is designed with two operating modes in mind: the first mode is the proton-proton collision delivering unprecedented luminosity ($10^{34} \text{ cm}^{-2}\text{s}^{-1}$) and energy in the center of mass equal to 14 TeV; the second operating mode allows the LHC to collide lead ions (Pb-Pb) with center-of-mass energy of 1150 TeV. The particle beams are not continuous but in bunches with a repetition rate never shorter than 25 ns. The total number of events per second generated by the beam collisions for a given process can be calculated as:

$$N = L\sigma \tag{1.1}$$

where σ is the cross-section for the examined process and L is the luminosity. When looking for very rare events, like the Higgs boson, the luminosity must be very high in order to increase the probability of generating such events. The luminosity only depends on beam parameters and, for a gaussian beam profile, can be written as:

$$L = \frac{N_b^2 n f_r \gamma}{4\pi \varepsilon_n \beta^*} \tag{1.2}$$

where N_b is the number of particles per bunch, n is the number of bunches per beam, f_r is the revolution frequency (11.245 kHz), γ the relativistic γ factor, ε_n the normalized

transverse emittance and β^* the β function at the collision point.

Prior to being injected into the main ring, particles are accelerated in successive steps. In the very beginning the Linear Particle Accelerator (LINAC2) generates 50 MeV protons and feeds them to the Proton Synchrotron Booster (PSB) which accelerates them to an energy of 1.4 GeV. Next, the particles are injected into the Proton Synchrotron (PS) where they reach an energy of 26 GeV. The last acceleration stage is the Super Proton Synchrotron (SPS) which accelerates the protons at 450 GeV before injecting them into the LHC where their energy can be increased up to a peak of 7 TeV.

The basic layout of the LHC follows the LEP geometry and is shown in Fig.1.1. The machine has eight arcs and eight straight sections, four of the straight sections host the LHC experiments whilst the other four are used for auxiliary services and beam abort. Two of the straight sections, diametrically opposed one to the other, house the two general purpose experiments: the ATLAS detector is located at point 1 and the CMS detector is located at point 5 also incorporating the TOTEM experiment. The other two experiments, ALICE and LHCb, are placed at point 2 and point 8 respectively (see Fig.1.1 for more details). The ring is composed by 1232 dipole magnets used to maintain particles in a circular path and by 392 quadrupole magnets used for focusing the beam thus increasing the chances of particle interaction in the four intersection points, a picture of one of the

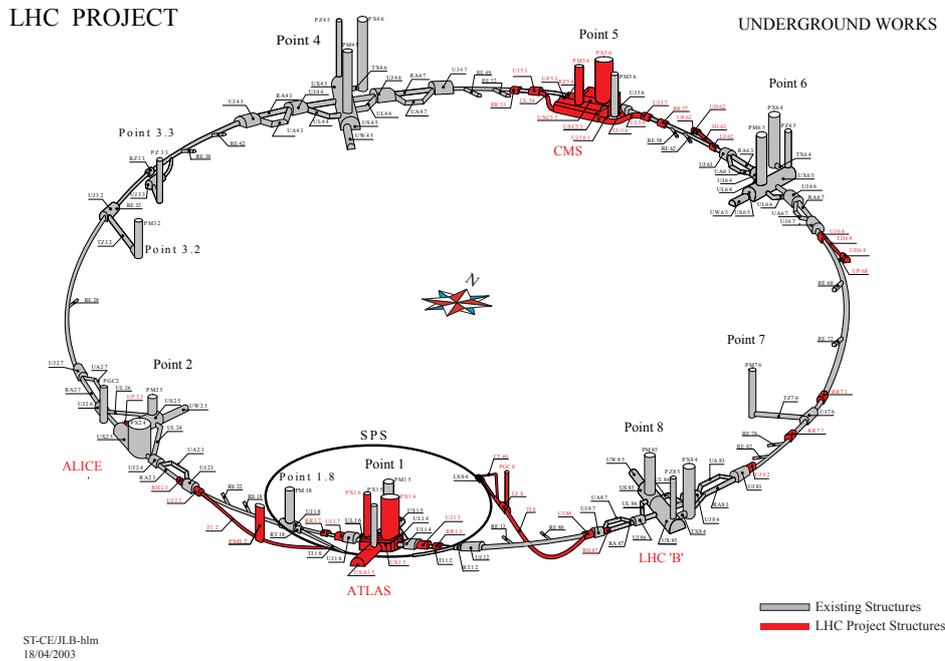


Figure 1.1: The layout of the Large Hadron Collider. Newer structures are represented in red while older structures are represented in grey.



Figure 1.2: Superconducting dipole magnets of the Large Hadron Collider. (CERN-AC-0911188 ©CERN)

dipole magnets if shown in Fig.1.2. A total of more than 7000 superconducting magnets are installed at LHC, they are operated at temperatures in the order of 1.9°K (-271.25°C) and are cooled with superfluid helium.

1.2 Brief history of the LHC

The Large Hadron Collider project was approved by CERN Council in December 1994. The project was initially split in two parts: the accelerator was going to be built with a maximum energy in the center of mass of 10 TeV and a later upgrade was going to increase its energy to 14 TeV. However, after some discussions, in December 1996 CERN Council passed a resolution approving the immediate construction of a 14 TeV accelerator. The construction started in 1998 and ended in 2008, when the first beam circulated the LHC on the morning of September the 10th 2008.

On September 19th 2008, a magnet quench occurred in about 100 bending magnets causing a loss of approximately 6 tonnes of liquid helium and also breaking the vacuum condition of the beam pipe. After some investigations, it was understood that the cause of the incident was a faulty electrical connection between a dipole and a quadrupole magnets resulting in mechanical damage and release of helium from the magnet cold mass into the tunnel [3].

The first modest high-energy collisions (900 GeV) at LHC were planned for the end

of September 2008 and the accelerator was expected to be operating at 10 TeV by the end of 2008 but, due to the delay caused by the incident, it was not possible to operate the accelerator safely until November 2009 when the first low-energy beams were circulated in the tunnel. On November 30th 2009 the LHC reached an energy of 1.18 TeV per beam becoming the world's highest-energy particle accelerator, beating Tevatron's previous record of 0.98 TeV per beam.

During 2010 the energy of the beams was gradually increased up to 3.5 TeV achieved on March 30th 2010, setting a new energy record and marking the official start of the LHC physics program. The proton-proton collision recorder during the first two years of the LHC operation led, on July 4th 2012, to the announcement from both ATLAS and CMS of the discovery of a boson in the mass range around 125-126 GeV, with statistical significance of 5σ consistent with the prediction of the standard model for the Higgs boson.

In order to run in full safety, the LHC will be operated at 3.5 TeV per beam until the end of 2012. In 2013 the LHC will undergo a long shutdown to allow for small upgrades and consolidations in preparation of the high-energy runs starting in 2014.

1.2.1 Planned machine upgrades

The LHC is now running at roughly half its designed energy, this was a conservative choice taken after detecting the cause of the 2008 incident. In order to reach full performance with the current machine, some upgrades will be necessary. Moreover, an increase of the nominal luminosity of the LHC is already planned, and both the accelerator and the experiments will require several major upgrades.

The milestones for the machine and experiment upgrades were set during the "LHC Performance Workshop" in Chamonix 2012 [4]. The LHC upgrade is currently planned and organized in three phases:

- LHC Phase-0: maximum performance without any hardware changes;
- LHC Phase-1: maximum performance keeping the LHC arcs unchanged;
- LHC Phase-2: maximum performance after "major" hardware changes.

The Phase-0 upgrade is planned during the first long shutdown from the beginning of 2013 to the end of 2014. The machine will be optimized to reach nominal luminosity ($\sqrt{s}=13\text{-}14$ TeV, $L=1\times 10^{34}$ $\text{cm}^{-2}\text{s}^{-1}$, with 25 ns bunch spacing), the main activities that will be performed regard the consolidation of the superconducting circuit which was the cause of the 2008 incident along with many other improvements and maintenance tasks. Experiments will install new components that were already approved in order to be ready to run at nominal energy by the end of 2014.

The second long shutdown is planned in 2017-2018 when Phase-1 upgrades will be performed: the areas that will see most of the upgrades are the injectors allowing to reach

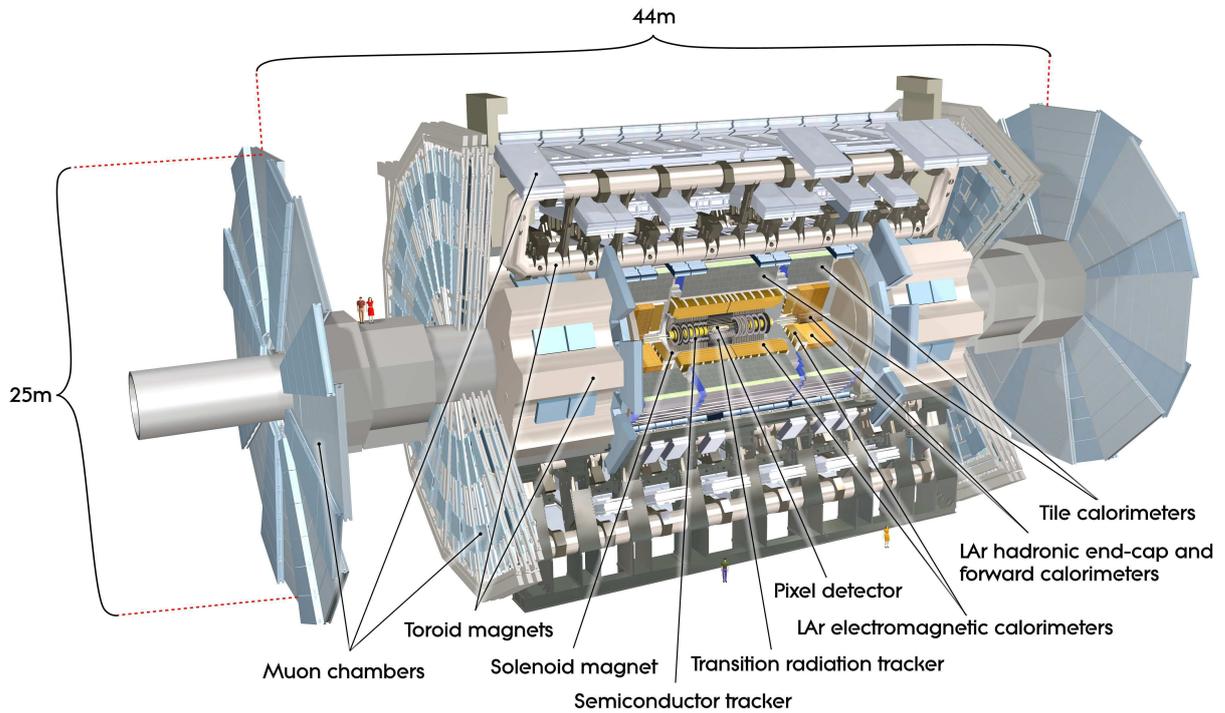


Figure 1.3: Sketch of the ATLAS particle detector. (CERN-GE-0803012 01)

full design luminosity ($\sqrt{s}=14$ TeV, $L=2\times 10^{34}$ $\text{cm}^{-2}\text{s}^{-1}$, with 25 ns bunch spacing).

The High Luminosity LHC (HL-LHC) is currently planned for 2022 and is referred to as Phase-2 upgrade. Many hardware upgrades will be required in order to go beyond design luminosity and reach $L=5\times 10^{34}$ $\text{cm}^{-2}\text{s}^{-1}$ while maintaining the same energy in the center of mass (14 TeV).

1.3 The ATLAS Experiment

ATLAS (A Toroidal LHC ApparatuS) is one of the general-purpose particle detectors built at the Large Hadron Collider (LHC). The experiment will take advantage of the unprecedented high energy and luminosity of the LHC to reach many objectives, spanning between the discovery of new particles, the confirmation of current theories and the discovery of new physics models. The most famous of these objectives is, of course, the discovery of the Higgs Boson.

The ATLAS experiment involves an incredible amount of institutes, physicists and engineers from all over the world. The detector itself is an incredibly complex machine: being 45 meters long, 25 meters in diameter and weighing about 7,000 tons, is one of the largest particle experiments ever built. ATLAS is composed by many layers, each of

which has a very specific task. The most important layers will be briefly described in the following pages with special regard to the inner detector, the silicon tracker. Additional details about the ATLAS experiment and all its components can be found in references [5] and [6].

1.3.1 Structure of the ATLAS experiment

This section briefly describes the different layers composing the ATLAS experiment. The description is performed from the inside out (inner layers first), and each layer is shown in Fig.1.3. Since the focus of this thesis is on silicon detectors, the Pixel Detector and the Semi-Conductor Tracker deserve their own sections and will be more carefully described in Sections 1.3.2 and 1.3.3.

Inner detector

The entire inner detector is surrounded by a strong magnetic field which causes the track of charged particles to bend. The direction of this curvature reveals the charge of the particle (positive or negative) and the curvature degree returns the momentum of the observed particle. The main objective of the inner detector is tracking charged particles exiting the interaction point after a collision has occurred. Different sensor topologies are combined inside the inner detector: (i) the Pixel Detector, located very close to the beam pipe, (ii) the Semi-Conductor Tracker (SCT), at an intermediated distance from the interaction point and (iii) the Transition Radiation Tracker (TRT) which is the outermost layer of the inner detector (details on the disposition of the different layers are shown in Fig.1.4(a) and Fig.1.4(b)).

The Transition Radiation Tracker (TRT) [7] consists of a central TRT Barrel and forward and backward TRT End-caps. The tracking is performed by means of axial drift tubes (straws) and by means of electrons identification from scintillating fibers interleaved between the straws. The TRT Barrel covers the radius between 56 and 108 cm and has a sensitive region of 144 cm in length along the beam direction. In order to operate at the expected high rates with the desired spatial resolution, the diameter of the straws in the TRT was chosen to be 4mm, each straw anode is composed by a 31 μm thick gold-plated tungsten wire and the straw cathodes are generally operated at 1530V allowing to reach a gas gain equivalent to 2.5×10^4 for the chosen gas mixture, containing 70% Xe, 27% CO_2 , and 3% O_2 . Straws in the barrel region are mounted in concentric cylinders and are parallel to the beam directions while the end-caps are perpendicular to the beam direction. In order to allow the correct readout of the sensors with the high occupancy rate at design luminosity, single tubes are split in half by an insulating glass joint and signal readout is performed at both ends.

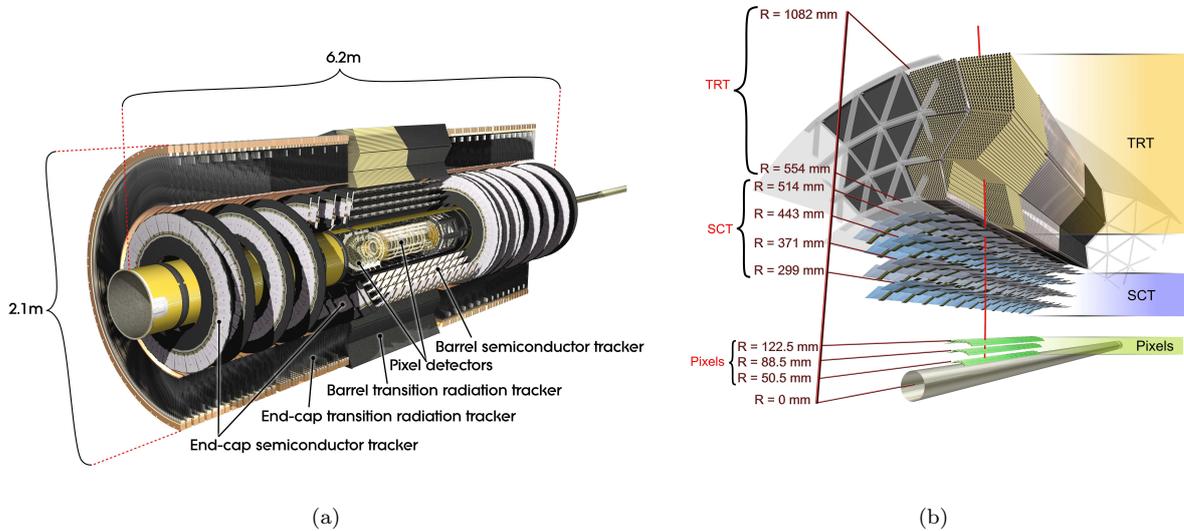


Figure 1.4: The ATLAS Inner Detector (a) and its expanded cross-section (b). (CERN-GE-0803014)

The magnet system

In order to measure the momenta of charged particles, it is necessary to bend them. To do so, ATLAS uses a set of two superconducting magnets so that the action of the Lorentz force can help identifying the properties of the observed particle: particles with high momentum will bend very little while particles with low momentum will curve more.

The inner solenoid, placed just outside the inner detector (see Fig.1.3), produces a 2 Tesla magnetic field which causes even very energetic particles to curve. Thanks to the uniformity of the field the momentum measurement can be very precise.

Outside the calorimeters but within the muon systems, eight flat superconducting race-track coils and two end-caps air toroidal magnets are placed (see Fig.1.3), they produce a very intense toroidal magnetic field which extends in a volume 26 meters long with 22 meters of diameter. The field in this region is not uniform because building a solenoidal magnet of the desired size would have been too expensive. The outer magnetic field varies between 1.5 and 7.5 Teslameters.

The calorimeters

Calorimeters are used to measure the energy of particles absorbed in them. The calorimeters in the ATLAS experiment are placed outside the solenoidal magnet, Fig.1.5 shows how the different calorimeters are placed inside the experiment. They are sampling calorimeters, meaning that particles are absorbed by high density materials and their energy is measured by periodically sampling the shape of the resulting shower. In the ATLAS detector two

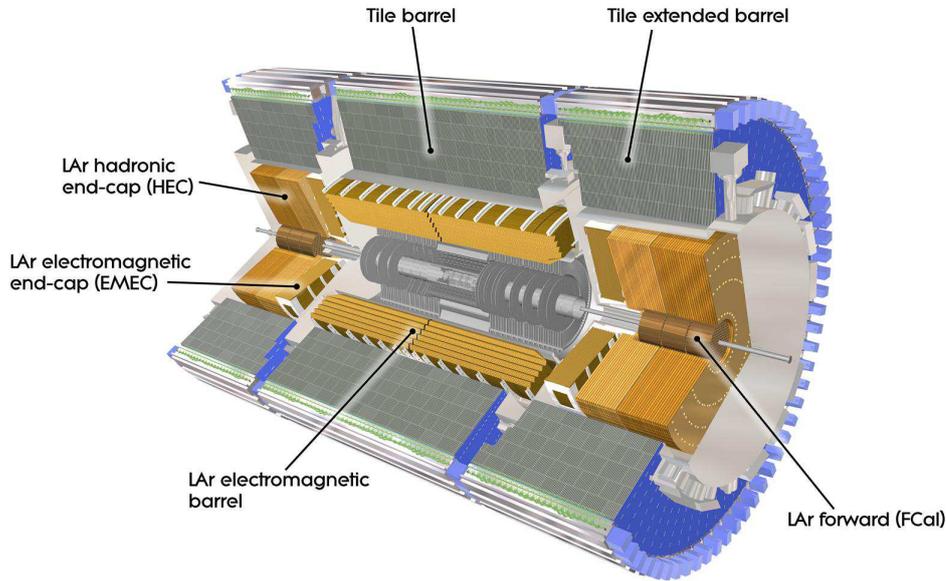


Figure 1.5: Computer generated image of the ATLAS Calorimeters system. (CERN-GE-0803015 01)

different calorimetry systems are present: (i) the Electromagnetic Calorimeter and (ii) the Hadronic calorimeter.

The electromagnetic calorimeter absorbs energy from particles that interact electromagnetically, mainly charged particles and photons. It returns a very high precision in both energy and position measurement. The absorbing elements are made of lead and stainless steel and the sampling material is liquid Argon. A cryostat is needed to maintain the calorimeter at operating temperature.

The Hadronic calorimeter measures the energy of particles that pass through the electromagnetic calorimeter but do not interact with strong force (e.g. Hadrons). The stopping material is steel and the energy is sampled using scintillating tiles.

The Muon spectrometer

The Muon spectrometer in the ATLAS detector is a very large system. It spans from a minimum radius of 4.25 m up to a maximum radius of roughly 11m (see Fig.1.3). It is used to accurately measure the momentum of muons and was designed to return a 1% accuracy for 100 GeV muons and 10% accuracy for 1 TeV muons.

The muon spectrometer was built like that in order to be sure to register all the muons resulting from the collisions. This is extremely important because only if all muons of a single event are detected it is possible to understand what kind of process was observed; moreover the total energy of the particles involved can only be measured if all muons are

detected.

The operation of the muon spectrometer is similar to the one of the inner detector (particles bending due to the presence of a magnetic field), but it is mainly composed by gaseous detectors. More details can be found in [8].

Data acquisition

The detector generates an incredible amount of data, about 1 Petabyte of raw data per second. The trigger system is very sophisticated and operates in real time to select only the most interesting events. Three different trigger levels are available: the first one uses signals coming from the detector to reduce the amount of selected events per second while the other two operate on a computer cluster close to the detector. After the trigger analysis is performed only a few hundred events remain to be stored for additional examinations, but there still is the need for about 100 Megabytes of disk space per second. Offline event reconstruction is performed through grid computing by scientists inside the ATLAS Collaboration that also write their own code to identify new patterns that might indicate new discoveries.

1.3.2 The Pixel Detector and the FE-I3 read-out chip

The pixel detector of the ATLAS experiment is located in the innermost layer and is installed very close to the beam pipe (see Fig.1.3 and Fig.1.4(a)) [9]. It was designed taking into account some very specific and stringent constraints related to the physics program that resulted in three major choices:

- three pixel hits over the full pseudorapidity¹ range ($|\eta| < 2.5$);
- minimum radius of the innermost pixel layer (b-layer) set to 5cm in order to maintain the proper clearance from the beam pipe vacuum system;
- smallest pixel size of $50 \times 400 \mu\text{m}^2$, constrain set by limitations in electronics design.

The ATLAS pixel detector is shown in more in Fig.1.6, its main components can be summarized as follows:

- the active region, composed by three barrel layers and three disks for each end-cap (both upstream and downstream);
- internal services and support structures (power, monitoring, communications etc...) on both ends of the active region (also supporting the Beryllium beam pipe).

The basic building block of both the barrel and end-cap regions, is a module made of hybrid silicon detectors connected to the readout chip which is itself connected to a flex-hybrid on which the control circuitry is mounted. The nominal pixel dimension is $50 \mu\text{m}$ in the ϕ

¹Pseudorapidity is a commonly used spatial coordinate describing the angle of a particle relative to the beam axis

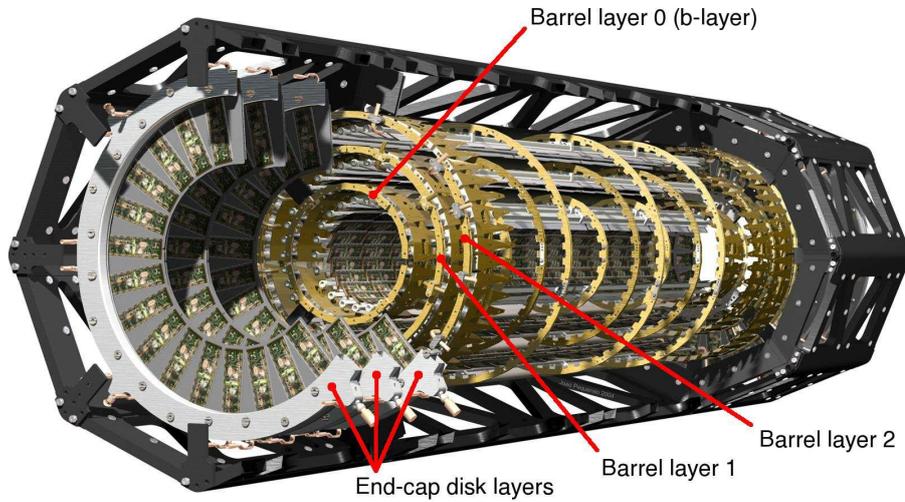


Figure 1.6: Sketch of the active region of the ATLAS pixel detector showing the barrel and the end-cap disks. (CERN-GE-0803013 02)

coordinate and $400\ \mu\text{m}$ in the z coordinate for the barrel region or r coordinate for the end-cap region. Each module contains 46080 pixels and is mounted on mechanical/cooling supports called staves (in the barrel region). Staves are composed of 13 modules each, they measure about 801mm and are equal for all the barrel layers. The staves are mounted on two carbon fiber half-shells that are later joined together to form each barrel layer. The disks in the end-cap regions are composed by modules mounted on similar cooling supports arranged in eight sectors per disk.

The ATLAS pixel detector covers an area of roughly $1.7\ \text{m}^2$ totaling approximately 67 million pixels in the barrel and 13 million in the end-caps.

The different parts of the detector were mounted in the surface building of the ATLAS experiment, tested, and were later lowered in the cavern. The entire pixel tracker was installed as single unit inside the Inner Detector.

The FE-I3 readout chip

The total number of channels is equal to 80 million, each containing about 1000 transistor for a total power of $100\ \mu\text{W}$ per channel. The read-out chip for the ATLAS pixel detector in its latest revision is called FE-I3, is designed in a $0.25\ \mu\text{m}$ CMOS technology and was produced in 2003. The chip contains 2880, $50 \times 400\ \mu\text{m}^2$ pixels, arranged in a 18×160 matrix and operates in a Time-over-Threshold (ToT) fashion: the total time for which the output signal remains above a set threshold is proportional to the total charge collected from the silicon sensor. The chip architecture is shown in Fig.1.7.

Each pixel cell contains a charge amplifier and a discriminator comparing the collected

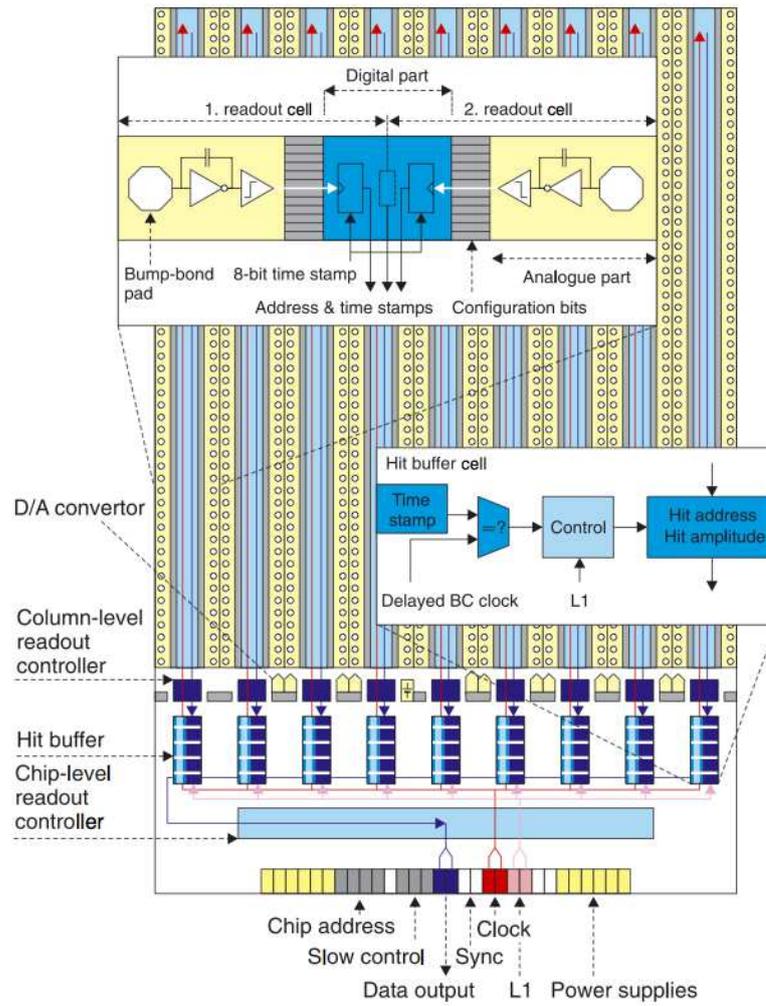


Figure 1.7: Schematic blocks of the FE-I3 readout chip. Image from reference [9].

charge to a programmable threshold. The digital part of the chip transfers three quantities to the buffers at the chip periphery: (i) the hit pixel address, (ii) the hit leading edge (LE) and (iii) the hit trailing edge (TE). The ToT is calculated as the difference between the TE and the LE timestamps. If a certain time interval ($\sim 3.2 \mu\text{s}$) passes without the arrival of a Level-1 trigger the hit is discarded and the buffers are cleaned. All the informations relative to selected hits (e.g. hits relative to a specific L1 trigger) are transmitted serially out of the chip in the order they arrived (First In First Out).

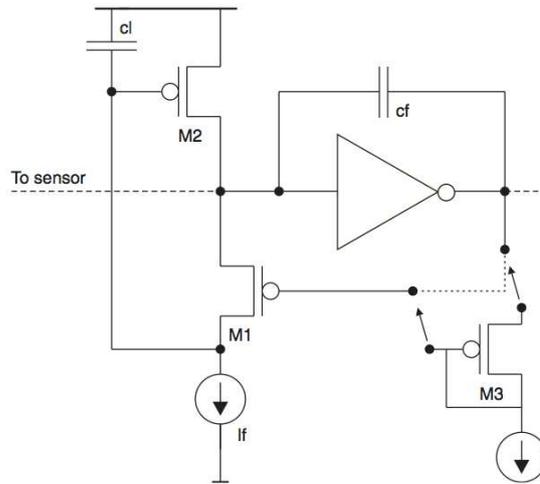


Figure 1.8: Schematic implementation of the FE-I3 charge amplifier feedback circuit. Figure from reference [10].

The Charge Sensitive Amplifier (CSA) is implemented with a single-ended, folded-cascode topology [10]. It is designed to cope with a maximum input capacitive load of 400 fF and to only accept negative signals in input. Due the foreseen high radiation levels, the input stage must be able to accept up to 100 nA of detector leakage current. As will be described later these parameters influence the architecture of the silicon sensor to be chosen.

The CSA feedback is realized with a 5 fF capacitor (C_f) with a current source continuous reset; the maximum rise time is 15 ns. The input stage will be DC coupled to the sensor and a leakage current compensation circuit is therefore needed in order to prevent unwanted voltage shifts on the analog output. This is shown in Fig.1.8 where M2 provides leakage current compensation and M1 resets the feedback capacitor. The circuit also includes a diode-connected transistor (M3), that acts as level shifter in order to assure that the output and input DC levels are essentially the same. Since C_f is discharged with a nearly constant current, the pulse width at the output of the CSA will be proportional to the input charge signal. It is therefore possible obtain the total collected charge by

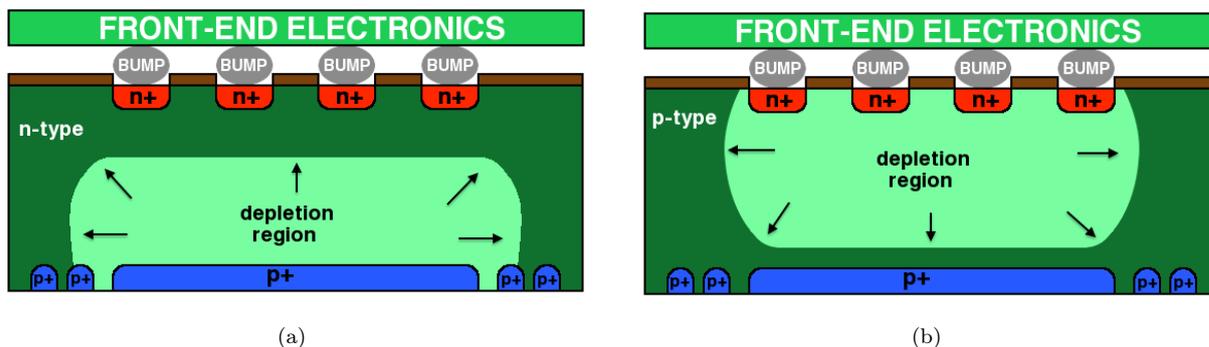


Figure 1.9: Evolution of the depletion region in an n^+ in n silicon sensor, (a) pre-irradiation and (b) post-irradiation.

measuring the ToT at the discriminator output. The measure of ToT is given in cycles of 40MHz clock.

The discriminator is implemented in two stages: a fully differential, low-gain amplifier and a DC coupled differential comparator. The threshold generator is locally implemented in each pixel in order to make it completely independent of the digital voltage supply across the chip and of the amplifier bias current.

The ATLAS silicon pixel detector

The silicon sensor must satisfy all the requirements imposed for the pixel detector, like geometries, material budget and granularity while maintaining high detection efficiency even after receiving extremely high radiation doses. As previously stated, all these constraints affect the sensor design in different ways, in particular the material choice and the layout of the pixel itself.

The final layout implement for ATLAS pixel sensors is a double-sided n^+ -in- n device architecture with pixelated electrodes (n^+) on the front side and a uniform p^+ implantation on the backside combined with several guard-rings at the edge. Device thickness is equal to $256 \pm 3 \mu\text{m}$. This particular choice of architecture was made for different reasons: (i) using the n^+ electrodes to read-out the generated charge will mean that the output signal will consist of electrons (one of the requirement of the read-out chip is that the input signal be negative), (ii) reading out electrons will also translate in faster signals due to the higher mobility of electrons in silicon with respect to holes and finally (iii) using an n -type bulk will ensure the proper operation of the pixel sensor also after irradiation. This last point in particular is crucial and, although the dynamics of radiation damage in silicon will be described in detail in Chapter 2, section 2.5, it deserves a brief explanation: it is known that n -type Float Zone silicon undergoes type inversion after sustaining some radiation, at

this point the effective doping of the bulk will be p-type and will tend to increase with increasing radiation damage causing a continuous increase of the full depletion voltage. If devices were made like standard p-in-n silicon detectors, this would mean that, after irradiation, the junction would move to the opposite side of the pixel and correct operation would be guaranteed only if full depletion was reached (this might require up to 2000 V in a standard 300 μm detector). By making a n-in-n silicon device, the junction will proceed from the backside before irradiation, when full depletion voltage is still at acceptable values while, after heavy irradiation and type inversion, the depletion will proceed from the pixel side thus ensuring the operation as a pixel device even if full depletion is not reached. This is illustrated in Fig.1.9.

Surface isolation on the pixel side of the sensor is ensured by means of moderated p-spray implants which proven to be reliable up to doses of 500 kGy in silicon. Pixel modules are expected to withstand a radiation fluence of 1×10^{15} 1MeV n_{eq}/cm^2 . This corresponds to the expected dose resulting from five years of LHC operation with a 10^{34} $\text{cm}^{-2}\text{s}^{-1}$ luminosity at the B-layer position.

A single sensor tile, made of 16 pixel detectors, is composed by 47232 pixels arranged in 144 columns and 328 rows. In 128 of these columns, the implant size for a simple pixel is equal to 382.5×30 μm^2 , with a pitch corresponding to 400×50 μm^2 , while in 16

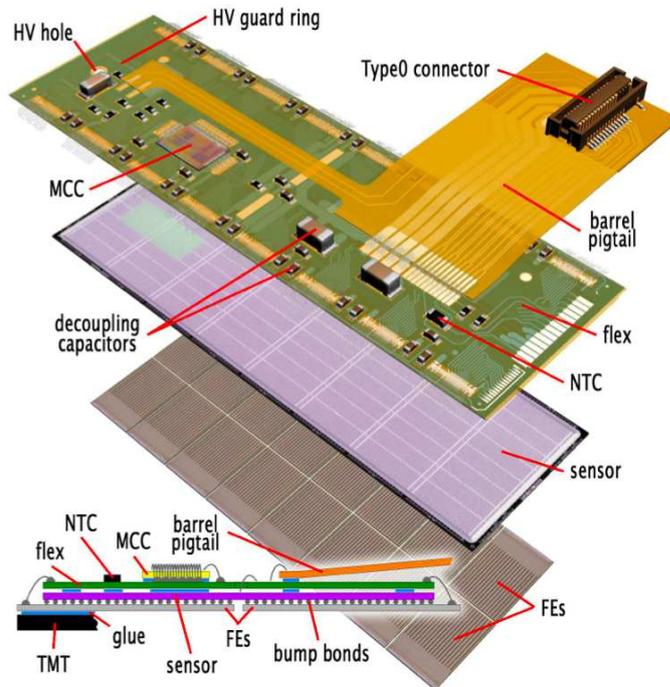


Figure 1.10: Sketch and cross-section of an ATLAS pixel module composed by a sensor tile and 16 front-ends. Figure from reference [9].

columns pixels have implant size of $582.5 \times 30 \mu\text{m}^2$ with a pixel pitch of $600 \times 50 \mu\text{m}^2$. In each column, eight pairs of pixel are connected together to a common readout, bringing the total number of independent readout rows to 320 or 46080 readout channels. This particular arrangement is needed in order to allow the connection of a sensor tile to 16 readout chips simultaneously.

Silicon sensors and readouts are connected together by means of bump-bonding and flip-chip. This process is complicated and expensive, it is therefore important to be able to select good devices directly on wafer. To do so, each pixel on the device is connected to a bias metal grid using punch-through connection. This allows for a measurement of the total sensor current before the bump-bonding thus allowing for a thorough device selection.

Each ATLAS pixel module, shown in Fig.1.10, has an active surface of $6.08 \times 1.64 \text{ cm}^2$ and is composed by the following parts:

- 47232 pixels;
- sixteen front-end chips;
- a fine-pitch, double sided, flexible printed circuit (flex-hybrid), with a thickness of $100 \mu\text{m}$ routing signals and power;
- a Module Control Chip (MCC) situated on the flex;
- a "pigtail" (only for barrel modules) providing connection to electrical services via microcable; in the disk modules microcables were attached without pigtails.

1.3.3 The Semi-Conductor Tracker

The Semi-Conductor Tracker (SCT) [12], is placed right outside of the pixel detector and is composed by 4 concentric layers in the barrel region and a total of 18 end-cap disks. Fig.1.4 illustrates both the positioning and the composition of the SCT. The sensors used in the SCT are silicon micro-strip detectors with a total area coverage of about 61 m^2 and 6.3 million readout channels. The radius of the innermost barrel layer is equal to 30 cm while the radius of the outermost is equal to 56 cm. The SCT has a total length of 160 cm along the beam direction (z -axis). The two groups of 9 end-cap disks are symmetrically positioned with respect to the interaction point.

The SCT module layout is essentially similar for both barrel and end-cap modules, the only difference is in the module shape. All the barrel modules [13] are identical while the end-cap modules come in four different flavors [14] depending on where they will be mounted. An ATLAS barrel module is shown in Fig.1.11, on each module two pairs of p-in-n silicon strip detectors are mounted, they are glued back-to-back with a stereo angle of 40 mrad in order to allow for the reconstruction of 2D coordinates.

The total 1536 strip on each module have a pitch of $80 \mu\text{m}$ in the barrel layers while

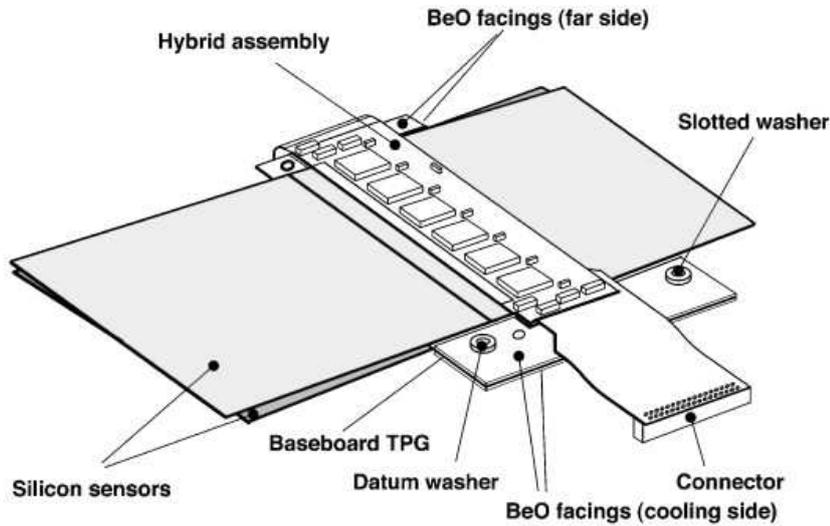


Figure 1.11: Drawing of the ATLAS SCT barrel module [13].

the pitch varies between 57 and 94 μm in the end-cap modules. Full depletion of the silicon sensors is reached at about 65 V, they are normally operated in over-depletion at a nominal bias voltage of 150V. The total power consumption per module is in the order of 5.6W before irradiation. The maximum space resolution achievable in the SCT is equal to 17 μm in the r - ϕ direction and 580 μm in the z direction.

Silicon strip detectors on each module side are readout using six 128-channels ABCD3TA chips [15]. These chips were fabricated in radiation hard DMILL technology. Signals coming from the detectors go through a chain composed by pre-amplifier, shaper and discriminator. The pre-amplifier is based on a transimpedance configuration and the shaper is a CR-(RC)³ filter with a peaking time of about 20 ns which becomes closer to 25ns if the sensor collection time is taken into account. The gain of the pre-amplifier and shaping chain is about 50 mV/fC. The discriminator threshold is set with a differential scheme. The output of the discriminator is buffered on chip until the arrival of an L1 trigger.

After a 10-years operation of the LHC, the foreseen radiation fluence for SCT modules is in the order of 2×10^{14} 1MeV n_{eq}/cm^2 . Radiation effects are limited by cooling down the modules to -7°C in the end-caps, between -2 and -1.5°C in the 3 inner barrel layers and 4.5°C in the fourth barrel layer.

1.3.4 ATLAS upgrade plans

Experiment upgrades must obviously follow LHC shutdowns; accelerator shutdowns planned in the Chamonix 2012 meeting, were reported in section 1.2.1. The outline of

the main upgrades for the ATLAS experiment was presented in [16] and will be briefly summarized in the following paragraph.

The so called, Phase-0 upgrade will take place during the long shut-down (LS1) of 2013-2014. This upgrade will mainly regard detector consolidations and in particular:

- a new tracker evaporative cooling plant will be installed;
- new calorimeters LV power;
- magnets cryogenics consolidation;
- muon spectrometer consolidation;
- infrastructure maintenance and repairs.

The only real upgrade during Phase-0 will consist in the installation of a new pixel layer in the core of the experiment: the Insertable-B layer (IBL). All the details of this new pixel layer will be described in chapter 4, section 4.1, because they are strictly related to the topic of this thesis. The installation of an additional pixel layer will require the installation of a new, smaller radius, Beryllium beam pipe. Apart from the IBL the so called Diamond Beam monitor will be mounted both upstream and downstream from the experiment and new chambers in the muon spectrometer will also be put in place.

The second long shutdown, marking LHC's Phase-1, is expected for 2017-2018. The main planned upgrades are related to the trigger system, in order to maintain triggering efficiency also when the pile-up will increase. In particular new muon small wheels will be installed together with a new high granularity calorimeter Level-1 trigger electronics. To further improve the triggering, the so called fast tracker trigger (FTK) will be implemented using pixel and SCT informations. Other several maintenance and network/electronics upgrades are planned. Last but not least, the ATLAS Forward Physics (AFP) detector will be finalized; since the detectors object of this thesis are strong candidates for AFP more information about the project are given in chapter 6, section 6.1.

By the end of Phase-1, the LHC will have delivered 300-500 fb⁻¹ and will be prepared for the luminosity leveling at 5×10³⁴ cm⁻²s⁻¹. The third long shutdown is currently foreseen for 2022-2023 and the ATLAS Phase-2 upgrade is currently taking shape. Main activities will regard the complete replacement of the Inner Detector with a new and more modern one. The forecasted conditions during LHC Phase-2 will probably require the complete replacement of the forward calorimeter and hadronic end-cap electronics. The muon spectrometer will be completely updated as well, together with all electronics and computing infrastructures that will be obsolete after more than ten years of operation. The plan is to be ready for installation by 2021 and the letter of intent should be ready by the end of December 2012.

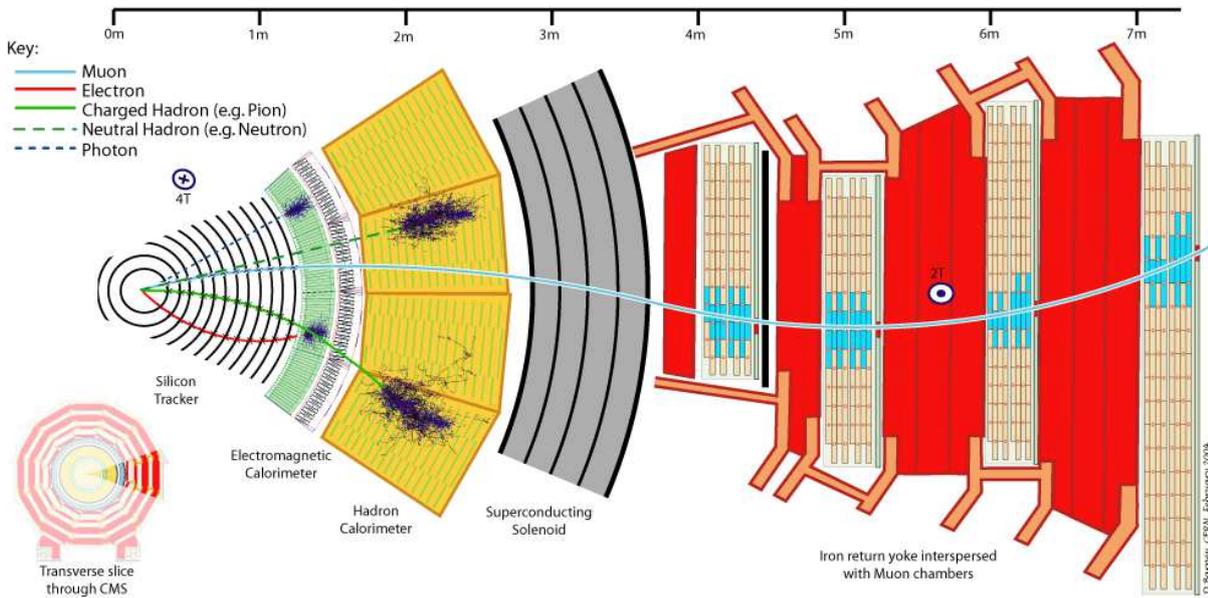


Figure 1.12: Sketch of the CMS particle detector. (IPPOG Document 12-v1)

1.4 The CMS Experiment

The Compact Muon Solenoid (CMS) is the other general-purpose particle detector built at CERN and, similarly to ATLAS, it will look for new particles and/or new physics phenomena in the TeV scale. The operation of CMS is very similar to the one of ATLAS but the design of the detector is different and the internal layers are arranged in a different order. The total weight of the the machine is 12500 tonnes, and it is slightly smaller than ATLAS, measuring a total length of 21.5m and a diameter of 15m. The next subsection will give a brief description of all the layers, the silicon detector will again be in a separate subsection in order to allow for a more thorough analysis. More detailed information are available in [11].

1.4.1 Structure of the CMS experiment

A schematic cross-section of the CMS experiment is shown in Fig.1.12. CMS is more compact than ATLAS and, in fact, both the tracker and the calorimeter are contained in the solenoid which generates a powerful 3.8T magnetic field. Outside the magnet, large muon detectors are installed.

The Inner Tracking system

The tracking system is the innermost component of the CMS detector. The arrangement of its internal layers was designed after considerations related to the expected particle flux at different radii at high luminosity. Three well defined regions were identified:

- close to the interaction region pixel sensors are installed in order to achieve an occupancy of about 10^{-4} per pixel per bunch crossing;
- the flux in the intermediate region ($20 < r < 55$ cm) is low enough to allow the installation of strip sensors with $80 \mu\text{m}$ pitch that will lead to an occupancy of about 2-3% per bunch crossing;
- in the outermost layer of the tracking system the particle flux drops significantly and the use of strip detectors with maximum pitch of $180 \mu\text{m}$ is possible while keeping the occupancy low.

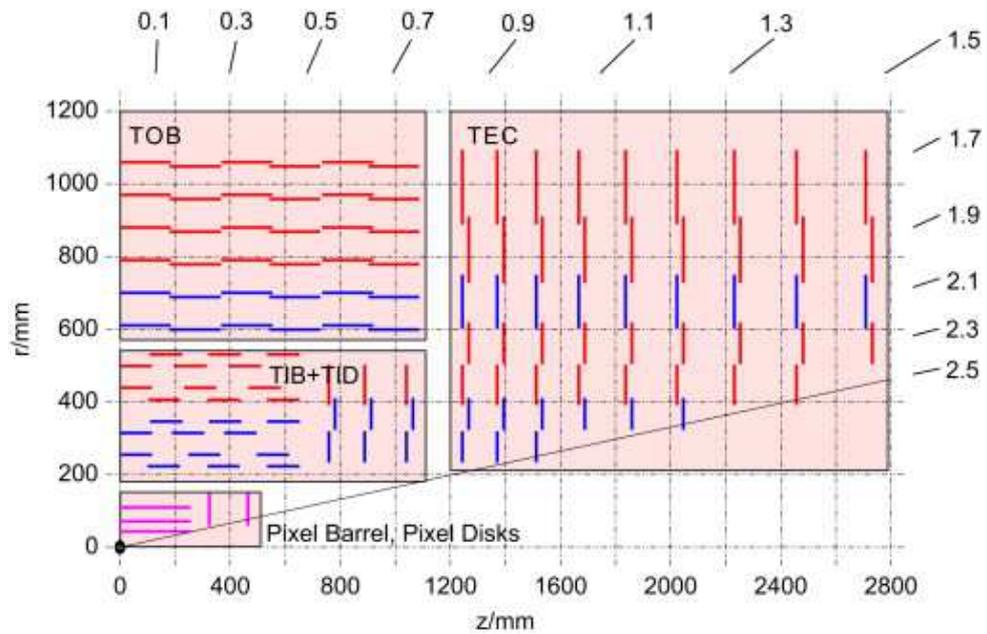


Figure 1.13: Layout of one quarter of the CMS Tracking system. Image from reference [18].

A sketch of a quarter of the CMS inner tracking system shown in Fig.1.13. In the region closer to the interaction point, in the barrel region, three pixel layers are installed at radii of 4.4, 7.3 and 10.2 cm. The strip detectors in the barrel region are placed between 20 and 110 cm radii; the barrel is subdivided into two region: the Inner Barrel (TIB) and the Outer Barrel (TOB), the former being shorter than the latter in order to avoid shallow track crossing angles. The TIB is composed by a total of 4 layers while the TOB is made of 6 layers. The forward region is made out of 2 pixel layers and 9 strip layers (in each of the two end-caps). Moreover three additional Inner Disks (TID) are inserted in the TIB

in the transition region between the barrel and the end-caps. The total area coverage of the pixel and strip detectors is roughly 1 m^2 and 200 m^2 respectively. The inner tracker includes a total of 66 million pixel channels and 9.6 million strip channels. Additional detail on silicon pixel and strip detectors of the CMS experiment will be given in sections 1.4.2 and 1.4.3.

The Calorimeters

Two different type of calorimeters are available in CMS (similarly to ATLAS): (i) the Electromagnetic Calorimeter (ECAL) and (ii) the Hadronic Calorimeter (HCAL) (see Fig.1.12).

The main objective of the Electromagnetic calorimeter is to measure the energies of electrons and photons with precision. It is made of lead tungstate (PbWO_4) crystals; this particular material is very dense but results to be extremely optically clear transporting about 80% of the light in the bunch spacing time (25ns). These good properties are balanced buy a rather low light yield of about 30 photon per MeV of energy deposited. The crystals have a volume of $22 \times 22 \times 230 \text{ mm}^3$ and are arranged in matrix with carbon fiber supports. The readout is performed through avalanche photodiodes.

The Hadronic Calorimeter, on the other hand, is used to measure the energy of the Hadrons produced from the collisions. The HCAL is made of layers of very dense materials (e.g. brass or steel) interleaved with plastic scintillating tiles which are readout through wavelength shifting optical fibers and hybrid photodiodes.

The Magnet

The CMS solenoid magnet is placed in between the ECAL and HCAL (Fig.1.12); the generated magnetic field allows for the correct measurement of particle momentum. The magnet itself is 13m long and 6m in diameter and is kept refrigerated with a cryostat. The design operating field was 4T but the magnet is now being operated at 3.8T in order to extend its lifetime. At such operating field, it requires a current equal to 18160A returning a stored energy of 2.3GJ. In order to protect the magnet from the possibility of a quench, dump circuits are in place.

The Muon detectors and the return yoke

The detection of muon trajectories in CMS is performed by means of gaseous detectors like in ATLAS. Three types of sensors are available: (i) drift tubes (DT), in the barrel region, (ii) cathode strip chamber (CSC), in the end-caps regions and (iii) resistive plate chambers (RPC) both in the barrel and end-caps regions. The disposition of each detector

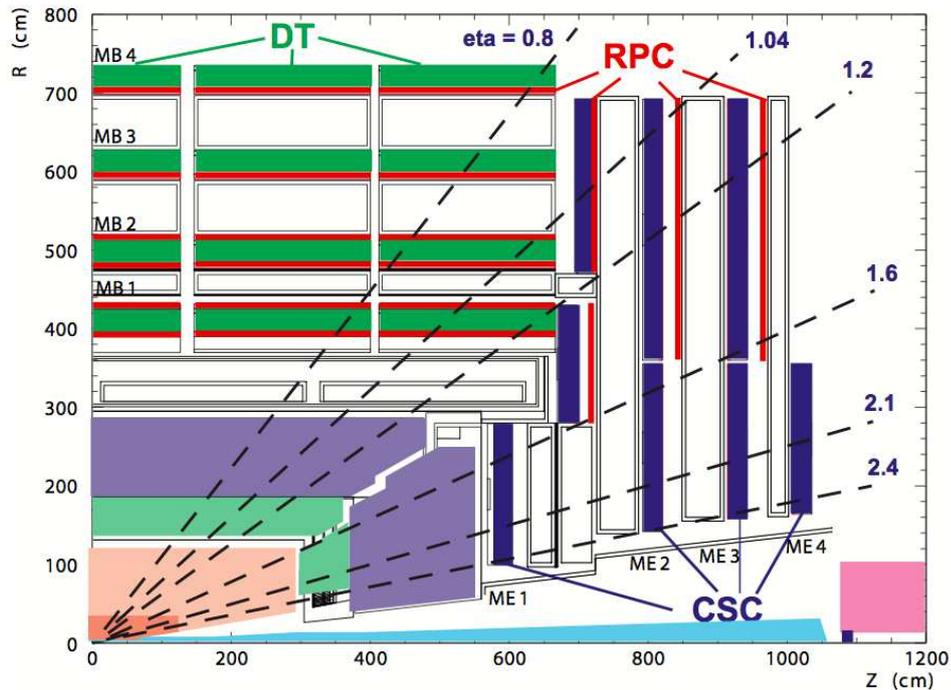


Figure 1.14: Layout of one quarter of the CMS Muon system. Image from reference [11].

type is shown in Fig.1.14. The return yoke of the CMS detector is responsible for the return of the magnetic flux and is split into a cylindrical central part (barrel) and two end-caps made of 600mm thick disks.

Data collection and analysis

The amount of data produced by CMS in a single crossing is equivalent to about 1MB which, given the 40MHz bunch crossing, results in a 40TB of data per second. This amount of data is too large to store even for modern high performance computers. Luckily the trigger system is able to reduce the amount of events per second to about 100. In order to do so multiple trigger stages are implemented. After each collision all data are temporarily stored into buffers while preliminary informations from the muon system and calorimeters are analyzed to look for interesting patterns. It takes around $1 \mu\text{s}$ to perform this preliminary analysis on custom field-programmable gate arrays (FPGA). Data from events that pass the so called "Level-1 trigger", are then collected and sent over optical links to the "High Level Trigger" which, thanks to the now lower event rate, is able to perform much detailed analysis and decide which events should be stored for further study. The High Level Trigger runs on ordinary computer servers. Similarly to what happens for ATLAS, data collected from the CMS detector are analyzed by means of grid computing

from scientist in the CMS Collaboration.

1.4.2 The pixel detector and the PSI46V2 read-out chip

The philosophy of the pixel sensor and readout chip of the CMS experiment is very similar to the one of the ATLAS experiment. The main differences are related to the chip layout which is mostly analog with a classical CSA followed by an analog shaper that also affects the final pixel size.

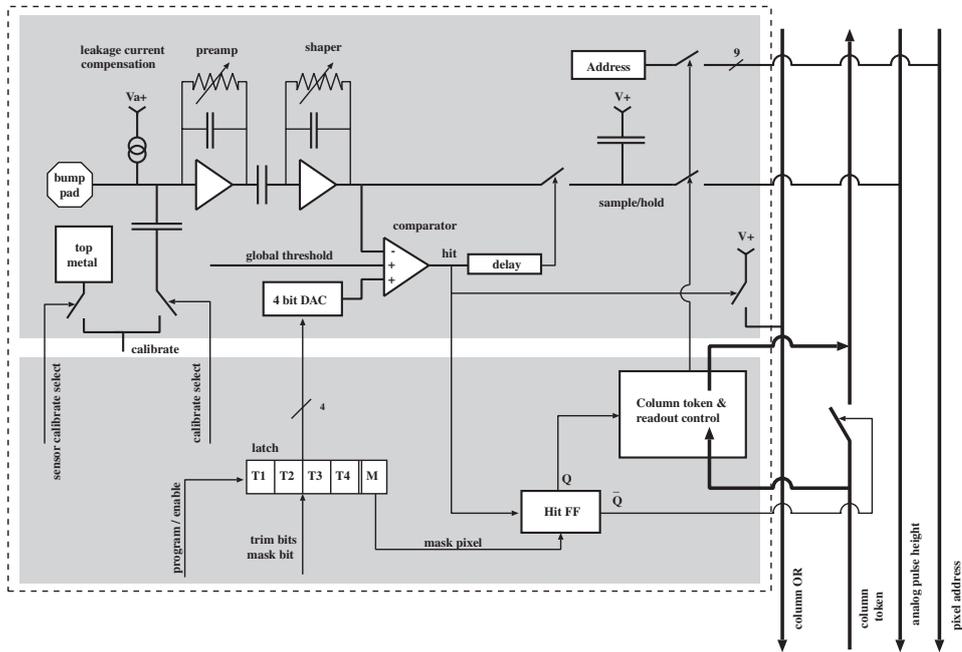


Figure 1.15: Schematic view of a pixel cell of the PSI46V2 chip. Image from reference [19].

The PSI46V2 readout chip

The readout chip of the CMS pixel detector is called PSI46V2 [19, 20] and a schematic view of one of its pixel is shown in Fig.1.15. Its active matrix is composed by 52×80 pixels and has a size of 8×7.8 mm². The periphery of the chip is 1.8 mm long mostly due to the buffer size. The full readout of the entire matrix at once is not feasible due to the large amount of data to be transferred. Zero suppression at a very early stage allows for a great reduction of data to be transmitted. The chip is realized in a radiation-hard $0.25 \mu\text{m}$ DMILL technology that allows for a minimum pixel size of $100 \times 150 \mu\text{m}$.

The analog part of the chip is composed by a CSA and shaping amplifier. Since the input pixel capacitance will be very low, the main concern is not noise but speed in order for the chip to be fully operative inside the LHC bunch crossing.

The CSA has a sufficient gain to deal with signals of just a few thousand electrons; the gain can be reduced for larger signals and at the same time the integration can be faster. In order to obtain a more power efficient design it was chosen to implement a 20 fF feedback capacitor followed by an additional gain stage instead of implementing only a very small C_f . The preamplifier input is DC coupled to the pixel sensor therefore the feedback circuit must be able to cope with the increase in leakage current expected for irradiated devices (expected values in the order of 10nA) without causing output offsets larger than ~ 100 mV (the feedback resistor should be kept inside reasonable values). Another important aspect is to keep the time constant of the preamplifier output ($R_f C_f$) considerably larger than the preamplifier rise time. In order to fulfill both constraint on the value of R_f , a $\sim \text{M}\Omega$ resistor should be implemented. To do so it was chosen to use a weak p-MOS transistor operating in the linear region. The second stage is the shaper and is AC coupled to the preamplifier output through a capacitor which also provides an additional gain stage (the gain is the ratio between the coupling capacitor and the preamplifier feedback capacitor). The shaper output is connected to the comparator and sample-and-hold through a buffer that reduces its load. The comparator threshold is adjustable with a 8-bit ADC. The peaking time is slightly larger than the bunch crossing, meaning that not all the pulses will reach the threshold in the same bunch crossing. This causes the effective threshold for useful signals to be slightly larger (e.g. for a 3000 electron threshold the effective threshold shifts to 3800 electrons with an analog current of $5 \mu\text{A}$ per pixel).

The Level-1 trigger latency in CMS is equal to $4 \mu\text{s}$. The probability of getting more than one hit in the same pixel per trigger latency is still pretty high so buffering is necessary. The chip was designed to have the buffers placed outside the active matrix in order to achieve a smaller pixel size. In this way it is also possible to share buffers between different pixels thus making the chip more efficient. The pixels communicate the detection of a hit over a wired OR without the clock being redistributed over the entire chip. The entire pixel matrix is then scanned to identify hit pixels; in order to reduce the hit collection times, hit pixels must resynchronize with the periphery, this allows to skip pixels without hits and reduces the transfer speed to 20 MHz. Data transferred in the buffers are the pixel address (row) and pulse height. Hits and time stamps are stored during the trigger latency and, if no L1 trigger arrives, buffers are made available for the next hits. Buffers overflow if more than 32 hits occur during the trigger latency, in which case some data are lost.

The CMS silicon pixel detector

The sensors for barrel and forward detectors were independently developed by two different vendors but the same layout choice was implemented. Similarly to ATLAS pixel sensors, CMS devices are n^+ -in- n as well. This choice was made for the same reasons previously described in section 1.3.2. The inter-pixel isolation technique was implemented differently between end-cap and barrel devices: for the barrel sensors a moderated p-spray was implemented while for the end-cap open p-stop was implemented. Pixel devices are tested on wafer before the bump-bonding process with a technique similar to the one used for ATLAS pixels.

The area between the pixels and the edge of the sensors is covered by an n-implant which is connected to ground through the readout chip in order to ensure the possibility of draining unwanted edge currents and to maintain the device edges to a low potential. The high voltage applied on the backside is gradually dropped toward the outside by means of multiple guard-rings. The edge region width is 1.2 mm wide.

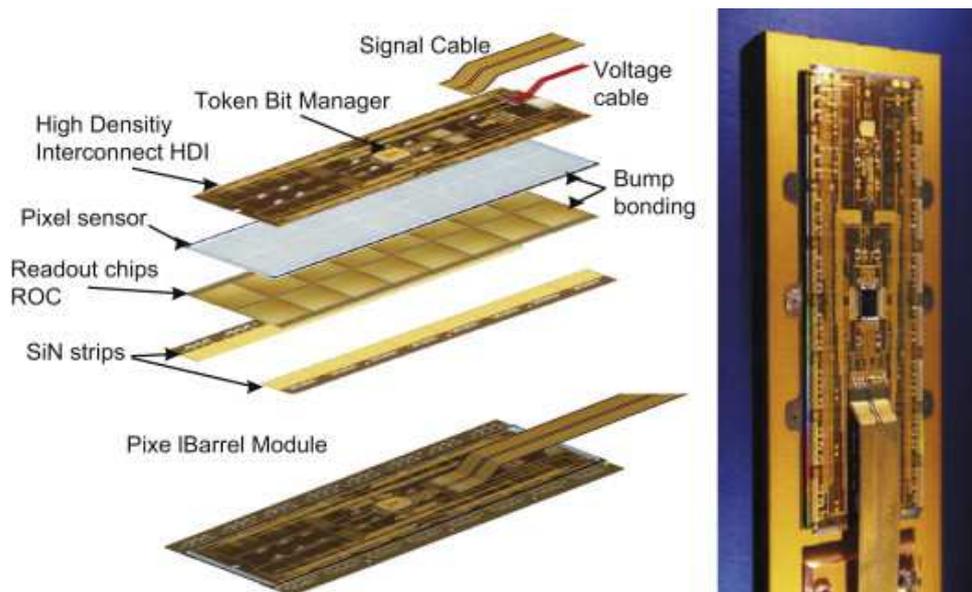


Figure 1.16: Drawing and picture of CMS barrel pixel module. Image from reference [21].

A barrel module of the CMS pixel detector is shown in Fig.1.16. The full module is composed by 16 readout chips connected to the same sensor tile. Sensor elements at the chip boundaries have a width double than normal in order to avoid dead regions, corner pixels are four times larger. Readout chips are 0.8 mm larger than the sensors allowing to reach the wire bond pads. Wire bonds connect the readout chips to a high density interconnect (HDI) glued to the back of the sensor tile. Base strips made of silicon nitride are glued underneath the readout chips and allow the mounting of the modules on the

barrel mechanics. A complete full module measures $66.6 \times 26 \text{ mm}^2$ and consumes a total power of $\sim 2 \text{ W}$.

1.4.3 The Silicon Strip Tracker (SST)

The strip detector of the CMS experiment is divided into two parts, the TIB (Tracker Inner Barrel) and the TOB (Tracker Outer Barrel) [17] (see Fig.1.13). The TIB is made of 4 layers and covers coordinates along the beam axis up to $|z| < 65 \text{ cm}$. The sensor thickness is in the order of $320 \mu\text{m}$ and the strip pitch varies between 80 and $120 \mu\text{m}$. In order to obtain accurate position measurements both in $r-\phi$ and $r-z$ the first two layers are composed of modules with a stereo angle of 100 mrad leading to a resolution of 23 to $34 \mu\text{m}$ in the $r-\phi$ direction and $230 \mu\text{m}$ in z .

The TOB features a total of 6 strip layers with a coverage of $|z| < 110 \text{ cm}$. Due to the larger distance to the interaction point it is possible to use $500 \mu\text{m}$ thick silicon sensors in this layer without affecting the signal to noise ratio. The strip pitch in the TOB varies between 120 and $180 \mu\text{m}$. A stereo angle of 100 mrad is used in the first two layers of the TOB, delivering a single-point resolution of 35 to $52 \mu\text{m}$ in the $r-\phi$ direction and $530 \mu\text{m}$ in z .

The end-caps are divided in TEC (Tracker End Cap) and TID (Tracker Inner Disks). Each TEC (one on each side of the tracker) is composed by a total of 9 disks covering the regions $120 < |z| < 280 \text{ cm}$ while each TID comprises 3 small disk that fill the gaps between the TIB and the TEC. The modules in the TEC and TID are radially arranged around the beam pipe and are organized in rings with strip pointing toward the center of the beam line. For this reason strips have a variable pitch.

The entire SST is composed by 15400 modules that are operated at a temperature of -20°C . The total amount of silicon sensors is equal to about 24000 and 15 different geometries are implemented.

Silicon sensors are produced on 6", n-type, $\langle 100 \rangle$ oriented wafers with a standard fabrication process [22]. A single strip tile is fabricated on each wafer and it is requested to lie into a fiducial region of 13.9 cm of diameter. As previously stated, two sensor thicknesses are of interest, 320 and $500 \mu\text{m}$. Wafer resistivity is in the range 1.5-3.25 $\text{k}\Omega\text{cm}$ for "thin" sensors and in the range 4-8 $\text{k}\Omega\text{cm}$ for "thick" sensors. Strip detectors were fabricated by two different vendors: ST Microelectronics and Hamamatsu Photonics.

Radiation tolerance constrains on the SST are less stringent than on the pixel tracker due to its large distance from the interaction point. For this reason silicon strip sensors are fabricated with a p-in-n approach, meaning that the readout electrodes on the frontside are p-type in a n-type silicon bulk. A uniform n^+ implantation is realized on the backside of the device. An additional n^+ implantation is requested also close to the edge on the

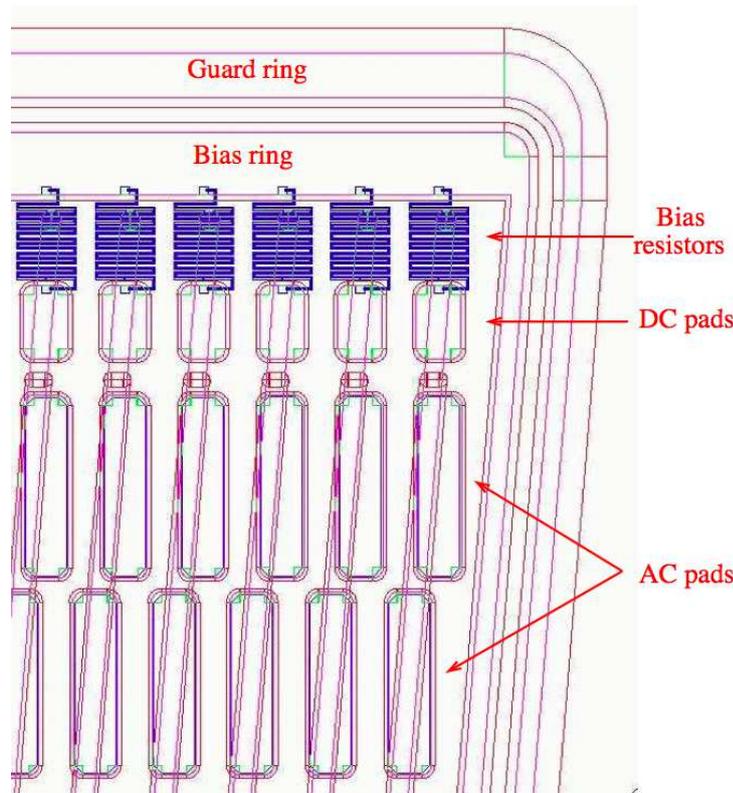


Figure 1.17: Layout of a CMS strip sensor, all the most important details are highlighted. Figure from reference [22].

front side in order to prevent the space charge region to reach the highly damaged cut region. The active area is surrounded by two p^+ rings, the outer one, let floating, helps in gradually reducing the electric field toward the edge while the inner one is used to bias the strips. In order to prevent unwanted edge related effects the strip to edge distance was chosen to be twice the thickness plus $110 \mu\text{m}$. Premature breakdown effects are avoided with an intensive used of field-plates. The pitch to width ratio is maintained constant to 0.25 for all sensor geometries. Each strip has an integrated coupling capacitor used to connect to the readout electronics and is biased by means of a polysilicon resistor of $1.5 \pm 0.5 \text{ M}\Omega$. Two rows of AC pads are available at each strip end for testing and wire bonding. The layout of one of the several sensor geometries is reported in Fig.1.17

The readout chip for the strip tracker at CMS is called APV25 and is a 128 channels chip realized in $0.25 \mu\text{m}$ CMOS technology [23]. It is realized including standard processing blocks like a charge amplifier (CSA) and CR-RC shaper with 25 ns peaking time that can operate in peak or deconvolution mode. The CSA is realized with a single-ended cascode amplifier with a 150 fF feedback capacitor. The p-FET input transistor has a W/L equal to $2000/0.36 \mu\text{m}$ and is biased with a $400 \mu\text{A}$ current. A feedback transistor provides

the discharge path for the feedback capacitor. The shaper is composed of a single-ended cascode amplifier (non-folded) with a feedback capacitor of 150 fF and a coupling capacitor of 1.4 pF. The chip noise was estimated to be 246 electrons plus 36 electrons for each pF loading the preamplifier input (e.g. 900 electrons with a 18 pF detector capacitance).

1.4.4 CMS upgrade plans

The CMS upgrades will also follow the LHC's long shutdowns but experiment components will be upgraded with a different schedule with respect to ATLAS. The CMS upgrade plans are reported in [24].

During LS1 the complete consolidation of the muon end-cap station will be performed mounting new RPC and CSC together with new electronics. Another upgrade will regard the replacement of photodetectors in the hadron forward and outer calorimeters with multi-anode Photo Multipliers (PM) and Silicon Photo Multiplier (SiPM). The tracker cooling will also be consolidated in order to work efficiently at -20°C . A new 45 mm beam pipe will also be installed during LS1, this will allow the replacement of the silicon tracker in future shutdowns.

The tracker upgrade is currently planned for the LS2 in 2017-2018 but thanks to the fact that CMS is considerably more modular than ATLAS, the installation of a new silicon tracker is simpler, faster and might occur anytime after 2016, for example during an extended winter shutdown. Several silicon sensor technologies are being investigated for this upgrade and among them the devices object of this thesis. Other upgrades planned for LS2 are the replacement of photodetectors in the barrel and end-cap hadron calorimeter and the implementation of new trigger electronics (micro-TCA).

Upgrades plans for CMS Phase-2 are currently being outlined. The expectations are to completely replace the tracker, the end-cap calorimeters and the trigger electronics. The technical proposal for the full Phase-2 CMS upgrade will be ready by the end of 2014.

Chapter 2

Silicon Radiation Detectors

Semiconductor detectors have been used in spectroscopy applications since the 1960s. Their main advantage is the lower energy to produce an electron-hole pair with respect to ionization chambers: 3.6 eV versus about 20 eV. This translates in a much better energy resolution for silicon detectors.

The intensive use of semiconductor detectors as tracking elements in particle physics, started in the 1970s. Silicon is preferred in these applications because it is the most studied semiconductor, is really cheap and can be found in great abundance. Moreover, the availability of well established processing capabilities, thanks to ever growing progress of electronics industries, made silicon the most used material in particle tracking.

Being a crystalline material, silicon is sensitive to radiation damage but, as presented in sec.2.5, radiation effects are understood and several counteractions can be taken in order to limit their effects. Other semiconductor materials are nowadays available that might offer better radiation hardness than silicon but they are not currently available in large wafers (e.g. Diamond) or their quality is not yet fully acceptable (e.g. CdTe and SiC).

Since this thesis focuses on novel silicon detectors, only silicon will be discussed in this chapter. Basic working principle of radiation detectors and readout electronics will be introduced also focusing on sensor properties needed in tracking systems. Radiation damage in silicon will also be discussed.

2.1 Basic concepts on semiconductor detectors

This section will only describe the basic semiconductor physics necessary for a sufficient understanding of silicon detectors behavior. This choice was made to leave more room to more important topics in later chapters. The understanding of semiconductor physics is well established and discussed in several textbooks [25, 26]. The use of semiconductors as tracking materials and relative readout electronics are also very well described in literature

and in particular references [28, 29, 30] are the main source of informations used for this chapter.

2.1.1 Basic notions of semiconductor physics

Silicon, as every other semiconductor, has a forbidden region in the energy band structure, the so called *band gap*. In intrinsic silicon (e.g. without impurities) and at low temperatures, the conduction band is empty while the valence band is full. In these conditions the concentration of electrons " n " and holes " p " inside the material is equal to the intrinsic concentration $n_i=n=p$. More specifically, the concentration of electrons can be calculated by multiplying the density of states in the conduction band $N(E)$ by the probability of their occupation given by the Fermi-Dirac function $F(E)$ [26]:

$$n = \int_{E_C=0}^{+\infty} N(E)F(E) dE, \quad (2.1)$$

where E_C is the lower bound of the conduction band. The density of states in the conduction band can be calculated as [26]:

$$N(E) dE = 4\pi \left(\frac{2m_n}{h^2} \right)^{2/3} E^{1/2} dE, \quad (2.2)$$

where m_n is the effective mass of the electron and h is Plank's constant. The Fermi level at room temperature is usually located toward the middle of the band gap. The Fermi function $F(E)$ can therefore be approximated with an exponential function in the conduction band:

$$F(E) = \frac{1}{1 + e^{(E-E_F)/kT}} \approx e^{-(E-E_F)/kT}, \quad (2.3)$$

where E_F is the energy of the Fermi level, k is Boltzmann's constant and T is the temperature. By substituting Eq.2.2 and Eq.2.3 in Eq.2.1 and solving the integral, it is possible to obtain the concentrations of free charge carriers in the material:

$$n = 2 \left(\frac{2\pi m_n kT}{h^2} \right)^{3/2} e^{-(E_C-E_F)/kT} = N_C e^{-(E_C-E_F)/kT}, \quad (2.4a)$$

$$p = 2 \left(\frac{2\pi m_p kT}{h^2} \right)^{3/2} e^{-(E_F-E_V)/kT} = N_V e^{-(E_F-E_V)/kT}, \quad (2.4b)$$

where n and p are the concentrations of free electrons and holes, m_n and m_p are the masses of electrons and holes, E_C and E_V are the energies of the conduction and valence bands and E_F is the energy of the Fermi level. The quantities N_C and N_V are the states concentrations in the conduction and valence band respectively. The product of electron

and hole concentrations in the material:

$$np = n_i^2 = N_C N_V e^{-E_g/kT}, \quad (2.5)$$

is independent of the Fermi level, it only depends on the temperature. The energy gap E_g is defined as the difference between the energies of the conduction and valence bands ($E_C - E_V$). The amount of free electrons in an intrinsic semiconductor always equals the amount of free holes and this allows for the calculation of the intrinsic carrier concentration in silicon at a temperature $T=300$ °K:

$$n_i = 1.45 \times 10^{10} \text{ cm}^{-3}. \quad (2.6)$$

Being the Fermi level defined by the requirement that the semiconductor is totally neutral, it is possible to calculate the intrinsic Fermi level by equating Eq.2.4a and Eq.2.4b:

$$E_F = \frac{E_C - E_V}{2} + \frac{3kT}{4} \ln \left(\frac{m_n}{m_p} \right). \quad (2.7)$$

The material used for silicon devices is generally not intrinsic. In order to modify its conductivity, additional states are inserted in the forbidden band gap, so that a lower energy is required for hole or electron excitation. This procedure is commonly known as "doping".

Silicon is located in the fourth group of the periodic table, meaning that it has four valence electrons. Elements used to modify its conductivity are generally from group III (i.e. Boron) or group V (i.e. Phosphorus, Arsenic, Antimony) and they either have one valence electron less or more than silicon. The doping procedure can be described as an insertion of shallow energy levels into the band gap, very close to the conduction band for group V elements and very close to the valence band for group III elements.

When using group V elements, the extra electron can be easily released into the conduction band and, for this reason, these elements are called *donors*. At room temperature almost all donor states are ionized and the electron concentration " n " basically equals that of donor atoms " N_D ". The very same reasoning can be applied to group III elements: having one electron less, they can easily trap electrons from the valence band to form a covalent bond with a neighboring silicon atom; this results in a free hole and materials from group III are called *acceptors*. At room temperature, all acceptor atoms are ionized and the hole concentration " p " is equal to the one of acceptor atoms " N_A ".

The conduction of current in a semiconductor depends on the number of free charges, their ability to move and their "motivation" to move. Translating this into mathematical equations, it possible to define the conductivity (σ) and resistivity (ρ) of

doped semiconductors as

$$\sigma = q(\mu_n n + \mu_p p), \quad (2.8a)$$

$$\rho = \frac{1}{q(\mu_n n + \mu_p p)}, \quad (2.8b)$$

where q is the electron charge, μ_n and μ_p are the mobilities of electrons and holes respectively and n and p are the densities of electrons and holes. The mobility is generally defined as

$$\mu = \frac{v_D}{E}, \quad (2.9)$$

where v_D is the drift velocity and E is the electric field. Mobilities of electrons and holes in silicon are different but quite high, making it suitable to realize radiation detectors. In particular electron mobility is equal to $1350 \text{ cm}^2/\text{Vs}$ and holes mobility is equal to $450 \text{ cm}^2/\text{Vs}$. In materials dominated by only one type of impurity (e.g. the donor concentration N_D is much larger than the intrinsic carrier concentration), the following expression for resistivity is valid:

$$\rho = \frac{1}{q(\mu N_D)}. \quad (2.10)$$

The substrate resistivity is actually one of the important parameters when working with silicon detectors and, as will be described in a later section, is strictly related to the device optimal operating voltage.

Considering now the transport of electrical current in a semiconductor, two types of charge movements are present: drift and diffusion.

An electrical current is the motion of charge carriers through a material with a certain direction. In particular the current density can be expressed as:

$$J = qF. \quad (2.11)$$

Charge carriers inside a semiconductor, generally move in a non ordinate way. By applying an external electric field "E", it is possible to give a direction to the charge carriers, generating a flux and, therefore, a current. Considering both electrons and holes contributions, the "drift" current density can be written as

$$J = qF_p + (-q)(-F_n) = qp v_{dp} + qn v_{dn}. \quad (2.12)$$

By inserting the mobility into the previous equation the current densities for electrons and holes become:

$$J_p = qp v_{dp} = qp \mu_p E, \quad (2.13a)$$

$$J_n = qn v_{dn} = qn \mu_n E, \quad (2.13b)$$

an by finally using Eq.2.8a, the total drift current is equal to

$$J = J_p + J_n = q(n\mu_n + p\mu_p) E = \sigma E, \quad (2.14)$$

which essentially corresponds to Ohm's Law.

The other contribution to the current in a semiconductor is the "diffusion" current. It is normally related to carrier concentration gradients inside the material, and derives by the notion that, in case a gradient is present, carriers will diffuse from regions where the density is high to regions where the density is low. The diffusion occurs following first Fick's Law and the contribution to the total current densities for electrons and holes in the mono-dimensional case are:

$$J_p = qD_p \frac{\partial p}{\partial x}, \quad (2.15a)$$

$$J_n = -qD_n \frac{\partial n}{\partial x}, \quad (2.15b)$$

where D_p and D_n are the diffusion coefficients and can be expressed using Einstein's relation:

$$D = \left(\frac{kT}{q} \right) \mu_{n,p}. \quad (2.16)$$

Finally, considering both drift and diffusion contributions, the total current density in a semiconductor becomes:

$$J = J_n + J_p = q(n\mu_n + p\mu_p) E + q \left(D_n \frac{\partial n}{\partial x} - D_p \frac{\partial p}{\partial x} \right). \quad (2.17)$$

Considering now a semiconductor in thermal equilibrium, without exchanges with the external world, the charge carrier concentration in it is constantly balanced by generation and recombination. The thermal generation rate of carriers (G_{th}) does not depend on carriers concentration and is equal to

$$G_{th} = \frac{n_i}{\tau_g}, \quad (2.18)$$

where τ_g is the generation lifetime. The thermal recombination rate (R_{th}) is proportional to the product of the charge carrier concentration, np , and, in thermodynamic equilibrium, it perfectly balances the generation and only depends on the temperature:

$$R_{th} = \beta n_0 p_0 = \beta n_i^2 = G_{th}. \quad (2.19)$$

In presence of exchange with the external world, considering low level injections for which the majority carrier concentration is practically unchanged, the recombination is

limited by the concentration of the minority carriers:

$$R = \frac{\Delta p}{\tau_{r,p}} \quad \text{for n-type silicon,} \quad (2.20a)$$

$$R = \frac{\Delta n}{\tau_{r,n}} \quad \text{for p-type silicon,} \quad (2.20b)$$

with τ_n and τ_p being the recombination lifetimes in n-type and p-type silicon respectively. It is important to notice that τ_g and τ_r can be very different.

In case of excess charge carriers generated in the material, for example by radiation or injection, the product of charge carrier concentrations will exceed the value in Eq.2.5, when the external cause of the generation stops, the thermal equilibrium is reached again by an enhanced recombination, proportional to the concentration of excess minority carriers. This leads to an exponential decay with characteristic time τ_r .

If, instead, charge carriers are removed from the semiconductor, the product of charge carrier concentrations will fall below the value in Eq.2.5. In this case the recombination will remain essentially unchanged because of the lack of carriers. In order to re-establish the thermal equilibrium, generation must come into play. This leads to a return to the equilibrium condition with a time constant τ_g . If the generated carriers are continuously removed, like in a reverse biased diode, the carrier concentration product will remain below n_i^2 and the equilibrium will never be reached. This will translate in a steady generation current (i.e. leakage current).

Charge carrier generation and recombination processes, are very different for *direct gap* semiconductors (e.g. GaAs) and *indirect gap* semiconductors (e.g. Si). In an indirect gap semiconductor, the direct band-to-band recombination is highly suppressed as electrons at the bottom of the conduction band and holes at top of the valence band have different crystal momentum. A direct transmission conserving both energy and momentum is not possible without lattice interactions.

Recombination in Silicon is dominated by the Shockley-Read-Hall (SRH) process which uses the presence of localized energy levels inside the semiconductor band gap as aids to the generation/recombination. These energy levels are caused by imperfection in the silicon lattice or unwanted impurities (e.g. Au, Cu, Fe). The presence of these energy levels has a direct influence on carrier lifetimes, and it is possible to calculate that, levels that most drastically reduce carrier lifetimes in silicon, are located near the middle of the band gap. A complete analysis of SRH theory is not object of this thesis but can be easily found both in literature and in textbooks [26].

2.1.2 P-N junction, important parameters for silicon detectors

In an intrinsic silicon substrate the size of a silicon sensor, there are roughly 10^9 free charge carriers. Normally, only 2×10^4 radiation induced electrons are present, causing the signal to be lost in the higher number of free charge carriers. It is therefore very important to reduce the amount of free charge carriers by several orders of magnitude. To achieve so, different approaches are available but the most common is, probably, the use of p-type and n-type silicon in combination in a reverse-biased pn-junction configuration. The pn-junction is in fact the building block of any silicon sensor.

When a transition between a p-type and an n-type material is present, some of the majority carriers will diffuse from one side to the other, into the region of the opposite doping type. Close to the junction they will recombine with majority carrier coming from the other side of the junction creating a region depleted from free charge carriers. In the vicinity of the junction, donor and acceptor ions are left without their balancing charges, causing this region to be electrically charged and be often referred to as *Space Charge Region (SCR)*. Inside the SCR an electric field is created, counteracting further diffusion of charge carriers from one side of the junction to the other. This electric field is caused by the so-called *built-in potential*.

Assuming an abrupt junction, it is possible to extract electric-field and electrostatic potential distributions around the pn-junction by successive integrations of Poisson's equation:

$$\frac{\partial^2 \Psi}{\partial x^2} = -\frac{dE}{dx} = -\frac{\rho(x)}{\varepsilon_s}, \quad (2.21)$$

where Ψ is the electrostatic potential, E is the electric field, ρ is the resistivity and ε_s is the dielectric constant of silicon. The final value of the built-in potential of an abrupt junction is in first approximation equal to

$$\Psi_0 = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right). \quad (2.22)$$

The value of the built-in potential is, ultimately, the difference of the Fermi potentials between n and p doped materials.

As already stated, in order to be able to detect charges generated from an external source, it is necessary to fully deplete the bulk of the detector. This is done by applying an external potential to the junction, in the same direction as the built-in potential, to further remove charge carriers and extend the SCR to the entire device. The width of the depleted layer, the electric field and electrostatic potential distributions as functions of the applied bias potential, can be again extracted from the integration of Poisson's

equation. In particular the width of the depletion layer can be calculated as:

$$w = \sqrt{\frac{2\varepsilon_s}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_{bias} + \Psi_0)}. \quad (2.23)$$

Taking the doping levels in consideration, the silicon bulk of silicon detectors is generally low-doped ($\sim 10^{12} \text{ cm}^{-3}$) while the implant acting as electrodes are generally very highly doped ($> 10^{18} \text{ cm}^{-3}$). Assuming an n-type bulk material it is possible to neglect the $1/N_A$ term in Eq.2.23. Moreover, the built-in potential is generally considerably lower than the externally applied voltage ($\sim 0.5 \text{ V}$ versus $\sim 50 \text{ V}$). These assumption leads to a simplification of Eq.2.23

$$w \simeq \sqrt{\frac{2\varepsilon_s}{qN_D} V_{bias}}. \quad (2.24)$$

The maximum electric field value inside a typical pn-junction device, is located at the junction and is equal to

$$E_{max} = \frac{2V_{bias}}{w} \simeq \sqrt{\frac{2qN_D}{\varepsilon_s} V_{bias}}, \quad (2.25)$$

and it decreases linearly toward the end of the SCR. The linearity is related to the presence of a constant doping in the silicon bulk while the maximum value is proportional to peak of the doping concentration at the junction.

The full depletion voltage V_{fd} , is the external voltage needed to extend the SCR to the entire thickness of the silicon substrate. As expressed in Eq.2.23, V_{fd} is related to the square of the wafer thickness. If the applied bias voltage exceeds the full depletion voltage, the device is said to be *overdepleted*. In absence of external generation, the steady state *leakage* or *dark* current of the device has multiple components: (i) the diffusion of free carriers from the undepleted volume into the SCR and (ii) the thermal generation at generation-recombination centers at the surface and in the depleted bulk of the device. The second contribution normally dominates the first and the leakage current of a reverse biased pn-junction can be approximated to:

$$J_{vol} \simeq -q \frac{n_i}{\tau_g} w \simeq -q \frac{n_i}{\tau_g} \sqrt{\frac{2\varepsilon_s}{qN_D} V_{bias}}, \quad (2.26)$$

where J_{vol} is the volume generation current per unit area, τ_g is the carrier generation lifetime and n_i is the intrinsic carrier concentration. Increasing the bias voltage of the devices will result in an increase of the leakage current until the silicon bulk is completely depleted, when the current saturates (see Fig.2.1). This is a first method of estimating the full depletion voltage in a real device. The reverse current of the pn-junction is proportional to the temperature and this proportionality is hidden inside n_i and τ_g leading to

$$J_{vol} \propto T^2 e^{-E_g(T)/2kT}. \quad (2.27)$$

This suggests that, by cooling the device during operation, it is possible to reduce its reverse current. The current at a temperature T_2 , can be estimated from the current at a temperature T_1 by applying the following equation:

$$\frac{I(T_2)}{I(T_1)} = \left(\frac{T_2}{T_1}\right)^2 \exp\left[-\frac{E_g}{2k} \left(\frac{T_1 - T_2}{T_1 T_2}\right)\right], \quad (2.28)$$

where $E_g=1.12$ eV is the silicon band gap energy and the Boltzmann's constant k is expressed in eV/K. A rough estimation can be made assuming that the volume current doubles every 7°K .

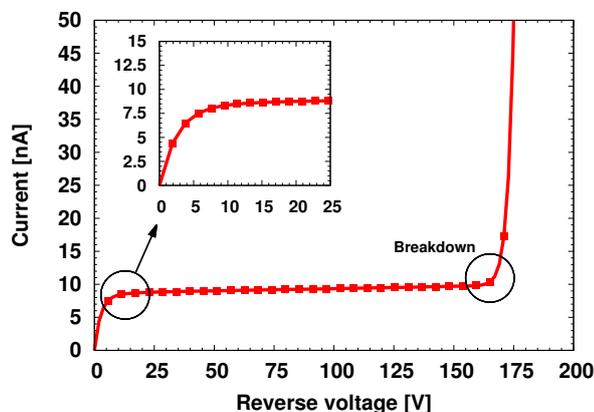


Figure 2.1: Current of a semiconductor diode in reverse bias.

Increasing the bias voltage to very high values will cause the electric field at the junction to reach the critical value triggering the so called avalanche breakdown effect. This effect is related to the kinetic energy gained by free carriers thermally generated inside the material: a free electron under the influence of a strong electric field will be accelerated to very high speed gaining sufficient energy to break the covalent bond of another electron in the silicon lattice by colliding with it. This mechanism is called impact ionization and the released electron will be subjected to the same process. When the field is sufficiently high, the avalanche effect is self sustained and leads to a large increase in the reverse current of the device (see Fig.2.1). If the current reaches very high value for sufficiently high bias voltages, the power dissipated in the sensor ($P=VI$) can be enough to destroy it. As will be described in later chapter, this becomes an issue especially in presence of radiation damage: due to the very high operating voltages and currents the sensor can suffer from a uncontrollable self heating mechanism, also known as *thermal runaway*.

It is possible to calculate the maximum operating voltage (V_B) for a silicon device

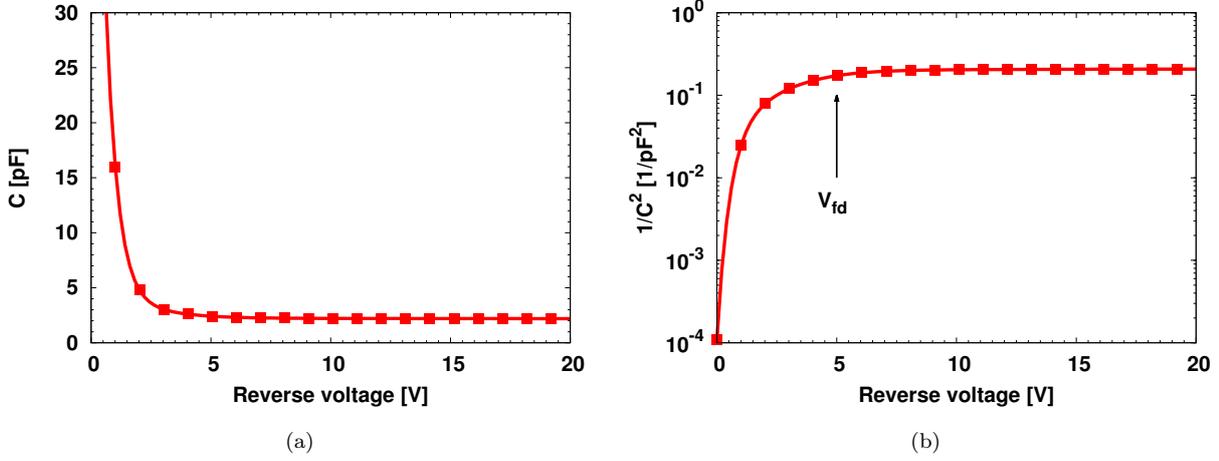


Figure 2.2: Capacitance measurements on a silicon diode, capacitance versus reverse voltage (a) and $1/C^2$ versus reverse voltage (b).

by isolating V_{bias} in Eq.2.25:

$$V_B \simeq \frac{\varepsilon_s}{2qN_D} E_B^2, \quad (2.29)$$

where N_D is the doping concentration of the less doped region of the junction, and E_B is the critical electric field for avalanche multiplication in silicon at $T=300^\circ\text{K}$ and its value is $E_B=4 \times 10^5$ V/cm.

The full capacitance of a pn-junction silicon device, can be calculated assimilating the two planes of the SCR to the parallel plates of a capacitor with a silicon dielectric. The capacitance can therefore be described by the following equation

$$C = \varepsilon_s \frac{A}{d}. \quad (2.30)$$

As the bias voltage increases, the SCR increases its extension (d increases with A remaining roughly constant) and therefore the total capacitance of the device decreases. The bulk capacitance of a silicon device can be approximated with the following formula for two separate cases:

$$C_{bulk} = \begin{cases} A \sqrt{\frac{\varepsilon_s}{2\rho\mu V_{bias}}}, & V_{bias} \leq V_{fd} \\ A \frac{\varepsilon_s}{w_{depl}} = \text{const.}, & V_{bias} > V_{fd} \end{cases} \quad (2.31)$$

Measuring the device capacitance is another way of estimating the full depletion voltage: when the device is fully depleted the capacitance saturates to its minimum. This is even more evident looking at the $1/C^2$ curve. An example is reported in Fig.2.2(a).

2.2 Silicon devices for particle tracking

Since many years, silicon is one of the most used materials in tracking detectors. Several geometrical implementations are available, allowing to obtain the desired informations in terms of particle crossing position, or amount of energy released or both.

2.2.1 Ionization of Silicon

Charged particles moving through matter interact with the electrons of the atoms in the material. This interaction ionizes the atoms leading to an energy loss of the traveling particle. The basic principle of all tracking devices, is to detect the free charges resulting from the ionization of a medium from a passing charged particle. The Bethe-Bloch formula is used to estimate the average energy loss of a charged particle in a medium:

$$-\frac{dE}{dx} = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} \right) - \beta^2 - \frac{\delta(\gamma)}{2} \right], \quad (2.32)$$

where z is the charge of the incident particle, T_{max} the maximum kinetic energy which can be imparted to a free electron in a single collision, I the mean excitation energy, Z the atomic number and A the atomic mass of the considered material, N_A Avogadro's number, m_e the electron mass, c the speed of light, r_e the classical electron radius, $\beta = v/c$, $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ and δ are the density effect correction. An example of the application of this equation is given in Fig.2.3, where the stopping power of different materials on different particles is plotted. The most important region of this plot is the minimum present at $\beta\gamma \simeq 3$, which expresses the minimum energy deposited in the medium. Particles providing such energy loss are called Minimum Ionizing Particles (MIPs) and each detector system must have an intrinsic noise lower enough to detect these "worst-case" particles.

The complete analysis of these kind of phenomena is not object of this thesis but some additional remarks are important for later discussions. When a particle interacts with a material some statistical fluctuations in the number of collisions and energy transfer per scattering are present. The first phenomena is generally modeled with a Poisson distribution, while the second is described with a "straggling function". In rare cases, δ -rays or δ -electrons produced by the interaction, have sufficient energy to become ionizing particles themselves and are responsible for an asymmetry in the collected spectrum, with a longer tail toward higher energies. The resulting spectrum distribution is known as *Landau distribution* [27]. The most probable value of energy transfer is generally about 30% lower than the average value.

In silicon, the average energy needed to create an electron-hole pair is 3.6 eV, about three times larger than the band gap, because part of the energy is needed for phonons creation. For a MIP, the most probable number of generated electron-hole pairs in one

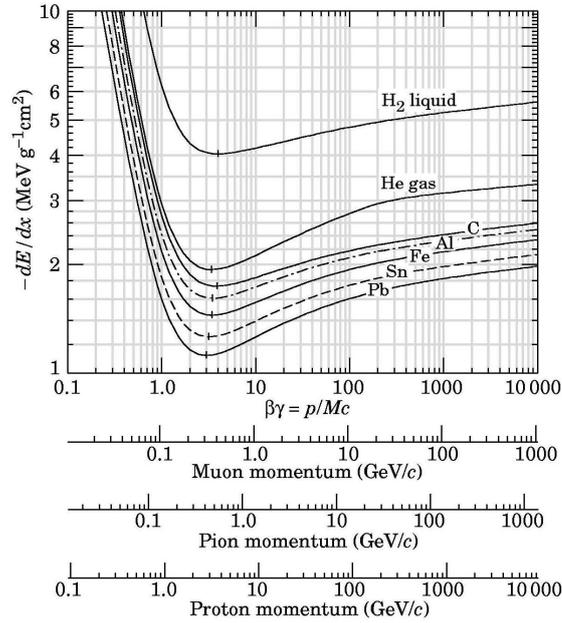


Figure 2.3: Energy loss of different particles in different materials as a function of their energy.

micron is 76, with an average value of 108. If a 300 μm thick silicon sensors is taken as example, the transit of a MIP will result in a most probable charge deposited of about 300 $\mu\text{m} \times 76$ corresponding to a total of ~ 22800 electrons. The readout system will therefore need to be able to detect a charge of ~ 3.6 fC without problems.

For low-energy particles (or in the presence of very thick absorbers) the velocity of the particle is strongly reduced by the energy loss in the material. This results in an increased ionization as shown in Fig.2.3. If the particle is completely stopped inside the medium, most of its energy is released near the end of the trajectory. This effect is called *Bragg peak* and is often used in very specific applications like proton therapy, to deliver the desired radiation dose to the tumor while reducing to a minimum the damage to the healthy tissue.

Another example of short lived particles come from α -particles. They have very large charge and low speed, resulting in a penetration of just a few microns in silicon, with most of the charge released close to the stopping point.

An important effect to consider when tracking particles, is the so called *Multiple Scattering*. The trajectory of a particle traversing a medium is deviated (scattered) multiple times by small angles, mainly due to Coulomb interaction with the nuclei of the material. The scattering angle after many interactions, roughly follows a Gaussian distribution [32]

with an rms value of:

$$\theta_{plane}^{rms} = \frac{13.6 \text{ MeV}}{\beta pc} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln \left(\frac{x}{X_0} \right) \right], \quad (2.33)$$

where z is the charge number of the considered particle and x/X_0 is the thickness of the absorption medium in units of radiation length. The angle θ is expressed in rad, the particle momentum p in MeV and the velocity β in units of the velocity of light c . The radiation length X_0 of silicon is 9.36 cm. As an example, a pixel detector built for LHC experiments, has a thickness of about 2% of a radiation length per layer, changing the trajectory of a 1 GeV particle by an angle of about 0.1 rad.

Besides detecting charged particles (feature used in high energy physics), silicon is sensible to electromagnetic radiation from the visible light up to the X-ray range, making it useful for several other application like photo cameras or medical imaging.

Photons interact with silicon mainly via three different processes: (i) photoelectric effect, (ii) Compton effect and (iii) pair production. In the photoelectric absorption and pair production modes, the photon is completely absorbed while in Compton mode is scattered by a large angle. A monochromatic photon beam penetrating through a material is not changed in energy but attenuated according to Beer's law

$$I(x) = I_0 e^{-x/\mu}, \quad (2.34)$$

whit I_0 being the beam intensity before the interaction with the medium and $I(x)$ after traversing a material of thickness x . The attenuation length μ is a property of the material and depends on the photon energy. Fig.2.4 shows the probability of photon interaction in a 300 μm silicon layer as a function of the photon energy comparing it with the one for CdTe to show the difference between silicon and high- Z materials.

2.2.2 Charge motion and signal formation

Radiation interacting with silicon, can generate electron-hole pairs in the material. As previously stated in subsection 2.1.1, free carriers in silicon can be transported through two different processes, *drift* or *diffusion*. The diffusion is typically driven by concentration gradients and charges spread out with time forming a Gaussian distribution with variance

$$\sigma = \sqrt{Dt} \quad (2.35)$$

where D is a material dependent diffusion constant and t the time.

In presence of an electric field, carriers drift with a direction parallel to the field itself. The velocity of free carriers in silicon can be expressed as

$$\boldsymbol{\nu} = \mu_{n,p} \mathbf{E}, \quad (2.36)$$

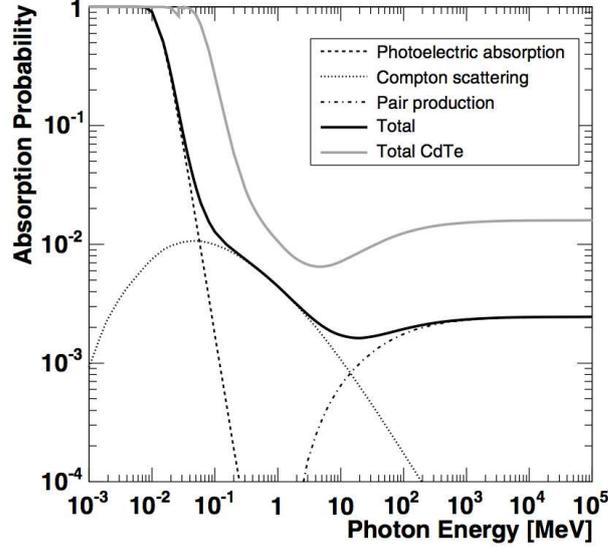


Figure 2.4: Probability of photon absorption in a 300 μm silicon layer as function of the photon energy. For comparison with high- Z materials, the same function is plotted for CdTe [30].

where $\mu_{n,p}$ is the mobility of electrons and holes respectively.

Electrons and holes move in silicon in different directions but their contribution to the signal current has the same polarity because they have opposite sign charge. The time a carrier needs to traverse the entire device is referred to as *collection time*. Remembering what was discussed in subsection 2.1.2, a silicon pn-junction device can be considered fully depleted when the extension of the SCR is equal to the entire thickness of the bulk, condition that occurs when the applied bias voltage equals

$$V_{fd} \simeq \frac{qN_D d^2}{2\epsilon_s}, \quad (2.37)$$

where d is the substrate thickness and the built-in voltage is neglected because considerably lower than the applied bias voltage. In full depletion conditions, the electric field drops from its maximum at the junction to zero at the contact on the opposite side. When the device is operated in over-bias, the field distribution can be expressed as

$$E(x) \simeq \frac{2V_{fd}}{d} \left(1 - \frac{x}{d}\right) + \frac{V_{bias} - V_{fd}}{d}. \quad (2.38)$$

If the applied excess bias is considerably larger than the full depletion voltage (V_{fd}), the electric field distribution can be considered constant and equal to $E(x) = V_{bias}/d$. Fig.2.5 shows the distribution of the electric field inside a pn-junction device both in under and over-depletion.

A common misconception is that free carriers generated by impinging radiation in a silicon device, induce signal on its electrodes only when they are collected. On the

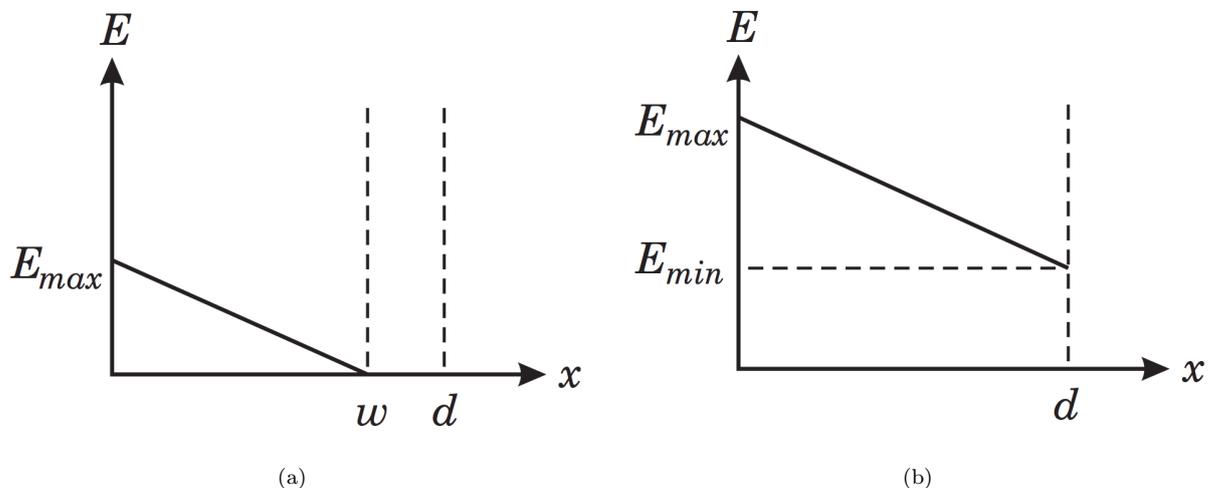


Figure 2.5: Electric field distribution in a non-depleted pn-junction (a) and in an over-depleted pn-junction (b) [29].

contrary, the signal is induced as soon as the carrier starts moving inside the material. This concept was first formally described by S. Ramo with the following equation:

$$i(t) = -q\vec{v}(t) \cdot \vec{E}_W, \quad (2.39)$$

where q is the net charge moving in the material with a velocity \vec{v} , and \vec{E}_W is the weighting field [33]. A very important remark needs to be made: *weighting field* and *electric field* are two very different quantities, the electric field determines the charge trajectory and velocity while the weighting field only depends on the geometry and determines how charge motion couples to a specific electrode.

A simple example can be examined by assuming a detector with a parallel plate geometry. In this situation only, electric field and weighting field have the same distribution. Assuming an over-bias situation, the carrier velocity can be calculated as

$$v = \mu E = \mu \frac{V_{bias}}{d}. \quad (2.40)$$

The weighting field is obtained by applying a unit potential to the collection electrode and grounding the other, obtaining

$$E_W = \frac{1}{d}, \quad (2.41)$$

leading to an induced current

$$i = qvE_W = q\mu \frac{V_{bias}}{d} \frac{1}{d} = q\mu \frac{V_{bias}}{d^2}. \quad (2.42)$$

Assuming an electron-hole pair is generated at a coordinate x from the positive electrode,

the collection times for both carriers can be expressed as

$$t_e = \frac{x}{v_e} = \frac{xd}{\mu_e V_{bias}}, \quad (2.43a)$$

$$t_h = \frac{d-x}{v_h} = \frac{(d-x)d}{\mu_h V_{bias}}. \quad (2.43b)$$

The induced charge can consequently be calculated as

$$Q_e = it_e = q\mu_e \frac{V_{bias}}{d^2} \frac{xd}{\mu_e V_{bias}} = q \frac{x}{d}, \quad (2.44a)$$

$$Q_h = it_h = q\mu_h \frac{V_{bias}}{d^2} \frac{(x-d)d}{\mu_h V_{bias}} = q \left(1 - \frac{x}{d}\right). \quad (2.44b)$$

The charge measured from a silicon detector is therefore strongly influenced by the integration time. If the total integration time is larger than the collection time of all carriers, then the measured charge will correspond to the full charge, otherwise part of the charge will be lost causing the so-called *ballistic deficit*.

2.2.3 Position sensing

A simple semiconductor diode with only two electrodes, will only return a sort of "digital" information, meaning that it will only detect the passage of a particle but not its position, or at least not with the required precision.

In order to overcome this limitation, different sensor topologies are available, mainly differing on the positioning of the readout electrodes and their segmentation.

Strip detectors

By segmenting the electrodes of a silicon device into strips, it is possible to obtain a 1D position information. Fig.2.6(a) shows the geometrical configuration of a single-sided strip detector. Depending on the track inclination one or more strips can sense the generated charge. By evaluating the magnitude of the signal on neighboring strip, it is possible to obtain a precision higher than the strip pitch.

In order to obtain a 2D position information, it is necessary to orthogonally segment the electrodes on the opposite detector side as well, as shown in Fig.2.6(b). This second configuration is relatively simple with respect to other available solutions but it leads to some problems when the detector is operated with high hit densities. Each hit generates both an x and y coordinate. In case n hits occur in a short time, n pair of coordinates will be generated, simulating a total of n^2 hits, $n^2 - n$ of which are fake.

A way of overcoming this, is to use a small stereo angle between opposite side strips instead of 90° as shown in Fig.2.6(c). If the strips are orthogonally placed, the capture

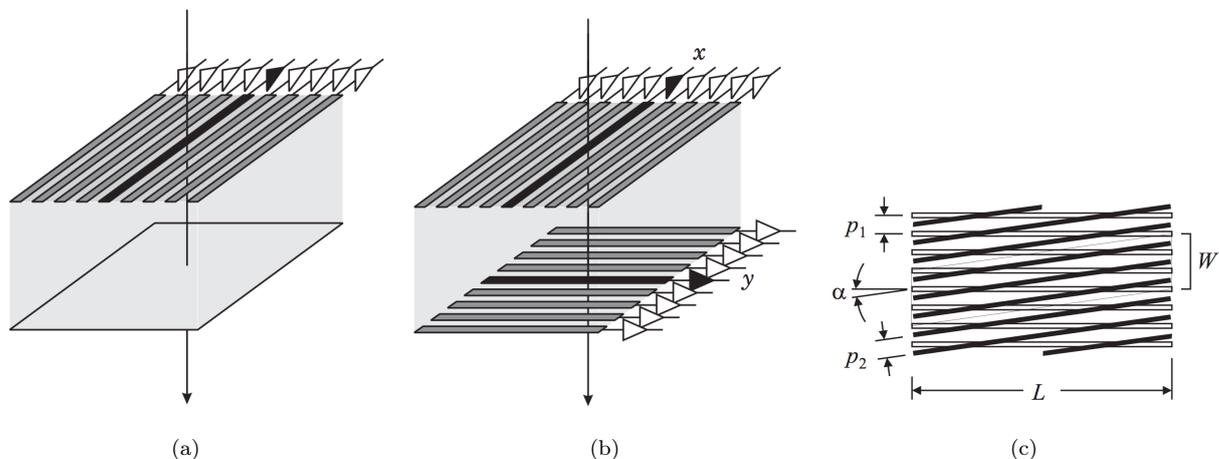


Figure 2.6: Electrode segmentation in a strip detector: single sided segmentation (a), double sided segmentation (b) and small stereo angle between strips on opposite sides (c) [29].

area will be $A=L_1L_2$, where L_1 and L_2 are the lengths of the considered strips, and a hit in a given strip can form combinations with all the traversing strips. If the angle α is, instead, very small, the capture area is reduced to

$$A \simeq L^2 \frac{p_1}{p_2} \tan \alpha + Lp_2. \quad (2.45)$$

In this case, the probability of multiple hits within the acceptance area is reduced as α gets smaller. The disadvantage of this solution is that making α smaller will affect the longitudinal resolution in a negative way.

Pixel detectors

Another way of obtaining 2D information is to realize so called pixel detectors. In this case the electrodes are segmented mimicking a check board and are read-out with a matching readout chip. This type of sensors are generally called *hybrid* pixel detectors. The chip is typically connected to the sensor through small solder bumps. The main limitation to pixel size usually comes from the electronics, because a large amount of circuitry must be fit in a single pixel with complexity changing depending on the type readout to be implemented. Fig.2.7 shows an implementation of this concept.

2.2.4 Position resolution

The spatial resolution of a segmented tracking device, is determined by the electrode pitch (strip or pixel). Several parameters such as readout mode (analog or single threshold binary), reconstruction algorithm and charge sharing among electrodes, also play an

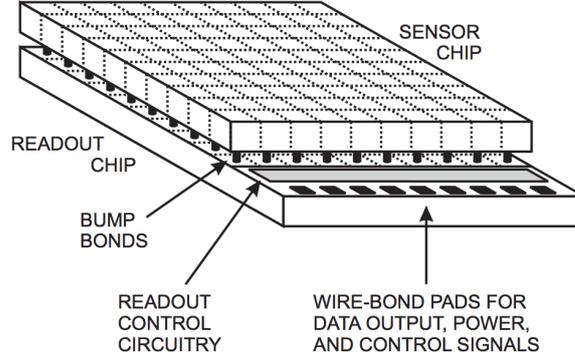


Figure 2.7: Sketch of the connection of an hybrid pixel sensor to its readout chip through bump bonds. The wire bond pads to connect the chip to the external system are also shown [29].

important role on position resolution. In this section two different readout mode are examined.

Binary readout

In the case of a single threshold binary readout, the spatial resolution is fairly easy to calculate. As first order approximation it is possible to consider a pixel detector with pixel pitch p around a position 0. A very similar calculation, leading to the same result, is valid for strip detector with the same inter-strip pitch.

In this readout mode the threshold is adjusted in a way that only one pixel per particle track will fire, that is, only particles crossing the detector between $-p/2$ and $p/2$ will trigger a signal in the pixel when the detector is hit by a uniform density of particles $D(x)=1$. It is possible to calculate the average difference between the *real* impact position x_r and measured impact position $x_m=0$ with the equation

$$\sigma_{position}^2 = \frac{\int_{-p/2}^{p/2} (x_r - x_m)^2 D(x_r) dx_r}{\int_{-p/2}^{p/2} D(x_r) dx_r} = \frac{\int_{-p/2}^{p/2} x_r^2 1 dx_r}{\int_{-p/2}^{p/2} 1 dx_r} = \frac{d^2}{12}, \quad (2.46)$$

leading to a spatial resolution of

$$\sigma_{position} = \frac{p}{\sqrt{12}} = 0.28p. \quad (2.47)$$

The threshold is normally set to the lowest value that will assure the lowest number of spurious hits caused by electronic noise. It is therefore possible for a particle traversing more than one pixel or strip, to trigger more than one readout channel. This process is commonly known as *charge sharing*. Charge sharing helps in increasing the position resolution because it is possible to calculate the center of gravity of the considered hit by averaging the position of all the channel in a single cluster. Despite charge sharing being

considered an important phenomena, in some critical cases it might be a disadvantage: for some particular hit conditions (e.g. large angles) the charge might be shared among several channels, leading to the possibility than none of them will reach the threshold. This is generally not a problem before irradiation, but, after irradiation, when charge trapping becomes non negligible, this can be an issue.

Analog readout

Complementing the binary readout with signal information coming from each channel, the position resolution can be considerably improved. As will be described later, some readout circuits can provide an output signal which amplitude is proportional to the amount of collected charge. Using pulse height information from each channel involved in a single hit, an algorithm can be applied to better determine the hit position. Considering two firing channels (strip1 and strip2), it is possible to calculate the so called η -function using their respective pulse height (PH_1 and PH_2) informations:

$$\eta = \frac{PH_1}{PH_1 + PH_2}. \quad (2.48)$$

The hit position is then calculated as

$$x = x_1 + \frac{PH_2}{PH_1 + PH_2}(x_2 - x_1) = \frac{PH_1x_1 + PH_2x_2}{PH_1 + PH_2}, \quad (2.49)$$

with a position resolution strictly dependent on the signal to noise ratio (S/N) and equal to

$$\sigma \propto \frac{p}{S/N} \quad (2.50)$$

As an example, applying this calculation to a strip sensor with pitch $p=25\mu\text{m}$ and a signal to noise ratio equal to 50, the obtainable position resolution is equal to $\sigma \sim 2\text{-}4\mu\text{m}$. More information about this algorithm can be found in [34].

2.3 Read-out electronics for silicon radiation detectors and noise

The readout electronics for radiation detectors is available in a large amount of different configurations. For the purpose of this thesis only the basic and most relevant configurations will be examined in order to show how different parameters affect the noise.

2.3.1 Current-sensitive amplifier

The first readout architecture that will be examined is the so called *current-sensitive amplifier*. This particular amplifier is used to convert the current signal coming from a detector to a voltage and amplify it.

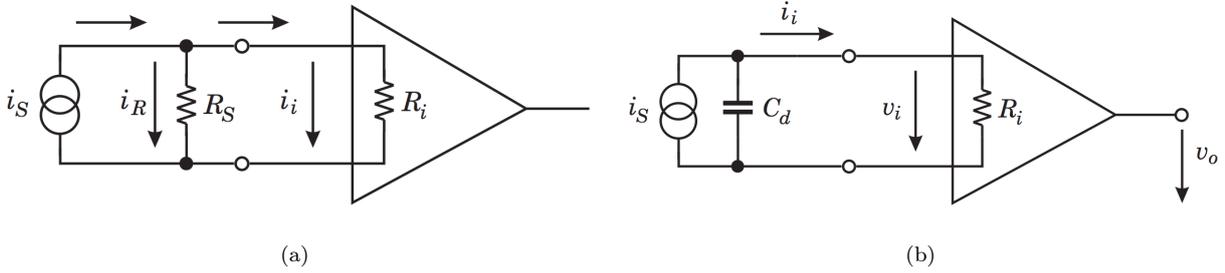


Figure 2.8: Current-sensitive amplifier with input current source and parallel resistor (a) and with capacitive input (b)[29].

As first approximation a current-sensitive amplifier can be assimilated to the circuit shown in Fig.2.8(a). The signal source i_s is a current generator with its parallel resistance R_s . The input resistance of the amplifier is R_i . In the considered configuration the source current will split between R_s and R_i in the following way

$$i_i = \frac{R_s}{R_s + R_i} \cdot i_s. \quad (2.51)$$

In order to assure that the input current is representative of the source current ($i_i \simeq i_s$), it is required that $R_i \ll R_s$. At the same time, in order to allow current drive to other following stage, an high output resistance is required.

In presence of a silicon detector, the proper modeling of the situation is represented in Fig.2.8(b) by the presence of a current source with a parallel capacitor C_d . When a particle impinges the device the current is represented by a fast pulse than can, in first approximation, be modeled with square wave of amplitude i_s and duration t_c . The total collected charge can therefore be calculated as $Q_s = \int i_s(t) dt = i_s t_c$. When the amplifier is operated in current sensitive mode, the collection time t_c is normally much lower than the time constant given by $R_i C_d$. In this way the sensor capacitance discharges rapidly and the output voltage is proportional to the input current or $v_o \propto i_s(t)$. For this reason the shape of the input signal is unaltered. This type of amplifier is often used in the Transient Current Technique (TCT), where some excitation is provided to the sensor in a very specific position and the evolution of the signal is observed. Different impinging positions will result in different signal shapes allowing to properly estimate the charge collection dynamics of the device under test.

2.3.2 Charge Sensitive Amplifiers (CSA)

When instead of the shape of the signal one is interested in measuring the total collected charge, an integrating amplifier is required. The Charge Sensitive Amplifier (CSA) provides

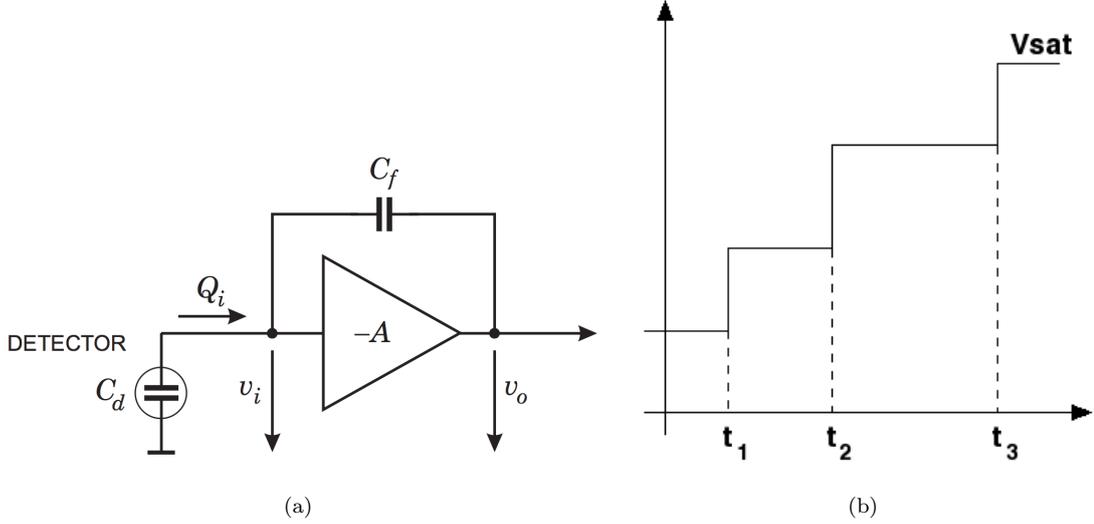


Figure 2.9: Ideal Charge Sensitive Amplifier configuration [29] (a) and output voltage saturation without reset circuit (b).

a measure of the sensor current integral by giving an output voltage signal proportional to the amount of charge collected from the sensor.

The basic block of CSA is an inverting voltage amplifier as shown in Fig.2.9(a) with infinite input resistance and voltage gain $dv_o/dv_i = -A$. The feedback is realized with a capacitor C_f that is used as integrating element. Since no current can flow inside the amplifier ($R_i = \infty$), the voltage across C_f can be calculated as

$$v_f = v_i - v_o = v_i + Av_i = v_i(A + 1), \quad (2.52)$$

and the charge stored on C_f is therefore

$$Q_f = C_f v_f = C_f(A + 1)v_i. \quad (2.53)$$

Because no current flows in the amplifier, the charge stored on the feedback capacitor is equivalent to the total input charge ($Q_f = Q_i$). The amplifier therefore presents a dynamic input capacitance equal to

$$C_i = \frac{Q_i}{v_i} = C_f(A + 1). \quad (2.54)$$

The output voltage per unit charge is expressed as

$$A_Q = \frac{v_o}{Q_i} = \frac{Av_i}{C_i v_i} = \frac{A}{C_i} = \frac{A}{A + 1} \cdot \frac{1}{C_f} \approx \frac{1}{C_f}, \quad (\text{with } A \gg 1), \quad (2.55)$$

which means that the charge gain of the amplifier is determined by C_f which is a very well controlled quantity.

When a current pulse reaches the input of the CSA a variation of the output voltage is observed; this variation will be equal to $\Delta V_o = \Delta Q_i / C_f$. In the ideal case shown in Fig.2.9(a), only a capacitor is present on the feedback. When a second current pulse reaches the input, another voltage shift will be observed on the output. If this happens several times, the output of the amplifier will reach saturation (Fig.2.9(b)). For this reason, it is very important to implement feedback reset mechanism that will fix the DC operating point of the CSA and prevent saturation removing charge from C_f , restoring the initial condition. Since, in many cases, further filtering will be present after the CSA, the discharge of C_f is voluntarily kept slow. The reset can be implemented with different methods and the two most famous one are: (i) a simple resistor and (ii) a transistor providing constant current discharge. The first method is very simple and probably the most used while the second is implemented in more modern readout chips like the FE-I3 and FE-I4. As an example, considering a resistor reset with a target reset time of $\tau=1 \mu\text{s}$ and a feedback capacitance $C_f=10 \text{ fF}$, the needed resistor will be equal to $R_f=\tau/C_f=100 \text{ M}\Omega$.

Most pixel devices are normally DC coupled to the readout (strips are generally AC coupled), meaning that the input channel must be able to withstand currents that can reach, after irradiation, several tens of nano amperes. If no countermeasure is taken, the input current will flow through the feedback resistor causing a large variation on the output DC voltage. Assuming a pixel leakage current $I_{LK}=10 \text{ nA}$ and a feedback resistor $R_f=100 \text{ M}\Omega$, the total voltage drop across R_f will be 1V. This is obviously something one would like to avoid. A current sink can be implemented at the input stage by subtracting a constant current determined from measurements on dummy pixels.

An additional feature of the CSA is the ability to provide ease of charge calibration by means of a very simple injection circuit (Fig.2.10). If $C_T \ll C_i$, the voltage difference on the test input is completely applied on C_T injecting a charge equal to Q_T in the input of the CSA, and in particular:

$$Q_T = \frac{C_T}{1 + \frac{C_T}{C_i + C_d}} \cdot \Delta V \approx C_T \left(1 - \frac{C_T}{C_i + C_d} \right) \Delta V. \quad (2.56)$$

The calibration must, therefore, be performed with the detector connected. Additional information on Charge Sensitive Amplifiers can be found in [29].

2.3.3 Shaping Amplifiers

As demonstrated in the previous subsection, the output voltage of a CSA is proportional to the charge injected in the input stage. Spectroscopy systems usually collect statistics on the amplitude of the output signal to extract the spectrum of the radiation source used. In order to limit the influence of noise on the system, further filtering is needed after the

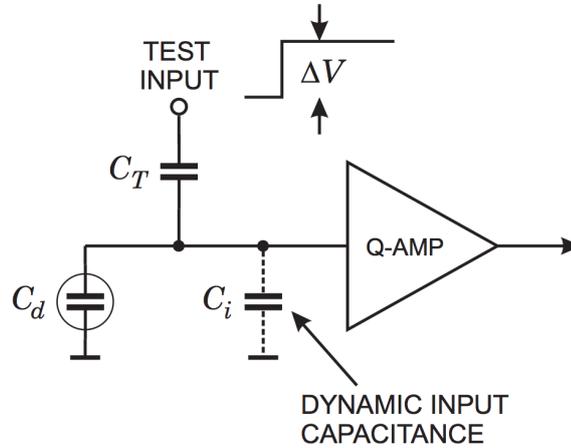


Figure 2.10: Charge Sensitive Amplifier with test input (C_t) for charge calibration purposes [29].

CSA. This technique is known as *pulse shaping* because the shape of the output voltage is modified to obtain the required timing or noise performance.

A simple shaping amplifier can be assimilated to a band-pass filter with well defined low and high cut-off frequencies ($f_{c,L}$ and $f_{c,H}$), limiting the total CSA signal band thus reducing low and high frequency noise. A band-pass filter is composed by several stages, usually a high-pass stage (referred to as *differentiator*) which sets the duration of the pulse and low-pass stage (referred to as *integrator*) which increases the rise time to limit the noise bandwidth.

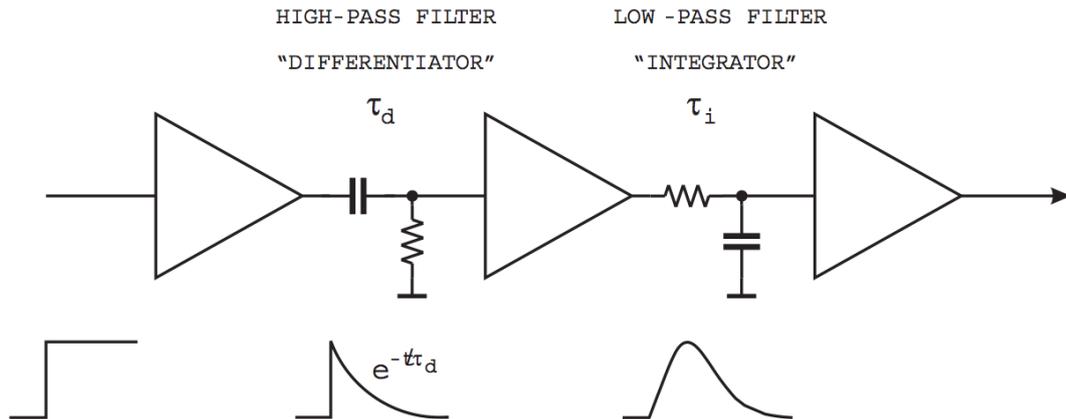


Figure 2.11: Basic scheme of a CR-RC shaper. The different stages are separated by buffers. [29].

The simplest pulse shaper is the so-called CR-RC shaper shown in Fig.2.11, implementing the differentiation and integration stages with discrete components. The analysis of the operation of this particular circuit is rather simple, its total frequency response is

given by

$$G(f) = G_d(f) \cdot G_i(f), \quad (2.57)$$

where $G_d(f)$ and $G_i(f)$ are the frequency responses of the differentiation and integration stages respectively. Signal processing theory demonstrates that a product in the frequency domain becomes a convolution in the time domain

$$g(t) = g_1(t) * g_2(t) = \int_{-\infty}^{\infty} g_1(\tau)g_2(t - \tau)d\tau. \quad (2.58)$$

The voltage output of shaping amplifier can therefore be calculated as

$$V_o(t) = V_i(t) * g_i(t) * g_d(t), \quad (2.59)$$

and in the examined case (CR-RC), the response to the unit step becomes

$$V_o(t) = \frac{\tau_d}{\tau_d - \tau_i} [e^{-t/\tau_d} - e^{-t/\tau_i}], \quad (2.60)$$

which, if $\tau_d = \tau_i = \tau$, becomes

$$V_o(t) = \left(\frac{t}{\tau}\right) e^{-t/\tau}. \quad (2.61)$$

The output signal has a fast rise and slower decay and reaches its maximum at the characteristic time $\tau = T_P$, also known as *peaking time*. As will be explained later, the peaking time has a strong effect on the noise of the system and, as a rule of thumb, with a fixed integration time, is best to have $\tau_d = \tau_i = \tau$.

Since in CR-RC shapers the return to baseline is rather slow, more symmetry in the pulse can be achieved by implementing n integration stages, leading to an output pulse equal to

$$V_o(t) = \left(\frac{t}{\tau}\right)^n e^{-t/\tau}, \quad (2.62)$$

where care must be taken to modify the integration time to $\tau = \tau_{n=1}/n$ in order to maintain the desired peaking time.

The theory behind signal processing can be quite complicated and it is not object of this thesis. Several different additional techniques can be implemented such as, baseline restoration, pole-zero cancelation and several others. More details are available in [29].

2.3.4 Equivalent Noise Charge (ENC)

The minimum detectable signal and the precision of the amplitude measurement are limited by fluctuations. Even considering a fixed energy absorption in the detector, the average number of generated e-h pairs $N = E_{ph}/E_i$ is not constant. The fraction of deposited energy

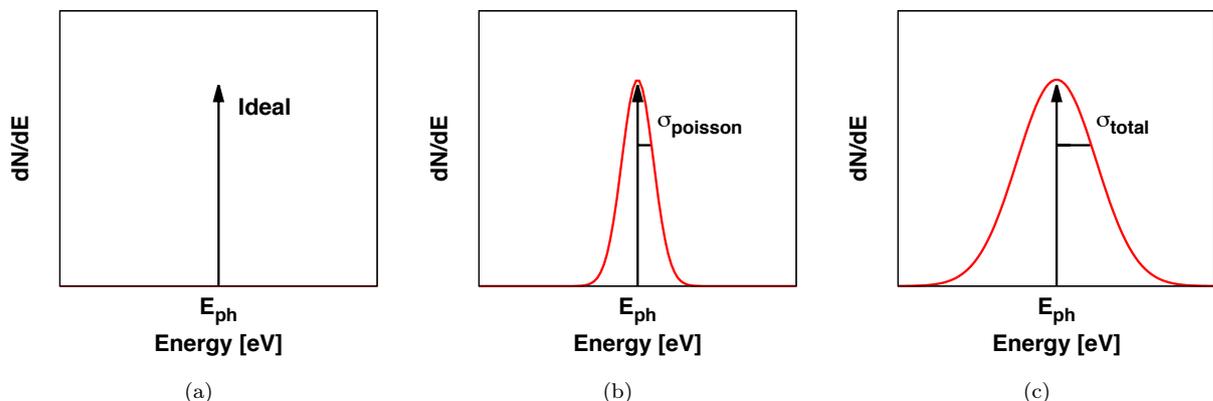


Figure 2.12: Ideal spectrum measurement without fluctuations (a) with poisson (b) and with both poisson and electronics fluctuation.

required for e-h separation and phonon generation is subject to fluctuation which cause N to vary

$$\langle \Delta N^2 \rangle = FN = F \frac{E_{ph}}{E_i}, \quad (2.63)$$

where F is known as Fano factor and its value in silicon is $F \simeq 0.12$. These fluctuations are assimilable to a Poisson process with variance

$$\sigma_Q = \sqrt{F \frac{E_{ph}}{E_i}}. \quad (2.64)$$

In addition to signal fluctuation, the energy resolution is degraded by fluctuation in electronics that cause baseline shifts and degrade the peak amplitude and time dependence. Electronic noise is usually referred to as white and gaussian. An example of an ideal spectrum measurement compared with situations in presence of fluctuations is shown in Fig.2.12.

The resolution of a detection system is usually expressed using the Full Width at Half Maximum (FWHM) of the measured spectral peak. The FWHM is directly proportional to the variance with the formula $FWHM = 2.354\sigma_{tot}$.

The total noise of the system is expressed in terms of *Equivalent Noise Charge* (ENC) which corresponds to the amount of charge which, applied to the input, gives a unitary signal to noise ratio. The ENC in silicon devices can be calculated in one the following forms

$$ENC [e^-] = \sigma_{tot} [e^-] = \frac{FWHM [e^-]}{2.354} = \frac{FWHM [eV]}{2.354 \cdot E_i} = \frac{FWHM [eV]}{8.5}. \quad (2.65)$$

The complete study of the ENC of a readout system is rather complicated because it depends on a large number of variables, for this reason only a basic analysis will be performed here, additional details can be found in [35, 36].

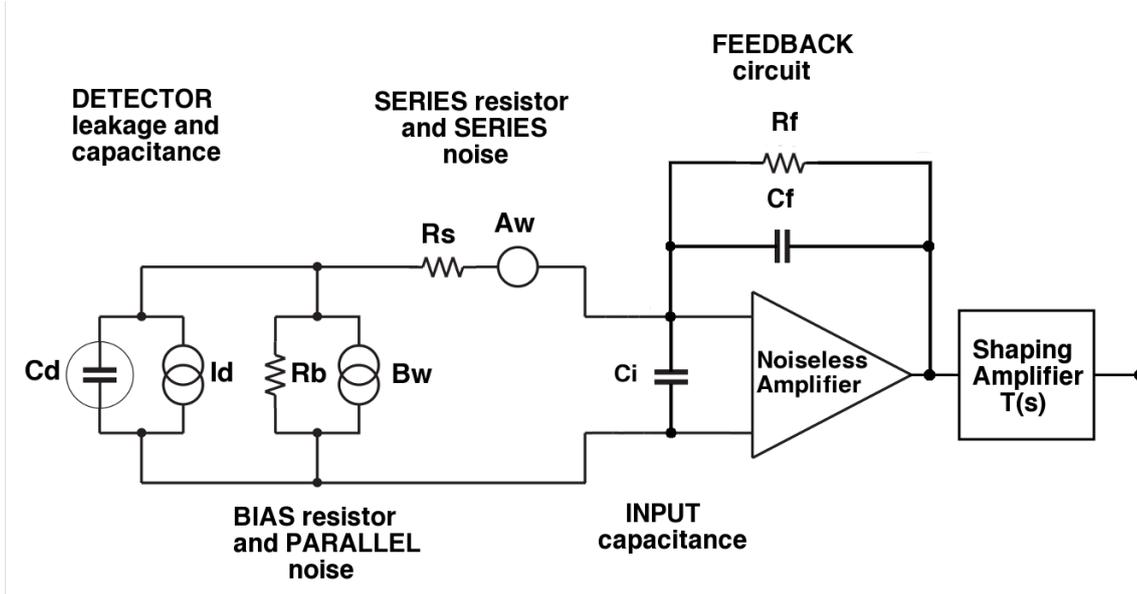


Figure 2.13: Schematic model of all the noise sources in a readout system.

Modeling noise sources in readout electronics

Considering a time invariant system, noise components can be modeled as *white series noise* and *white parallel noise*. Series noise is normally represented with a series voltage generator with amplitude A_W while parallel noise is represented with a parallel current generator with amplitude B_W . In Fig.2.13 both noise source are shown together with other important circuit elements such as the detector capacitance, the input capacitance and the shaping amplifier transfer function $T(s)$. The detector is modeled, as usual, with a pulsed current generator. The response of the considered system to a δ current pulse with area Q coming from the sensor is equal to

$$V_\delta = \frac{Q}{C_f} \cdot \mathcal{L}^{-1} \left[\frac{T(s)}{s} \right]. \quad (2.66)$$

The output mean square noise voltage can be calculated as

$$\overline{v_{u,N}^2} = \int_0^\infty S_u(\omega) df = \int_0^\infty [|T_{A_W}(j\omega)|^2 \cdot S_{A_W}(\omega) + |T_{B_W}(j\omega)|^2 \cdot S_{B_W}(\omega)] df, \quad (2.67)$$

which, after some calculations returns

$$\overline{v_{u,N}^2} = A_W \frac{C_T^2}{C_f^2} \frac{1}{2\pi} \int_0^\infty |T(j\omega)|^2 d\omega + A_f \frac{C_T^2}{C_f^2} \int_0^\infty \frac{|T(j\omega)|^2}{\omega} d\omega + B_W \frac{1}{C_f^2} \frac{1}{2\pi} \int_0^\infty \frac{|T(j\omega)|^2}{\omega^2} d\omega, \quad (2.68)$$

where A_W and B_W are series and parallel white noises respectively, A_f is the $1/f$ noise, $C_T = C_D + C_i + C_f$ is the total capacitance and $T(j\omega)$ is the transfer function of the shaping

filter. From the previous equation it is possible to extract the "shape factors", quantities strictly related to the type of shaping filter being used and that are usually found tabulated in literature:

$$A_1 = T_P \frac{1}{2\pi} \int_0^{\infty} |T(j\omega)|^2 d\omega, \quad (2.69a)$$

$$A_2 = \int_0^{\infty} \frac{|T(j\omega)|^2}{\omega} d\omega, \quad (2.69b)$$

$$A_3 = \frac{1}{T_P} \frac{1}{2\pi} \int_0^{\infty} \frac{|T(j\omega)|^2}{\omega^2} d\omega. \quad (2.69c)$$

The square of the equivalent noise charge is expressed as

$$ENC^2 = \overline{v_{u,N}^2} \cdot C_f^2 = A_W C_T^2 \frac{A_1}{T_P} + A_f C_T^2 A_2 + B_W A_3 T_P. \quad (2.70)$$

Using Eq.2.70 with the correct set of parameters, it is possible to theoretically estimate the noise of almost any readout system. It is very important to notice that, different dependences on the peaking time are present in the three terms of the equation: in particular, the series noise is inversely proportional to T_P and directly proportional to the total capacitance, the parallel noise is directly proportional to T_P while the 1/f noise is not depending on T_P but only on the total capacitance. This is well summarized in Fig.2.14 where the contribution to the ENC of each term, is plotted with respect to peaking time. The sum of the three components returns a total ENC function which is maximum for very fast shaping time, it decreases increasing the shaping time reaching a minimum, and then starts increasing again. By finding the minimum of this function it is possible to determine the ideal peaking time for each system.

In order to better understand how every component of the system affects the noise, the noise contributions to A_W , B_W and A_f are here discussed. The series noise is almost completely contributed by the white noise in the main current of the input transistor of the CSA and, in case is present and relevant, by the stray resistance in series with the input:

$$A_W = 4kT \frac{\Gamma}{g_m} + 4kT R_S, \quad (2.71)$$

where Γ depends on the type of input transistor ($\Gamma=2/3$ for long channel FETs).

Concerning the parallel noise, its main contributions are the shot noise in the detector leakage current, the shot noise in the input transistor gate current, the thermal noise of the feedback resistor of the CSA and the thermal noise of the resistor in detector bias

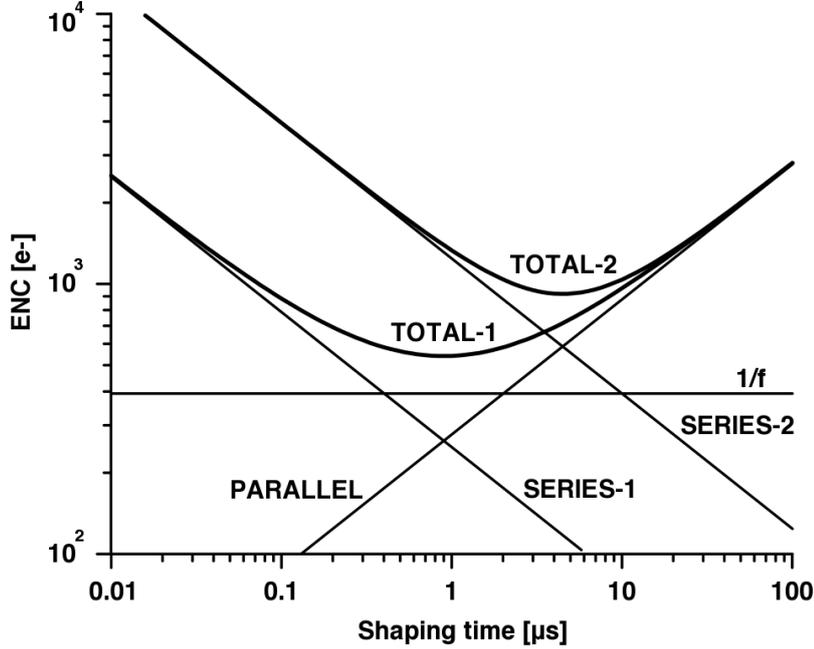


Figure 2.14: Summary of the different contributions to the ENC. Parallel, series and 1/f noise are plotted with respect to the shaping time. The plot also shows how an increase of series noise from SERIES-1 to SERIES-2, moves the minimum of the ENC from TOTAL-1 to TOTAL-2 [29].

filter:

$$B_W = 2qI_D + 2qI_G + \frac{4kT}{R_f} + \frac{4kT}{R_{bias}}. \quad (2.72)$$

Finally the 1/f noise is only dependent on the type of input device and is generally given in data sheets or extracted from appropriate measurements. As an example, the value of A_f for MOSFETs can be calculated, as reported in [29], with the equation

$$A_f = \frac{K_a}{C_{ox}^2 WL} \quad (2.73)$$

where C_{ox} is the gate-channel capacitance per unit area, K_f is an empirical constant that is device and process dependent and W and L are the width and length of the transistor channel respectively.

Summarizing, the choice of the adequate peaking time is fundamental to reduce the effects of noise. If T_P is chosen to be very short, the detector capacitance will play a very important role together with the drain current of the input stage, on the other hand, if the peaking time is long the leakage current of the sensor and the gate current of the transistor will be dominant. It is therefore crucial to wisely chose the peaking time, if at all possible. However, this is not possible in all the applications, and in particular in high energy physics experiments, where the peaking time is strongly limited by the

bunch crossing which can be very short (25 ns at LHC) causing the noise to be strongly dependent on detector capacitance.

2.4 The bump bonding and flip-chip process

Sensors and electronics for high energy physics experiments, need to be assembled together to form a module that will later be installed on the staves used to build the tracking layer of interest. In the specific case of pixel detectors [30], the connection between sensor and readout is performed by means of the so called *bump bonding and flip-chip* process [38].

The use of this technique is increasing as a consequence of the need for compact packaging in the electronics market. Two main technologies are available (and well established), they make use of either electroplated *solder bumps* or *indium bumps* deposited by evaporation. The bump deposition is performed at wafer level while the flip-chip is normally carried out on single dices.

A brief description of both techniques will be given in the following subsections also stating advantages and disadvantages of each technology.

2.4.1 Solder based bump-bonding process

The standard workflow of the solder based bonding process, derives from the Controlled Collapse Chip Connection (C4) process [39] introduced by IBM more than 40 years ago. The maximum bump pitch in this process was 250 μm or higher, not acceptable for most high energy physics applications. This limitation was overcome in the past years with increasing industrial developments [40, 41, 42, 43] thanks to the use of eutectic solder (e.g. 37Pb/Sn). The basic steps of this process are sketched in Fig.2.15 and can be summarized as follows:

- a. From the aluminum contact pad on the IC wafer, first a thin Ti/W adhesion layer (200 nm) and a diffusion barrier are sputtered before the Cu plating base (≈ 300 nm). A wettable 1-5 μm thick Cu metallization follows. This set of layers is known as *Under Bump Metallization (UBM)*.
- b. A photoresist is spin coated and developed to realize the bump pad openings.
- c. The bump deposition process is performed and 37Pb/Sn is deposited through electroplating.
- d. The remaining photoresist is stripped and a wet etching of the plating base is performed leaving only small PbSn cylinders.
- e. The PbSn cylinders are turned into 25 μm diameter spheres by the reflow process performed at temperatures ranging between 250-350 $^{\circ}\text{C}$.

- f. The UBM is also grown on the sensor wafer with the addition of Ni and Au layers for better wettability. The flip-chip is performed and the subsequent reflow process is performed at temperatures never exceeding 350 °C.
- g. The assembly is completed. The distance between the readout IC and the sensor is in the order of 25 μm and the connection resistance is in the order of 1 Ω or less. The ultimate shear stress is ~ 50 MPa

The main disadvantage of the solder bumping is its complexity. To guarantee good adhesion, the UBM deposition must be well controlled. Moreover, the process requires relatively high temperatures, between 250 and 350 °C.

2.4.2 Indium based bump-bonding process

The Indium based bump-bonding technology [44] was developed for infrared sensor arrays, which require good mechanical and electrical connection properties down to liquid nitrogen temperatures. Although the electroplating of indium is feasible, the bumps are normally grown through polyimide masks spun on top of the wafers. The bump pitch can be as low as 30 μm but the bump height is limited to 10 μm . Bumps must be deposited on both the sensor and the electronics because the connection is obtained by an Indium-Indium thermocompression. Because indium belongs to the third group of the periodic table, it oxidizes very easily creating an insulating layer of In_2O_3 which is difficult to break. Luckily it is possible to permanently breaking this barrier with a rather low applied voltage (≈ 500 mV), restoring the connection resistance to values in the order of ~ 10 Ω .

The flip-chip operation can be performed at room temperature although the best results are obtained at around 100 °C. The bonding is formed by applying about 2000 N/cm², or slightly less than 1 g for a 20 μm diameter bump. In order to assure successful bonding on the entire sensor area, force must be applied uniformly on all the flip-chipped parts.

The main disadvantage of this technology comes from the fact that Indium has poor mechanical properties, making this kind of connection more fragile, requiring careful handling. Moreover, being a deposition process, it is wasteful, meaning that only a tiny fraction of the deposited indium is used to grow bumps, the rest is evaporated on the surrounding surfaces and is, therefore, wasted.

Both the described bump-bonding technologies were used in the assembly of the current ATLAS pixel detector [6]. An example of a grown solder bump is compared to a deposited indium bump in Fig.2.16. The proper bump technique for each application must be carefully decided and, at the same time, it is very important to be able to carefully control the quality of the process. The quality control is typically performed using television cameras and laser interferometry or by means of X-ray machines able to estimate

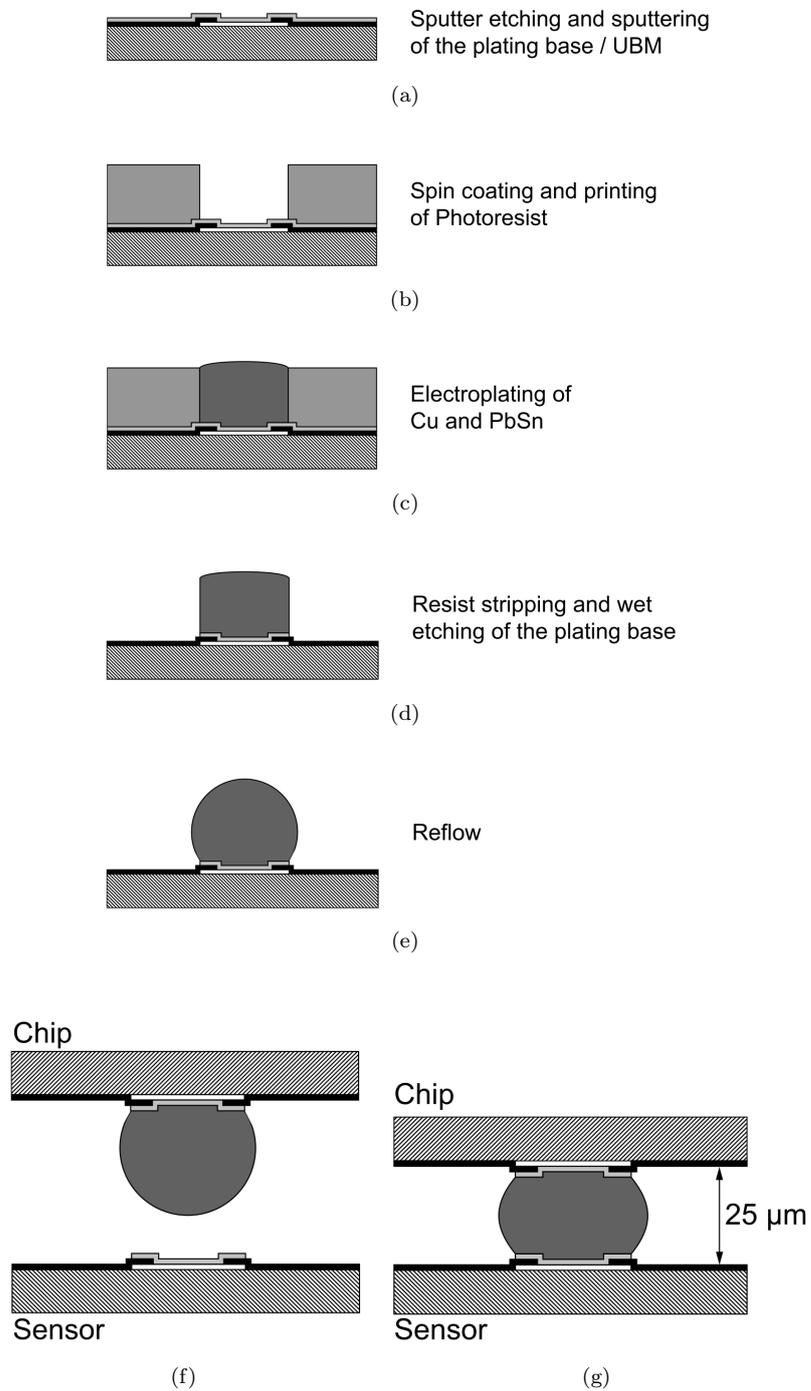


Figure 2.15: Sketches of the process flow in the PbSn (solder) bump deposition process (a)-(e) and flip-chip of the electronics die to the sensor (f)-(g) [30].

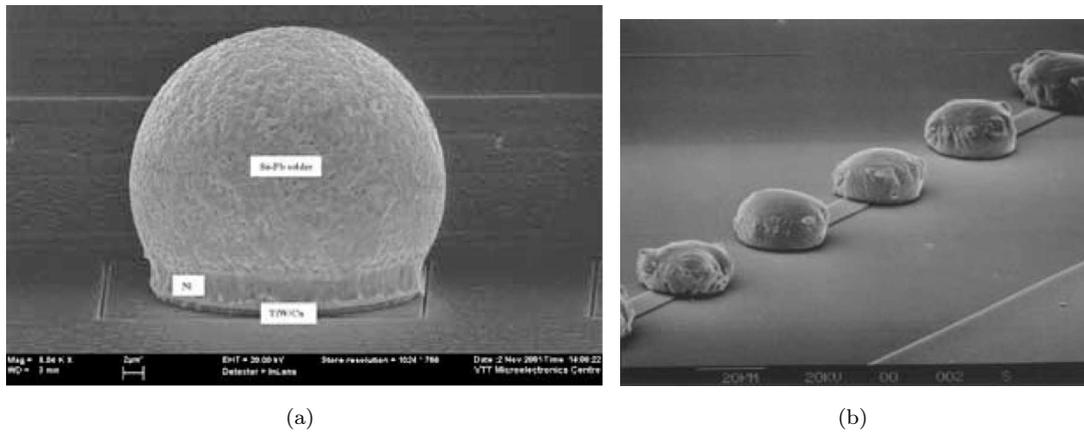


Figure 2.16: Comparison between a scanning electron microscope image of a deposited solder bump (a) with a micrograph of indium bumps deposited on silicon (b) [30].

misalignments or merged bumps. The yield for both technologies is well established with a defect rate of about 10^{-4} - 10^{-5} at wafer level and 10^{-3} - 10^{-4} after flip chip [45, 46].

2.5 Radiation damage in Silicon

When operating silicon devices in highly radioactive environments it is important to fully understand the consequences of radiation on the material. Several comprehensive studies have been performed on this topic in the past two decades leading to a fairly complete understanding of radiation damage in silicon devices. The analysis of all the radiation induced defects on semiconductor materials is very complicated and, in fact, several books have been written about it. For the purpose of this thesis only the most relevant effects will be here analyzed.

Radiation effects on silicon detectors can be divided in two well distinguished categories: (i) surface damage and (ii) bulk damage, the former causing modification to breakdown properties, inter-electrode isolation and surface recombination, the latter effecting full depletion voltages, leakage currents and charge trapping. The following analysis will show what are the consequence of these radiation induced modifications on silicon detector operation.

2.5.1 Surface damage

Most of the surface layers present in silicon devices are realized with the use of silicon dioxide (SiO_2). Silicon dioxide is so common because is readily available in any silicon related process with relatively simple high temperature steps in oxidizing atmosphere. The main known use of silicon dioxide is as gate insulator in MOS transistors up to a few

years ago when, due to the increasing scaling of transistor features, different materials with higher dielectric constants started to be used. Silicon dioxide is also present in silicon detectors as insulating layer on both wafer surfaces.

Silicon dioxide is known to contain defects even when well fabricated [37]. These defects are generated both inside the material and at the interface with silicon and can be divided in two different categories:

1. *Interface trapped charge*: positive or negative charges caused by structural defects, oxidation defects, metal impurities or radiation induced bond breaking. They are also caused by unterminated Si bonds. Interface traps, located at the Si-SiO₂ interface, can be charged or discharged depending on the applied surface potential and are often known as *interface states*. Their main effect on device property is a possible increase of the surface recombination (depending on their energy level) and, therefore, of the surface current.
2. *Oxide charge*:
 - *Fixed oxide charge*: positive charge near the Si-SiO₂ interface. It will attract negative charge on the opposite side of the interface, potentially affecting major electric quantities in the device, and can ultimately lead to a strong change in voltage handling capabilities.
 - *Oxide trapped charge*: positive or negative charge, typically results from ionizing radiation, avalanche injection or other mechanisms. Can be annealed at low temperature.
 - *Mobile oxide charge*: mainly caused by ionic impurities such as Na⁺, Li⁺ and possibly H⁺.

Radiation acts on these defect modifying their intrinsic properties [49]. When a particle crosses a SiO₂ layer with sufficient energy, it generates charge through ionization. Most e-h pairs will recombine instantly but a fraction of them will not. Because of the very different mobilities of electrons ($\mu_n \simeq 20 \text{ cm}^2/\text{Vs}$) and holes ($\mu_p \simeq 2 \times 10^{-5} \text{ cm}^2/\text{Vs}$) in silicon dioxide, electrons are able to escape quickly while holes diffuse to the Si-SiO₂ interface where they get trapped, resulting in an increase of the total oxide charge. An additional effect of radiation on SiO₂, is the increase in interface states concentration with a consequential increase in surface recombination velocity and current. The evolution of these defects with radiation fluence is understood and was measured [48]. Fig.2.17 shows how oxide charge concentration and surface recombination velocity vary with radiation fluence. Oxide charge concentration starts, even in very good oxides, from a few units of 10^{11} cm^{-2} (may be lower for <100> substrates). Radiation causes this value to increase of at least one order of magnitude ($1 \times 10^{12} \text{ cm}^{-2}$) as shown in Fig.2.17(a). At the same time, a standard value for surface recombination velocity (s_0) is in the order less than 10 cm/s

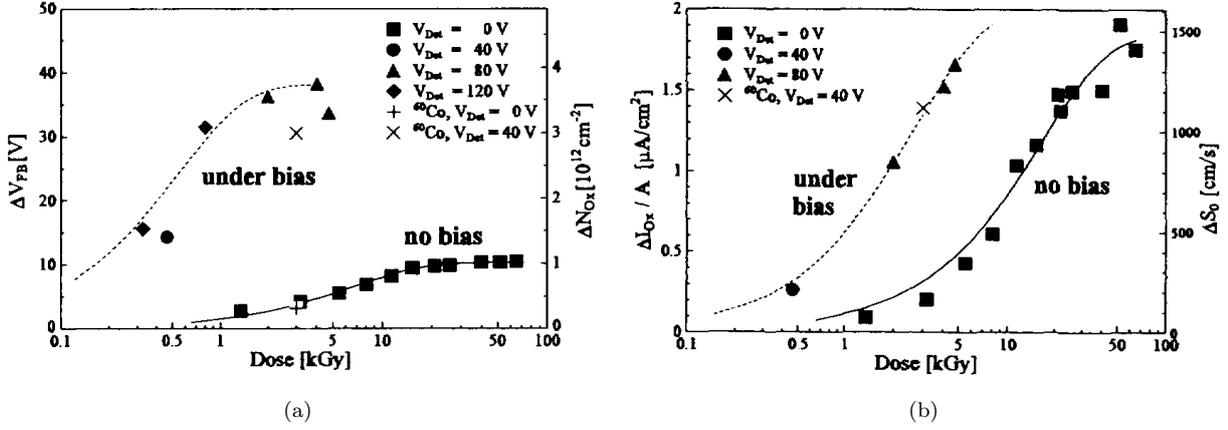


Figure 2.17: Evolution of radiation induced oxide charge (a) and surface recombination velocity (b) [48].

before irradiation while it increases of several orders of magnitude after (Fig.2.17(b)).

A very important aspect related to surface damage that is often underestimated, is its strong dependence on irradiation conditions: if irradiation is performed under bias, as it happens in the experiments where devices are operated, oxide charge concentration and surface recombination velocity start increasing considerably for lower radiation doses and, moreover, the final saturation value of the charge concentration is in the order almost $4 \times 10^{12} \text{ cm}^{-2}$ (see Fig.2.17).

The main consequences of the discussed radiation effects on device surfaces can be summarized as follows:

1. *Charge concentration*: the positive charge trapped in the oxide, will attract negative charge on the other side of the interface leading to:
 - compromised isolation between n^+ regions that is of great concern in n^+ readout detectors;
 - increase of the parasitic capacitance between adjacent regions that could degrade the noise performance of the device;
 - modification of the electric field distribution at the interface that can affect the voltage handling capabilities of the sensor.
2. *Interface states and surface recombination velocity*:
 - increase of the surface related leakage current.

Some of this effects can be mitigated with particular counteractions described in subsection 2.5.3.

2.5.2 Bulk damage

In silicon detectors used for tracking in highly radioactive environments, the damage to the bulk is caused by hadrons (neutrons, protons, pions and others) or highly energetic leptons (electrons, muons, neutrinos). The damage mechanism is characterized mainly by the loss of kinetic energy of the traversing particle inside the silicon lattice via multiple collisions with silicon atoms. If the energy of the considered particle is larger than the displacement threshold energy ($E_d \sim 25$ eV), this results in the displacement of the Primary Knock-on Atom (PKA) causing interstitials and vacancies in silicon, also known as Frenkel pairs [49]. Both interstitials and vacancies can migrate in the silicon lattice and finally form point defects with impurity atoms present in silicon.

If the particle energy is much higher than E_d defect clusters can be formed. The recoil atom from a highly energetic collision can potentially cause further damage to the silicon lattice. Its energy loss can occur through ionization (fully recoverable in silicon) or further displacement. At the end of a heavy recoil range, displacement prevails and defect clusters are formed as shown in the simulation reported in Fig.2.18.

Non Ionizing Energy Loss (NIEL) scaling hypothesis

It is well established that different particles interact with materials in different ways, for instance charged hadrons mainly interact through Coulomb interaction while neutrons

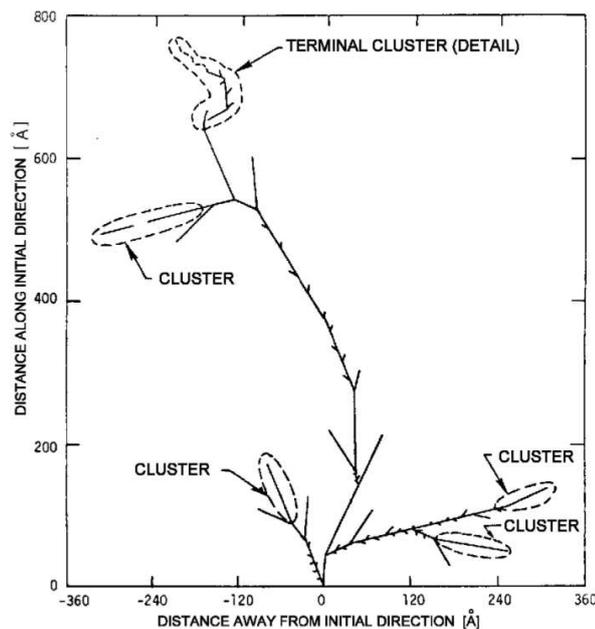


Figure 2.18: Monte-Carlo simulation of a recoil atom track with primary energy equal to 50 keV [49].

typically interact with the nuclei of the material. For this reason is very important to find a way to scale radiation damage from different particles with different energies with respect to the effects observable in silicon. This is done through the Non Ionizing Energy Loss (NIEL) hypothesis: any displacement damage induced change in the material, scales linearly with the amount of energy imparted in the displacing collisions. Using the displacement damage cross-section $D(E)$, it is possible to define a hardness factor "k" which allows to compare the damage efficiency of different radiation sources with different particles and individual energy spectra $\Phi(E)$:

$$k = \frac{1}{D(E_n = 1 \text{ MeV})} \cdot \frac{\int D(E)\Phi(E) dE}{\int \Phi(E) dE}. \quad (2.74)$$

In the previous equation E is the energy of the considered particle, $\Phi(E)$ is the energy spectrum of the radiation field and $D(E)$ is the displacement damage cross-section. Fig.2.19 shows an example $D(E)$ for different type of particles. The hardness factor is commonly used to compare the damage produced by a specific type of irradiation to the damage that would be caused by the same fluence of 1 MeV mono energetic neutrons. The 1MeV neutron equivalent fluence corresponding to a specific irradiation can be calculated as

$$\Phi_{eq} = k\Phi = k \int \Phi(E) dE. \quad (2.75)$$

The displacement induced defects in the silicon lattice, translate into the creation of energy levels in the forbidden band gap, behaving like acceptors or donors, that can

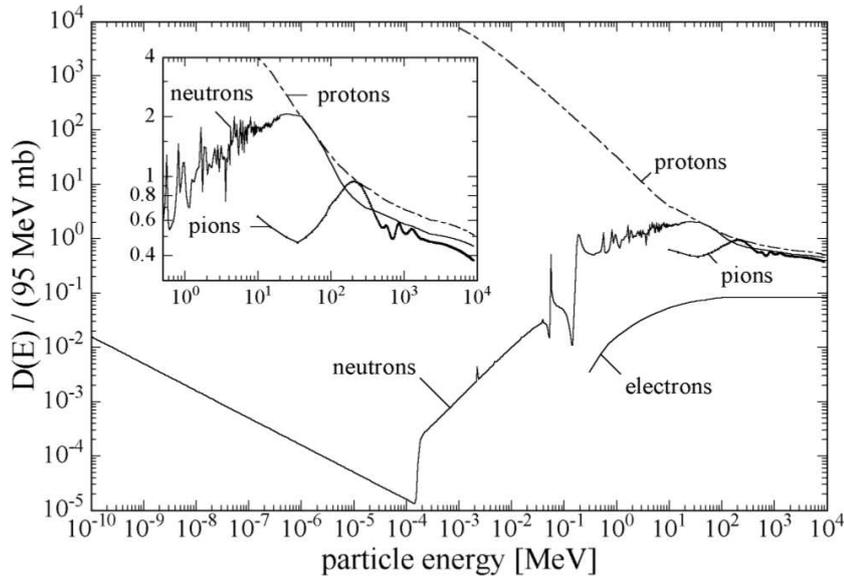


Figure 2.19: Displacement damage function $D(E)$ normalized to 95 MeV mb, for different type of particles [49].

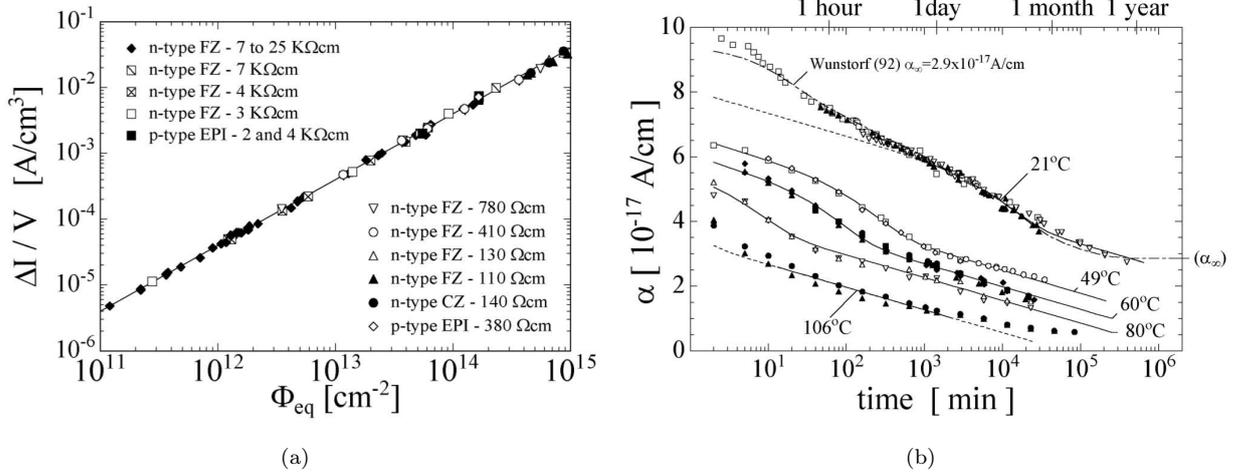


Figure 2.20: Fluence dependence of the leakage current for devices produced on different materials after a thermal treatment at 60 °C for 80 min (a) and dependence of the damage constant α on the annealing time (b) [49].

capture or emit electrons. In thermal equilibrium the charge state of the defect is strictly related to the Fermi level. An acceptor is negatively charged if occupied by an electron while a donor in the same condition is neutral. If the Fermi level is higher than the defect level the acceptor will have negative charge and the donor will be neutral, on the contrary, if the Fermi level is lower than the defect level, the acceptor will be neutral and the donor will be positively charged. As will be described shortly, the introduction of donors-like and acceptor-like defects will influence the effective doping concentration of the silicon bulk.

As already discussed in subsection 2.1.1, energy level in the forbidden band gap will enhance the generation recombination rate, causing the leakage current to increase. In particular, considering a defect energy level E_t , the total energy required to excite a captured electron to the conduction band will correspond to $\Delta E_t = E_C - E_t$.

The last effect of displacement defects on detector performance is a reduction of the charge collection efficiency caused by the increase of charge trapping in the material.

The consequences of the bulk damage on device properties are summarized in the following paragraphs.

Leakage current

The creation of spurious energy levels in the forbidden band gap enhances the generation-recombination process in silicon. In reverse biased pn-junction devices, this translates in an increase of the reverse leakage current, that will ultimately affect the noise and the power dissipation. The increase in current is normally proportional to the irradiation

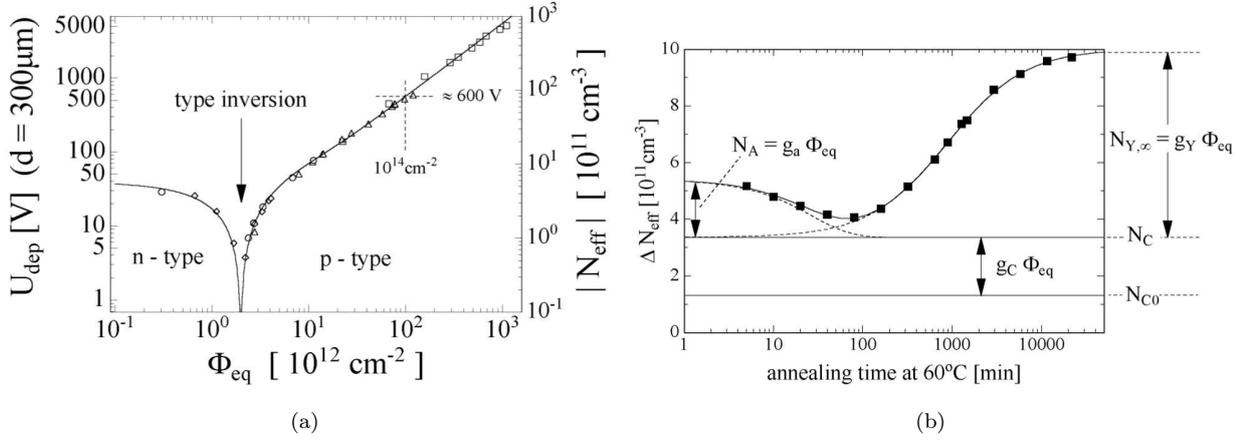


Figure 2.21: Variation of the effective doping concentration of an n-type silicon material as a function of the equivalent particle fluence (a) and its annealing behavior as a function of time at 60 °C after irradiation at a fluence of 1×10^{13} n_{eq}/cm² [49].

fluence and can be evaluated as

$$\Delta I = \alpha \cdot \Phi_{eq} \cdot V, \quad (2.76)$$

α being the current related damage constant, Φ_{eq} the 1MeV neutron equivalent fluence and V the total depleted sensor volume. The increase in current is also independent of material type as shown in Fig.2.20(a). As already stated in subsection 2.1.1, the leakage current is strongly temperature dependent so all the measurements must be scaled to the same reference temperature (e.g 20 °C).

The damage induced leakage current can be partially cured using annealing at high temperatures. This can be easily understood by looking at the behavior of α with time at different temperatures shown in Fig.2.20(b).

After the radiation fluences expected at LHC, silicon detectors mounted in the tracking stages must operate at low temperatures in order to reduce the effects of leakage current on readout noise.

Effective bulk doping concentration

The best operating condition for a silicon detector, is the condition in which the external bias voltage is such that the substrate is completely depleted from any free charge carriers. In a standard sensor, the full depletion voltage is strictly related to the substrate thickness and its doping concentration in agreement with Eq.2.37.

As previously stated, displacement defects can behave either like acceptors or donors depending on their nature. An example of the variation of effective doping concentration $|N_{eff}|$ for an n-type starting substrate is shown in Fig.2.21(a). The effective doping

concentration is initially reduced by an apparent donor removal and acceptor insertion at low fluences that finally lead to a sign inversion of the space charge region and a further increase of N_{eff} proportional to the radiation fluence.

Differently from what happens to the current related damage constant α , N_{eff} undergoes both a beneficial and a detrimental annealing also known as *reverse annealing*. Both these effects are shown in Fig.2.21(b). The variation of N_{eff} for an n-type substrate can be evaluated as

$$\Delta N_{eff}(\Phi_{eq}, t(T_A)) = N_{eff,0} - N_{eff}(\Phi_{eq}, t(T_A)), \quad (2.77a)$$

$$\Delta N_{eff}(\Phi_{eq}, t(T_A)) = N_A(\Phi_{eq}, t(T_A)) + N_C(\Phi_{eq}, t(T_A)) + N_Y(\Phi_{eq}, t(T_A)), \quad (2.77b)$$

where N_A is the short annealing term and can be represented by a sum of exponentials, N_Y is the reverse annealing term which start from zero and saturates at very high values for long times and, finally, N_C is the stable damage term which can be expressed as

$$N_{eff} = N_{C0} (1 - e^{-c\Phi_{eq}}) + g_c\Phi_{eq}, \quad (2.78)$$

where N_{C0} is the final value of the incomplete donor removal and the product $g_c\Phi_{eq}$ is the fluence proportional insertion of acceptors.

The increase of the effective doping concentration in p-type materials was found to be a one way process, meaning that no type inversion was observed [50]. The stable damage term can be written considering only the acceptor insertion part without considering the initial donor removal. As already mentioned in subsection 1.3.2, this turns out to be an important advantage of p-type over n-type materials, because the junction electrodes will remain on the same side of the device also after heavy irradiation, making n-in-p sensors strong candidates for the upgrades of future silicon trackers.

Degradation of charge collection efficiency due to charge trapping

The increase in defects in the silicon bulk has another direct consequence. As already mentioned, these defects can act as trapping centers for free carriers. Free carriers generated from an impinging particle can be captured by one of these defect centers and will not be contributing to the total charge collected from the sensor, thus degrading the total charge collection efficiency (CCE). Effects related to trapping are well studied and well documented in literature [51, 52].

The total trapping probability is directly proportional to irradiation fluence:

$$\frac{1}{\tau_{eff,(n,p)}} = \beta_{n,p}(t, T)\Phi_{eq}, \quad (2.79)$$

where $\tau_{eff,(n,p)}$ is the effective trapping time and $\beta_{e,h}(t, T)$ is the so called *trapping constant* which is time and temperature dependent and also influenced by the type of particles used

for irradiation. The trapping time can be seen as similar to the bulk lifetimes of a silicon detector, so the total length that free carriers can drift before being trapped is equal to

$$L_{drift} = \tau_{eff} v_{drift}, \quad (2.80)$$

meaning that shorter trapping times will result in a larger amount of carriers being trapped. Finally, the total amount of drifting charge that induces current on the readout electrodes can be expressed as

$$N_{e,h} = N(0) \exp\left(-\frac{t}{\tau_{eff,(n,p)}}\right). \quad (2.81)$$

The analysis of trapping times returns additional advantages for devices fabricated on p-type silicon: (i) the trapping constant β was found to be lower for electrons than for holes and (ii) the annealing of trapping times turn out to be beneficial for electrons and detrimental for holes [52].

2.5.3 Counteracting radiation damage

In order to prevent some of the outcomes of radiation damage in silicon, several techniques can be implemented. This subsection will briefly describe the most important among them.

Prevention of surface damage consequences

The increase of positive oxide charge up to very large values can cause several different issues and among them the most relevant are: (i) in case of p-in-n devices, a strong modification of electric field distribution at the devices surface occurs, possibly leading to anticipated breakdown and (ii) in case of n-in-p and n-in-n devices, the creation of a surface electrons layer that will eventually short all the segmented n^+ readout electrodes, causing the impossibility of position sensing. The former effect is usually less critical while the latter can render the device useless so it must be prevented.

Three well know solutions are available to prevent the inversion of surface layer and avoid the shorting of n side readout. They are often called *surface isolation techniques*: (i) p-spray, (ii) p-stop and (iii) moderated p-spray [53].

Thanks to numerical simulations the behavior of these techniques is very well understood [54]. The perfect choice of isolation technique is not possible, but by properly weighing the different options, it is possible to find the best one for a specific application. The main parameters that must be taken into account, are mainly: (i) the required breakdown voltage both pre and after irradiation, in order be able to operate the device at optimal bias, (ii) the inter-electrode capacitance, and of course (iii) the isolation properties

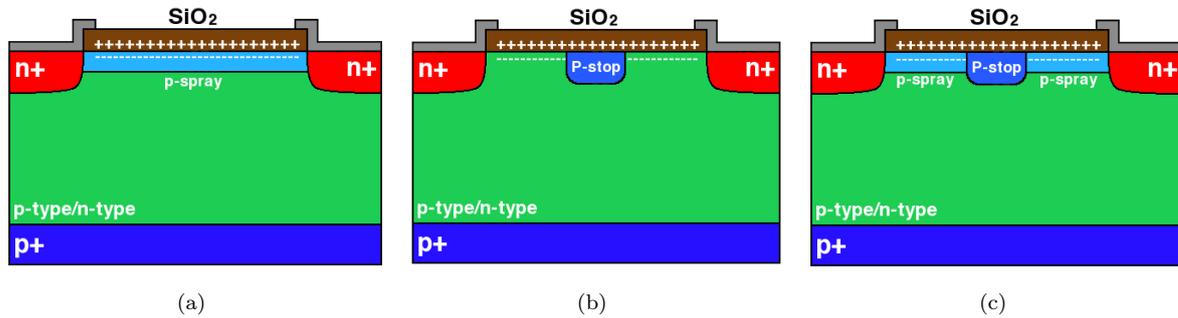


Figure 2.22: Different surface isolation techniques: p-spray (a), p-stop (b) and moderated p-spray (c).

(inter-electrode resistance). A brief description of each technique is here given highlighting the advantages and disadvantages of each one of them:

1. p-spray: it consists in a medium dose p^+ implantation on the readout side of the wafer (Fig.2.22(a)). This solution has the main advantage of being very simple. The end result is the compensation of the surface electron layer that is formed as a consequence of the positive charge trapped in the oxide. The main disadvantages of this technique are related to a rather low breakdown voltage before irradiation, caused by the increased doping concentration of the p^+ region in contact with the n^+ electrodes, by the fact that the p-spray potential will tend to follow the substrate potential, and by a larger inter-electrode capacitance (notice that the reduced breakdown voltage pre-irradiation is not a big issue because devices can be operated at rather low biases). When the devices undergo irradiation, the total oxide charge concentration increases and the effective doping of the p-spray layer is reduced. This leads to larger breakdown voltages and lower inter-electrode capacitances after irradiation. Unfortunately, if the implanted dose is not sufficient or if the forecasted irradiation levels are overcome, the inter-electrode isolation cannot be assured.
2. p-stop: this solution is intended to interrupt the continuity of the surface electron layer with localized high dose p^+ implants all around the read out electrodes. This approach is shown in Fig.2.22(b). The best geometrical implementation of p-stop is to have narrow implants, in order to limit its coupling with substrate bias and thus increasing the breakdown voltage. In this particular case the surface electron layer is in direct contact, on one end, with the n^+ junctions and will therefore be grounded. On the other end, the electron layer is in direct contact with a high concentration p^+ implant. The breakdown voltage of p-stop is typically high before irradiation but, as the oxide charge increases, it starts decreasing. As far as the inter-electrode capacitance is concerned, it increases with the charge oxide concentration. The main advantage of p-stop over p-spray is the certain isolation between electrodes.

3. moderated p-spray: in Fig.2.22(c) the moderated p-spray option is shown. This technique consists in combining both a medium/low dose uniform implant and a high dose localized implant in order to fuse the property of p-spray with those of p-stop. As far as breakdown voltage is concerned, it starts low and it increases with irradiation dose (typical of p-spray). If the p-spray layer is realized with a low dose implant, in order to maximize breakdown before irradiation, it might happen that the increase of oxide charge will result in its complete compensation. At this point the structure behavior resembles the one of p-stop, with breakdown voltage decreasing as the total radiation dose increases. Comparably, the inter-electrode capacitance will initially decrease (p-spray) and then increase (p-stop).

Prevention of bulk damage consequences

The prevention of bulk damage operates on two different levels: (i) material engineering and (ii) device engineering.

Material engineering mainly consist in the search for new types of semiconductors that will better withstand high radiation doses. A very strong technique to create more robust silicon substrate is to use oxygenated substrates. Oxygen is believed to capture vacancies in stable and neutral point defects, leading to a diminished effective doping modification after irradiation [55, 56]. This is limited only to the stable damage and reverse annealing and is restricted to charged hadrons irradiation. Another option is to use different kinds of semiconductors. In this sense, diamond is attracting a growing amount of attention due to its very low leakage current and high radiation hardness coming from a larger band gap. The main disadvantage of this, is the extremely high cost of diamond substrates and the difficulty of producing them in large sizes.

As far as device engineering is concern, it might be applied on current devices in order to enhance their performances, or can result in the production of new architectural implementations. The first structural modification that can make current devices more radiation hard, is the use of n-in-p structures in order to gain from the enhanced electron collection (higher mobility) and to benefit from the fact that p-type material typically does not encounter type inversion.

As previously described, from the point of view of leakage current not much can be done apart from cooling. The other option, the creation of new sensor technologies, has been taken into account in the past decade, thanks to birth and evolution of 3D silicon detectors, which are the real news in silicon detector technology since many years, together with Monolithic Active PixelS (MAPS). 3D silicon detectors are the object of this thesis and will be largely reviewed in the next chapters.

Chapter 3

3D detectors state of the art before IBL

Silicon radiation detectors became of common use in the 1980s, after Kemmer pioneered the use of planar microelectronics processes [57] to produce devices which could detect radiation. The advantage of use such well standardized processes is the ease of fabrication, leading to devices featuring fine pitch segmentation of electrodes and very low leakage currents in relatively short times, allowing for medium/high volume production.

In the past three decades the field of silicon radiation detectors has grown at an incredible pace, several different architectural implementations are nowadays available, ranging from standard planar devices to Monolithic Active Pixels (MAPS) that make use of the latest CMOS processes developed for microprocessor fabrication [58]. Nowadays silicon detectors are able to provide excellent timing and position resolutions, long term stability and good radiation tolerance and, for this reason, they have been used as tracking devices in high energy physics experiments, as already discussed in Chapter 1.

When operated in extremely harsh environment, like highly radioactive locations inside the experiments, silicon detectors suffer from radiation damage that causes their performances to be compromised as discussed in Chapter 2. In order to properly understand how the operating conditions of the devices are affected by the constantly increasing radiation dose, it is crucial to regularly monitor the main electrical properties of tracking detectors. As an example, in the ATLAS experiment, leakage currents and full depletion voltages of the detectors in the tracker are frequently monitored. Leakage currents can be measured both per pixel, by means of on-chip functionalities, or per module (16 sensor/chip assemblies) through Current Monitoring Boards [59]. The measurement is normally performed on all modules of a half stave with a precision of ~ 80 nA. At the same time, the full depletion voltage of the sensors is also monitored through a cross-talk calibration scan which consist in reading out, from a single pixel, the charge injected in the two neighboring ones along the long side, while changing the bias voltage. When full depletion is reached, a saturation to a maximum collected charge is reached.

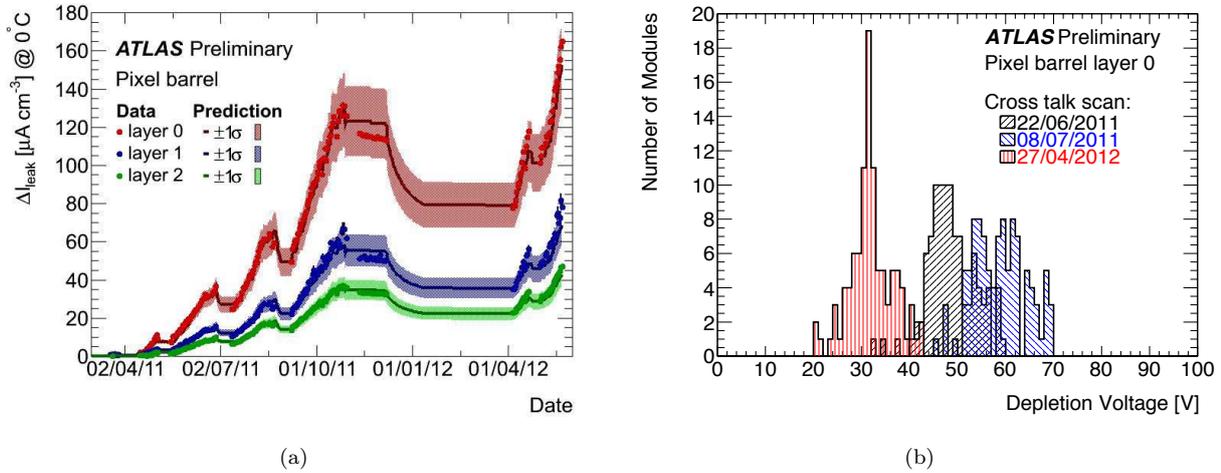


Figure 3.1: Increase in leakage current (a) and change in depletion voltage (b) in the ATLAS tracker as a function of the operation date [60].

Current available results for the ATLAS tracker are reported in Fig.3.1. Fig.3.1(a) shows the evolution of the leakage current as a function of the date. As of April 2012 a sensible linear increase due to radiation damage is observable and the LHC shutdown periods are evident by looking at the lowering of the currents due to beneficial annealing. For what depletion voltages are concerned, ATLAS silicon detectors are realized on n-type substrates and, as previously mentioned, radiation damage in this material causes an initial lowering of the bulk effective doping concentration thus resulting in lower full depletion voltages. Fig.3.1(b) shows exactly the described behavior, that is a lowering from about 60V to about 30V of the full depletion voltage in a little less than a year. The monotonic change in operating voltage indicates that type inversion was not reached yet, allowing to assume a correct sensor operation up to at least the full design luminosity of the LHC.

As the luminosity of the LHC will increase in the coming years, detector performances will keep on degrading due to radiation damage. Current pixel devices, installed in the innermost layer, are designed to withstand a fluence of $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ before being rendered inoperative. Many R&D activities are currently active to design and produce radiation-hard tracking devices for the foreseen upgrades of the LHC, also known as super-LHC (sLHC), that will greatly increase the machine luminosity. The expected fluence for the innermost layers after 5 years of operation at sLHC is reported in Fig.3.2(a) as a function of the radius from the interaction point. Since the highest expected fluence is above $1 \times 10^{16} \text{ n}_{eq}/\text{cm}^2$, experiments will require sensors that exhibit much higher radiation tolerance than the current ones. Moreover, at such radiation fluences, the charge trapping resulting from radiation damage in the bulk will reach values never seen before, drastically reducing the total collected charge and degrading the signal to noise ratio.

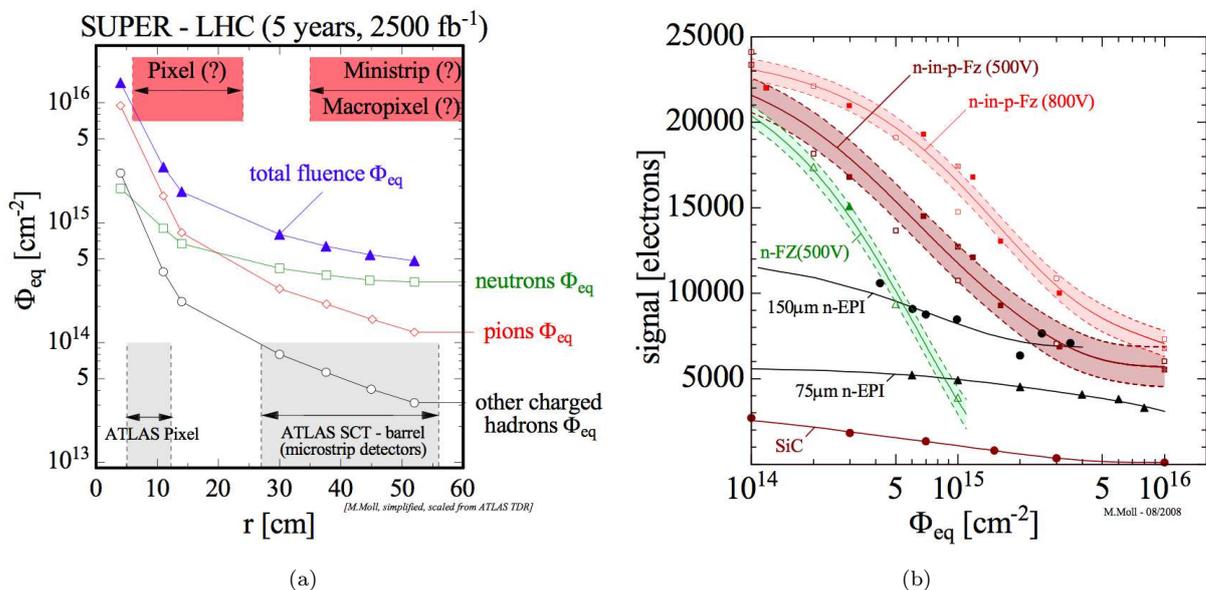


Figure 3.2: Expected radiation fluence in sLHC as function of the distance from the interaction point (a) and reduction in charge collection efficiency measured on irradiated sensors in different R&D activities [61].

The expected evolution of charge collection at sLHC fluences is reported in Fig.3.2(b) for different materials. As expected, p-type substrates should slightly increase device collection efficiency. Together with a drastic signal reduction, the increase in leakage current will increase noise and thermal dissipation, making the operation of the sensors very difficult.

As already mentioned at the end of Chapter 2, the increase in radiation tolerance of tracking detectors can be achieved in two ways: (i) material engineering and (ii) device engineering. From the point of view of material engineering it was already shown that the use of non-oxygenated p-type substrates should return several advantages. Other approaches would be to use different semiconductor materials like diamond which, despite its incredible ease of use, is still too expensive even for a low volume production. From the point of view of device engineering, n-in-p planar technologies are being evaluated in pre and after irradiation conditions [62].

Although it appears possible to realize planar devices able to withstand sLHC fluences, current levels and operation voltages after heavy irradiation are a big concern, especially in terms of power dissipation, that might lead to thermal runaway. For this reason a rather recent radiation-hard sensor architecture is being considered as strong alternative: the *3D architecture*.

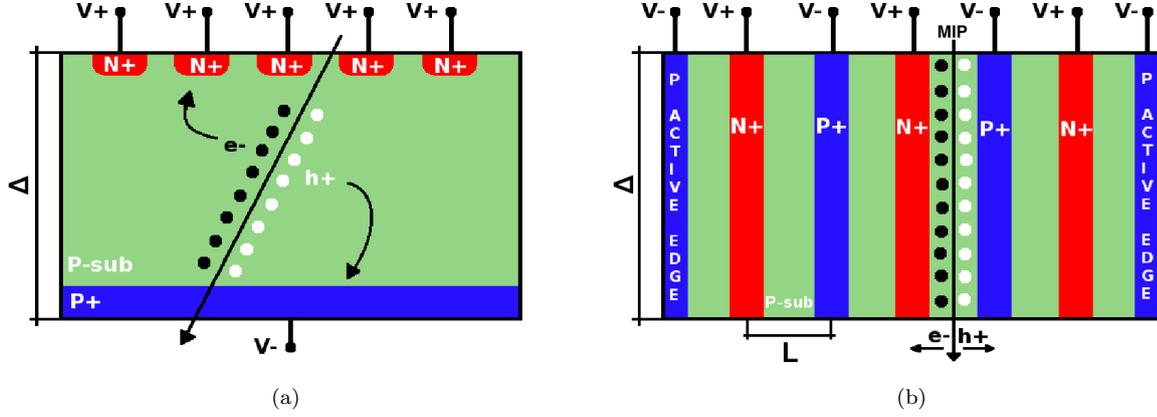


Figure 3.3: Comparison between planar (a) and 3D (b) sensor architectures.

3.1 The 3D silicon sensor architecture

The 3D architecture was first proposed by Parker and collaborators in 1997 [63]. Differently from the standard planar architecture, where sensor electrodes are realized on both wafer sides by means of ion-implantations, 3D architecture exploits modern micro-machining processes used in the production of Micro-Electro-Mechanical-Systems (MEMS) (e.g. the Deep Reactive Ion Etching, DRIE), to realize vertical columnar electrodes penetrating all the way through the silicon substrate, allowing to decouple the active volume thickness (imposed by the wafer thickness) from the inter-electrode distance.

A sketch of both technologies is reported in Fig.3.3. A minimum ionizing particle crossing devices with the same substrate thickness Δ will generate the same amount of charge. Differently from what happens in planar devices (Fig.3.3(a)), where the inter-electrode distance is equal to the wafer thickness ($L=\Delta$), in 3D detectors (Fig.3.3(b)), this distance can be chosen during the design phase and it is possible to reduce it to very low values (less than $50\mu\text{m}$). This peculiar architectural implementation, returns very low full depletion voltages thus allowing to obtain very high electric fields and carrier velocity saturation easily. Moreover, the average carrier drift length is much shorter than in planar devices, delivering faster signal and reduced trapping probability after irradiation.

In order to estimate and compare the effects of trapping on both planar and 3D detectors, it is possible to define the Signal Efficiency (SE) as the ratio between the maximum induced signal without trapping, to the maximum induced signal in presence of trapping. By applying Ramo's theorem [33], reference [64] shows that the signal efficiency in a silicon detector can be calculated as

$$\text{SE} = \frac{1}{1 + K_C \Phi}, \quad (3.1)$$

where

$$K_C = \frac{0.6L\beta_{n,p}}{v_D},$$

is the damage constant for the Signal Efficiency, which depends on the trapping time damage constant $\beta_{n,p}$ (see Chapter 2 subsection 2.5.2), the inter-electrode distance L and the drift velocity v_D . Assuming an operation condition in which a planar device and a 3D device, irradiated at the same fluence Φ , are operated in full depletion at voltage sufficient to fully saturate the carrier velocity v_D , it is easy to understand that, reducing the inter-electrode distance L , will translate in higher signal efficiency. For instance, considering a substrate thickness $\Delta=300 \mu\text{m}$, the inter-electrode distance for planar will be $L_{\text{planar}}=\Delta=300 \mu\text{m}$, while for 3D is a parameter than can be chosen to better fit the experimental needs. Let's suppose to fix $L_{3D}=50 \mu\text{m}$ for the sake of simplicity. Since the only variable in Eq.3.1 is the inter-electrode distance, and $L_{\text{planar}}/L_{3D}=6$, it is reasonable to expect a signal efficiency six times larger for 3D detectors. Additionally, the intrinsic self shielding between elementary 3D cells, provides reduced charge sharing between pixels with respect to planar devices, as will be shown in the following sections.

The superior operation of 3D detectors, comes to the price of a rather complicated fabrication process that will be detailed in subsection 3.2.2. Some functional disadvantages affect 3D sensors as well:

- because of their peculiar structure, 3D sensors have a non-uniform signal response due to the presence of low/null field regions between electrodes of the same doping type, and within the electrodes themselves. Charge generated in these regions will initially move by diffusion (slowly), thus increasing the trapping probability after irradiation;
- the capacitance of 3D sensors is larger than the one of a standard planar device, because of the shorter inter-electrode distance and the extension of the electrodes all the way through the silicon bulk.

An additional feature that is a direct evolution of 3D technology is the so called *active-edge*. In standard silicon detector processes, devices are separated from the wafer by means of a diamond saw. The cut procedure induces cracks and chipped regions acting as generation-recombination centers at the edge of the device (Fig.3.4). If the depletion region reaches these defects a large amount of current will be injected in the device, eventually leading to a premature discharge. For this reason, the edge region (indicated with "a" in Fig.3.4), usually has a large extension ($a=0.5\text{-}1 \text{ mm}$) in order to also insert current terminating structures and floating rings allowing to gradually drop the electrostatic potential toward the edge. By means of 3D technology, with the same technique used to fabricate columnar electrodes, it is possible to etch a deep trench all around the active area of the device which is later doped (and so passivated) and will act

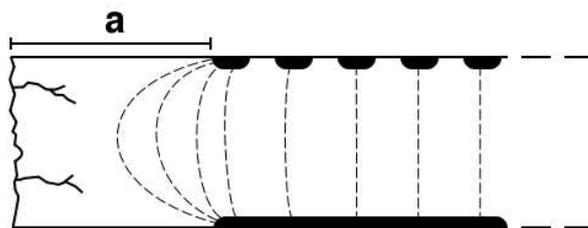


Figure 3.4: Cross-section sketch of a saw cut standard device, showing the depleted region extending toward the cut region. The distance "a" indicates the space needed to insert guard-rings and to safely operate the device at high voltage.

as an ohmic contact, thus removing the need for diamond saw cutting. The active-edge is feasible both on 3D and planar devices (see Chapter 6). As described later, this technique requires a support wafer, adding further complications to the fabrication process.

The study of 3D devices has greatly increased in the past few years and several papers are currently available in literature (cited in the text) together with some books. In particular a good summary of results on 3D detectors is reported in Chapter 2 of reference [65]. This chapter will review the state of the art in 3D detectors up to about two years ago. More recent developments will be discussed in the following chapter.

3.2 Full 3D detectors

Silicon 3D detectors with columnar electrodes passing through the entire bulk and active-edge will, from now, be referred to as *Full 3D detectors*. The first prototypes of full 3D detectors were designed and fabricated at Stanford University, USA. Verification of the correct operation and layout design were performed with Technology Computer-Aided (TCAD) tools and the fabrication was performed at Stanford Nano Fabrication (SNF) Facility. The following subsections will describe the different steps from simulation and design to fabrication and testing.

3.2.1 Numerical device simulations

Numerical device simulation is nowadays becoming crucial to verify device operation before fabrication, and is important when designing sensor prototypes with a new architectural implementation. Electrical and functional simulations were reported in [63] and a subset of those results is here shown and discussed.

An elementary simulation cell for 3D detectors is reported in Fig.3.5(a). The inter-electrode pitch is equal to $25 \mu\text{m}$ and the substrate is $300 \mu\text{m}$ and n-type. Different bulk doping concentrations can be chosen. In order to investigate device properties relative

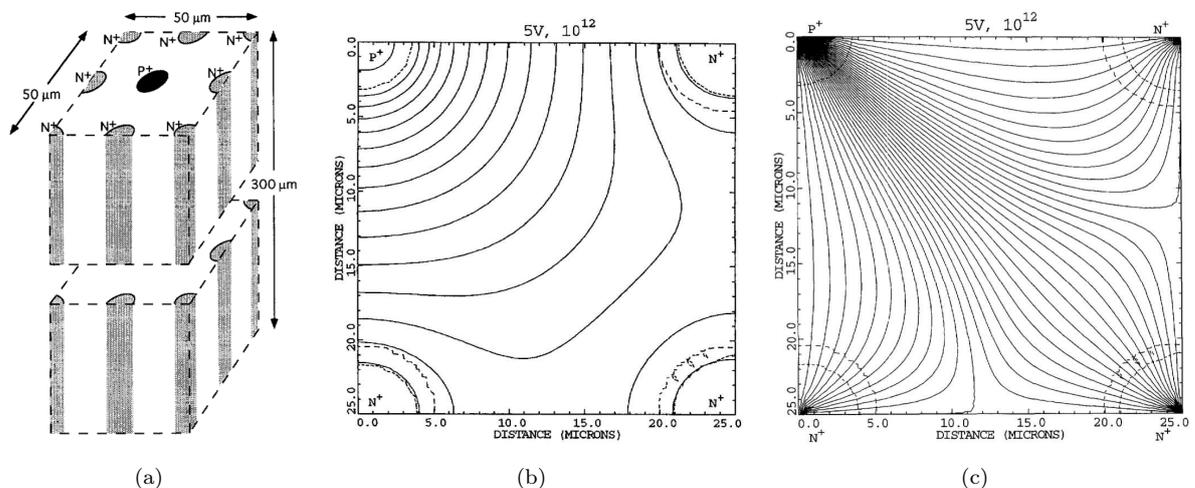


Figure 3.5: Simulation results of full 3D detectors. Elementary cell of a 3D detector (a), simulated equipotential lines for a quarter of elementary cell with bulk doping equal to 10^{12} cm^{-3} and bias voltage equal to 5V (b) and drift lines in the same conditions (c) [63].

to the bulk, where electrical quantities are not affected by surface effects, it is possible to perform a 2D simulation on a slice of the full structure taken from the middle of the substrate along a plane parallel to the wafer surfaces. This will greatly reduce the number of nodes and, as a consequence, the required computational time. To further reduce the complexity of the simulation, device symmetry can be exploited by only simulating a quarter of the elementary cell. Simulations of electrical quantities are typically performed by grounding one type of electrode and by applying a reverse bias ramp to the other electrode type. Considering an n-type silicon bulk with doping concentrations of $N_D=10^{12}$ and $N_D=10^{13} \text{ cm}^{-3}$, full depletion voltages can be estimated to be equal to 1.6 and 8.8 V respectively. Equipotential lines for the first case ($N_D=10^{12} \text{ cm}^{-2}$ and $V_{bias}=5 \text{ V}$) are reported in Fig.3.5(b) while the drift lines for the same operating conditions are shown in Fig.3.5(c). Despite full depletion in this conditions is already reached, low field regions are present between electrodes of the same doping type. This is explained in detail in Fig.3.6. The electric field distribution for the examined 2D structure can be extracted along the desired direction for different applied reverse voltages. Between a p^+ and an n^+ column, the field shows a large peak at the junction column (p^+) and a decrease followed by a smaller peak close to the other column (Fig.3.6(a)). The maximum field value is equal to roughly $6 \times 10^4 \text{ V/cm}$, still considerably lower than the critical value ($\sim 4 \times 10^5 \text{ V/cm}$), but allows for fast carrier drift times. On the other hand, along the line connecting two n^+ columns, the field has a lower magnitude and an almost zero field region is present (Fig.3.6(b)). These differences in field distribution cause the amplitude and timing evolution of the signal to be dependent on the particle hit position. This

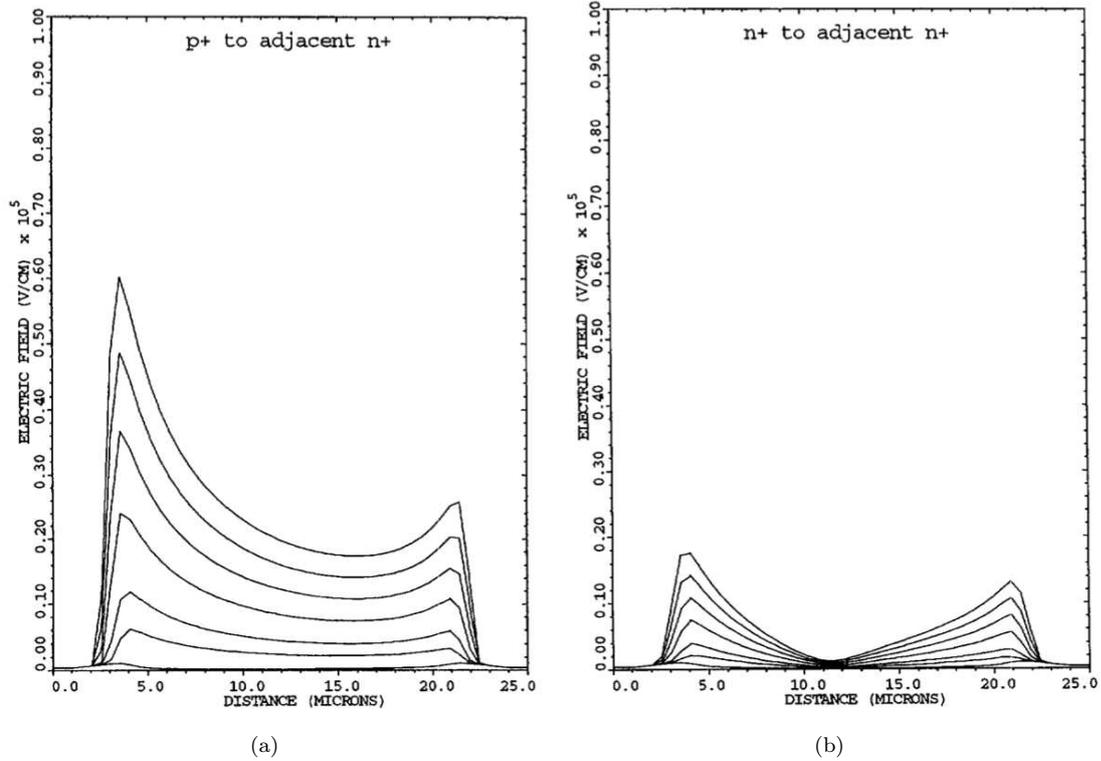


Figure 3.6: Electric field distributions for different applied biases, extracted along the drift lines connecting a p⁺ electrode to an n⁺ electrode (a) and along drift lines connecting an n⁺ to another n⁺ electrode (b). The bulk doping concentration is equal to 10¹² cm⁻³ reverse biases are equal to 0, 5, 10, 20, 30, 40 and 50 V. [63].

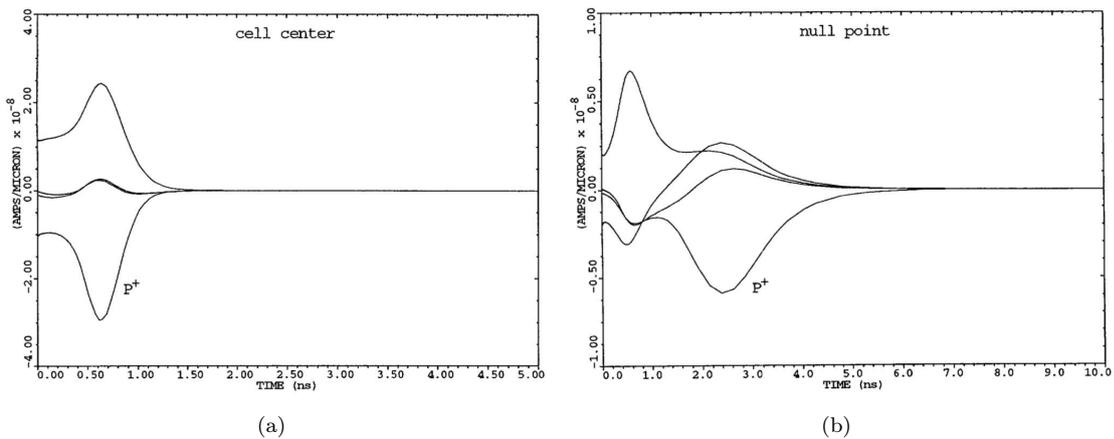


Figure 3.7: Readout electrode current in response to a MIP particle crossing the device in the center of a quarter of an elementary cell (a) and in the zero field point of the same structure ($N_D=10^{12}$ cm⁻³) [63].

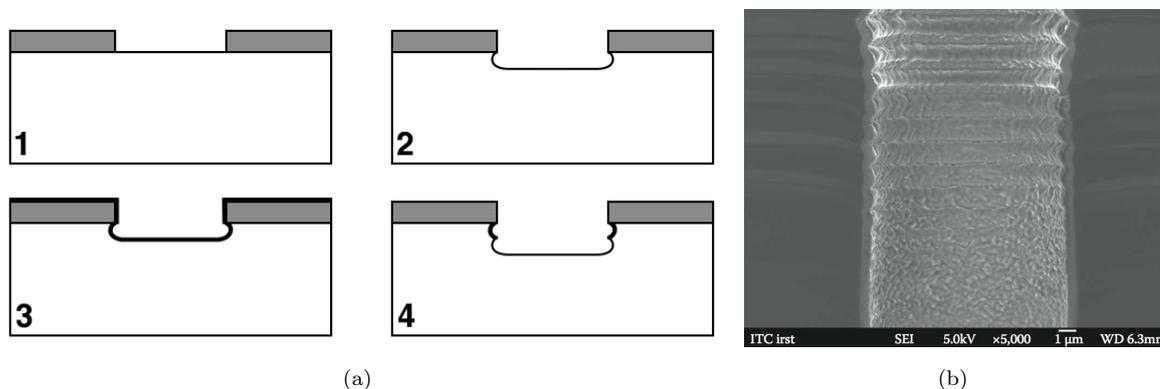


Figure 3.8: Deep Reactive Ion Etching process sketch (a) showing most relevant steps: structure definition (a.1), first etch step (a.2), hole passivation (a.3) and following etch step (a.4). Example of DRIE hole also showing the resulting scalloping effect (b) [65].

is highlighted in Fig.3.7. When the particle impinges the center of the cell (Fig.3.7(a)), electrons and holes are collected in about 1 ns, whereas when the hit position is inside the zero field point, the total collection time is longer, up to 5 ns (Fig.3.7(b)). It is important to point out that, even in the worst case, the total collection time in 3D detectors, is still shorter than in standard planar devices.

3.2.2 Fabrication technology

The fabrication of 3D silicon detectors strongly relies on non-standard steps inherited from MEMS technologies that were developed in the '90s. In particular, the Deep Reactive Ion Etching (DRIE), allows to etch very anisotropic structures in silicon, enabling the realization of columnar electrodes with high aspect ratios (higher than 30:1) with relatively high etch rates of about $3 \mu\text{m}/\text{min}$ and very low nonuniformities across the wafer [66].

The standard DRIE makes use of the so called *Bosch process* [67] which employs a continuous repetition of a two-phase etching cycle based on fluorine compounds, alternating nearly isotropic plasma etching steps (using SF_6) and sidewall passivation (using C_4F_8) to achieve high anisotropy along the entire etching profile (see Fig.3.8). The fabrication of 3D detectors was addressed in [63] but more details were given in [68].

Only the most important steps will here be reported and each described step is shown in Fig.3.9:

- a. *Oxidation and wafer bonding*: the passivation is typically the first step in any detector technology, in order to protect the surface of the wafer. Wafer bonding instead, is typically used in MEMS processes and is used in 3D technology because it provides mechanical support during fabrication, providing enhanced sensor wafer strength avoid-

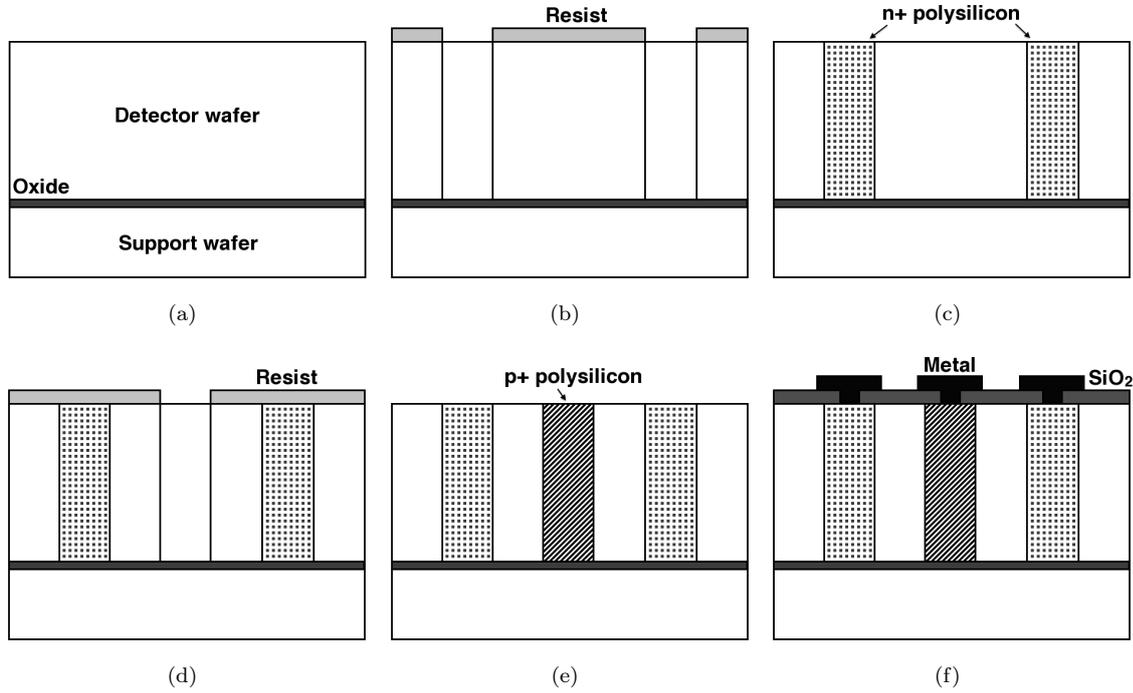


Figure 3.9: Schematic representation of the most relevant fabrication steps for full 3D detectors, the description is given in the text.

ing possible damages during the process, it is necessary in case of the realization of the active-edge (as will be described later) and allows the detector wafer to be back-thinned relatively easily.

- b. *p⁺ hole definition and etching*: the p⁺ holes geometries are defined by lithography and oxide etching. The columnar electrodes are etched all the way through the silicon wafer using DRIE, with the thick oxide and photoresist layers on the top wafer side acting as protection mask.
- c. *p⁺ hole filling and doping*: holes are completely filled with polysilicon by means of deposition inside an LPCVD reactor with conformal coating provided by properly setting the temperature and pressure conditions. The doping is performed by thermal diffusion from a solid source and can be performed in two different ways, after the complete filling of the holes or after a first pre-filling followed by a second deposition. The polysilicon filling is not strictly necessary but it provides several advantages: from the fabrication point of view, it helps in recovering the planarity of the wafer surface thus easing the following photoresist spinning, avoiding its trapping inside the holes; moreover, from the functional point of view, particles crossing a polysilicon filled electrode can generate charge inside it and, provided that lifetimes in polysilicon are large enough, part of the generated charge can be collected by diffusion. The main disadvantage of polysilicon

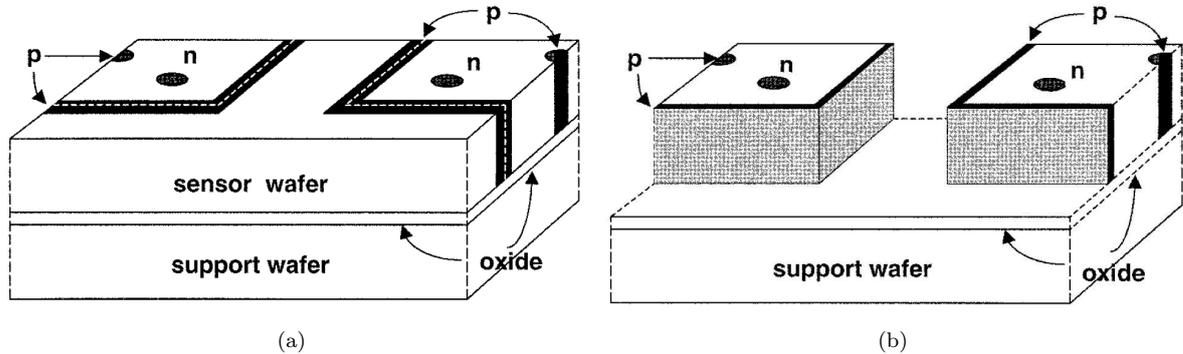


Figure 3.10: Active edge sensor fabrication. P^+ doped trenches and holes must be etched at the same time (a). After device fabrication the surplus material has to be etched away (b) [71].

filling, is that the wafer surface will also be covered by a rather thick polysilicon layer which must be removed, further increasing fabrication complexity.

- d. *n^+ hole definition and etching*: similar to step (b), lithography is used to define n^+ holes geometries and DRIE to etch them.
- e. *n^+ hole filling and doping*: similar to step (c), n^+ holes are filled with polysilicon and doped with thermal diffusion from a phosphorus source.
- f. *Metal deposition and definition*: the final oxide layer is deposited and contact holes are opened. Metal is deposited and patterned. A final passivation can be deposited and etched only on probe pads and bump pads.

The process is concluded with the removal of the support wafer. In addition, in case the signal is readout from n^+ electrodes, surface passivation layers are required forcing to add additional lithographic and implantation steps for the realization of p-spray or p-stop on both wafer sides. In case the active-edge is realized the support wafer is needed to keep pieces in place during fabrication; moreover, two other things have to be carefully taken care of:

- the etching step used to realize one hole type, must be used to etch the edge trenches as well, and it must, therefore, be completely compatible. The etching rate for different geometries is rather different, long trenches are etched faster than small holes, for this reason the trench width must be kept smaller than the electrode radius. The trench filling and doping must be performed at the same time of the columnar electrodes as well as shown in Fig.3.10(a).
- An additional etch step must be planned at the end of the process to remove all the material surrounding the active area of the devices, leaving only polysilicon as passivation layer as shown in Fig.3.10(b).

3.2.3 Experimental results

Several detector geometries can be implemented with 3D technology by properly arranging columnar electrodes in different configurations and by connecting them with metal lines. The possibility of choosing the inter-electrode distance during the design phase, allows to find the correct compromise between noise and collection efficiency specific to every application. Diode, strip and pixel detectors were fabricated in different configurations and tested in several laboratories around the world.

Electrical and functional characterization of the first prototypes was reported in reference [68]. Devices were fabricated on 121 μm thick, p-type wafers and showed leakage currents in the order of 1 nA/cm² and breakdown voltages larger than 60V. Although reverse discharge seems to appear very early, it must be remembered that full depletion in 3D detectors is reached for less than 10 V of applied bias, 5 and 8 V for 100 and 200 μm inter-electrode spacing respectively. Measurements with a pulsed Infra-Red laser confirm charge collection saturation, and therefore full depletion, before 10 V (Fig.3.11).

The first charge collection measurements performed with X-Ray beams and radioactive sources are reported in [69] resulting in a full width half maximum resolution on the manganese K line of a ⁵⁵Fe source equal to 652 eV. This value is slightly larger than what obtained with standard devices but it was expected and is fully explained by the values of reverse current and capacitance, that will ultimately affect the noise of the system. X-Ray beam measurements confirmed the expected low charge sharing.

Un-irradiated devices confirmed all the forecasted properties and so it was reasonable to proceed with radiation hardness tests that were first reported in [70]. Irradiations were performed at the Lawrence Berkeley national Laboratory (LBL) synchrotron with 55 MeV protons up to a fluence of 10¹⁵ protons/cm² and at the CERN Proton Synchrotron (PS) with 24 GeV/c protons up to a fluence of 5×10¹⁴ protons/cm². The damage constant was shown to be in agreement with expectations ($\alpha=4\text{-}5\times 10^{-17}$ A/cm), causing a corresponding increase in leakage current. Full depletion voltage was estimated by means of pulsed IR-laser measurement, from the charge collection plateau visible in Fig.3.11(b), which appears at ~105 V for the sample with inter-electrode spacing equal to 100 μm . Pre-irradiation charge collection is reported in Fig.3.11(a) for comparison.

Additional tests performed with a pulsed IR-laser on 3D sensors with wall electrodes [71] were performed, showing a very good charge collection efficiency up few microns away from the physical wall electrode.

Test with a 12.65 keV X-Ray beam were also performed in order to evaluate the spatial response of 3D detectors [72]. The uniformity was found to be very good and the energy resolution equal to 0.91 keV. Columnar electrodes were found to be less efficient but not completely dead.

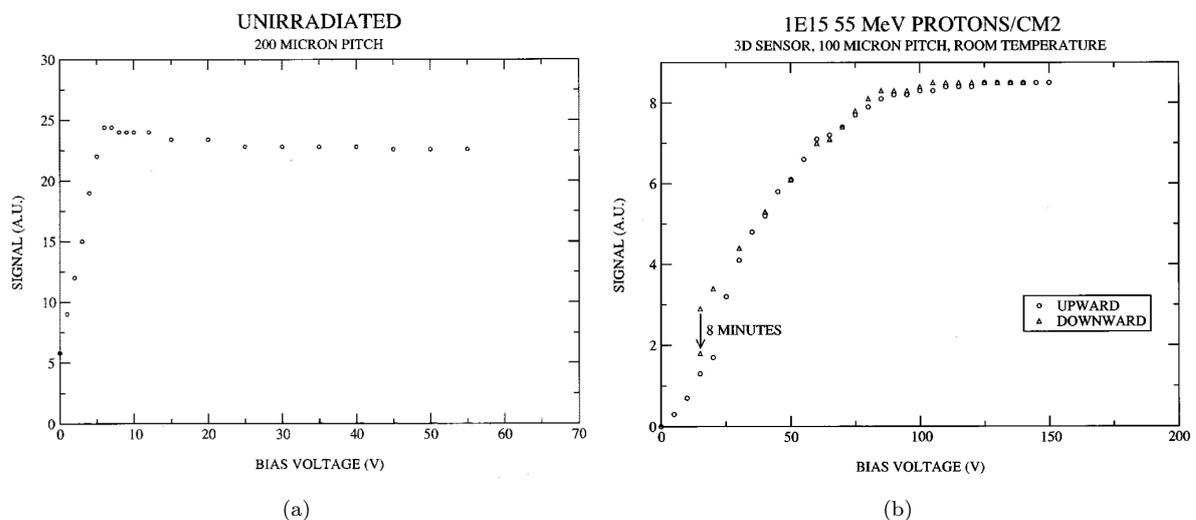


Figure 3.11: Infrared laser tests showing signal amplitude versus bias voltage in pre-irradiation condition (a) and post-irradiation with 55 MeV protons at $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^{-2}$ [70].

Most recent results are focused on proving that full 3D detectors are suitable candidates for the future upgrades of the tracking layers of the experiments at sLHC. Infra-red laser tests were performed on sensors irradiated at different fluences up to $8.8 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ using a fast trans-impedance amplifier as readout [73]. Results for a 3D detector with $71 \mu\text{m}$ pitch are reported in Fig.3.12(a). A large decrease in pulse height is observable with increasing radiation fluence, but the signal is still detectable even at the largest radiation dose. The corresponding signal efficiency is reported in Fig.3.12(b), experimental data are fitted using Eq.3.1 and show a very good agreement.

To prove the tracking capabilities of full 3D detectors, some un-irradiated pixel sensors were bump-bonded to the ATLAS FE-I3 front-end chip (see Chapter 1 subsection 1.3.2) and were measured in a 100 GeV pion beam at CERN SPS [75]. The detected spatial resolution was compatible with what expected for a $50 \times 400 \mu\text{m}$ pixel size and the hit efficiency was reported to be $95.9 \pm 0.1\%$ for an impact angle of 0° , due to losses inside the electrodes, and $99.9 \pm 0.1\%$ in case of a 15° track angle. Fig.3.13 compares the Landau distribution of the collected cluster charge for the two tilt angles: low energy hits in Fig.3.13(a) (0° tilt) are caused by particle passing through the columnar electrodes and are not present in Fig.3.13(b) (15° tilt). A possible matter of concern is represented by the larger Landau distribution measured at 15° inclination: the lowest detect charge was 5 ke^- , very close to the system threshold, that might affect the tracking efficiency after irradiation when the noise will be larger. Additional test beam measurements proved the very good tracking efficiency of the edge region due to the active edge ($10\text{-}12 \mu\text{m}$ probably dominated by the beam size). Measurements were also performed after irradiation with

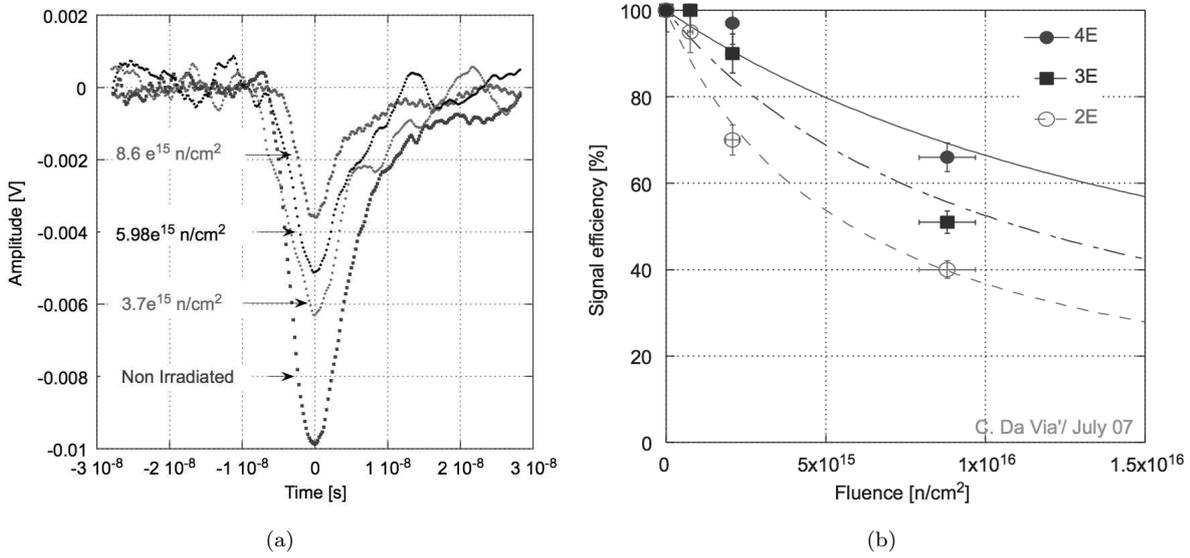


Figure 3.12: Infra-red (1060 nm) pulsed laser measurements on a silicon 3D detector (averaged 1000 times), for different radiation fluences are compared (a) [74]. Signal efficiency versus fluence (b) [73].

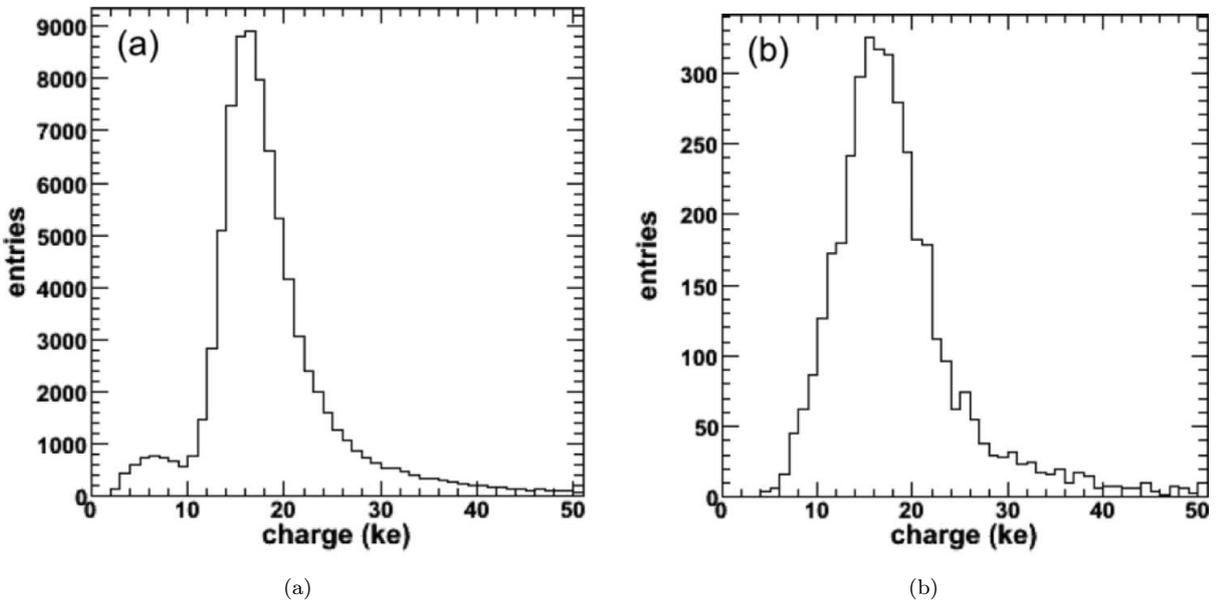


Figure 3.13: Measured cluster charge distribution for a 100 GeV pion beam with different incident angle: 0° angle (perpendicular to the device surface) (a) and 15° angle (b) [75].

24 GeV/c protons up to 10^{15} n_{eq}/cm^2 but, due to sensor damage caused by bad handling, the maximum operating voltage was 5 V, value for which the overall efficiency dropped to 21%.

After the first prototypes were tested and found working with satisfactory performances, it was time to start verifying the feasibility of a medium volume production of 3D detectors in view of the future upgrades at high energy physics experiments. A technology transfer was performed between Stanford Nano Fabrication Facility and SINTEF MiNaLab, Oslo, Norway. The first batch of full 3D detectors fabricated at SINTEF was completed in February 2008 [76, 77]. Many structures were available and in particular FE-I3 compatible pixel detectors, which showed leakage currents in the order 0.5-1.2 nA per pixel and breakdown voltages >80 V, well above the expected full depletion voltage of 3D detectors. The inter-pixel resistance was measured to be between 100 and 800 M Ω confirming that the p-spray isolation was working properly. Preliminary tests with the FE-I3 readout showed controversial results, but the characterization with an ^{241}Am source showed that devices were properly working. In addition, 3D pixel sensors compatible with the CMS PSI46V2 readout chip have been simulated [79] and tested in a 120 GeV proton beam at Fermi National Accelerator Laboratory (FNAL), Batavia, IL, USA [80]. Simulation and measurements of electrical quantities were in good agreement and functional characterization showed noise values lower than 450 electrons, full charge collection at about 30 V and tracking efficiencies in the order of 98.5%.

3.3 Description of alternative approaches to 3D technology

The fabrication process of full 3D devices is complicated because it includes several non-standard steps such as DRIE and wafer bonding. In the past years, several simplified approaches to 3D sensor technology were attempted aiming at a reduction of the fabrication complexity. The most relevant simplified approaches are sketched in Fig.3.14 in comparison with the original full 3D approach.

The first simplified approach is represented by the so called Single Type Column (STC) technology (Fig.3.14(b)) and was independently attempted at Fondazione Bruno Kessler (FBK), Trento, Italy [81] and Valtion Teknillinen Tutkimuskeskus (VTT), Espoo, Finland [82]. This architecture only implements one type of columnar electrode etched from the front side and leaves the other type planar on the back side. Implemented 3D electrodes are not completely passing through and not filled with polysilicon. This translates in a great reduction of the fabrication complexity because there is no need for a support wafer and all the steps required for electrode filling are not necessary. Moreover, only one DRIE step is required. STC devices shows a rather slow response to impinging

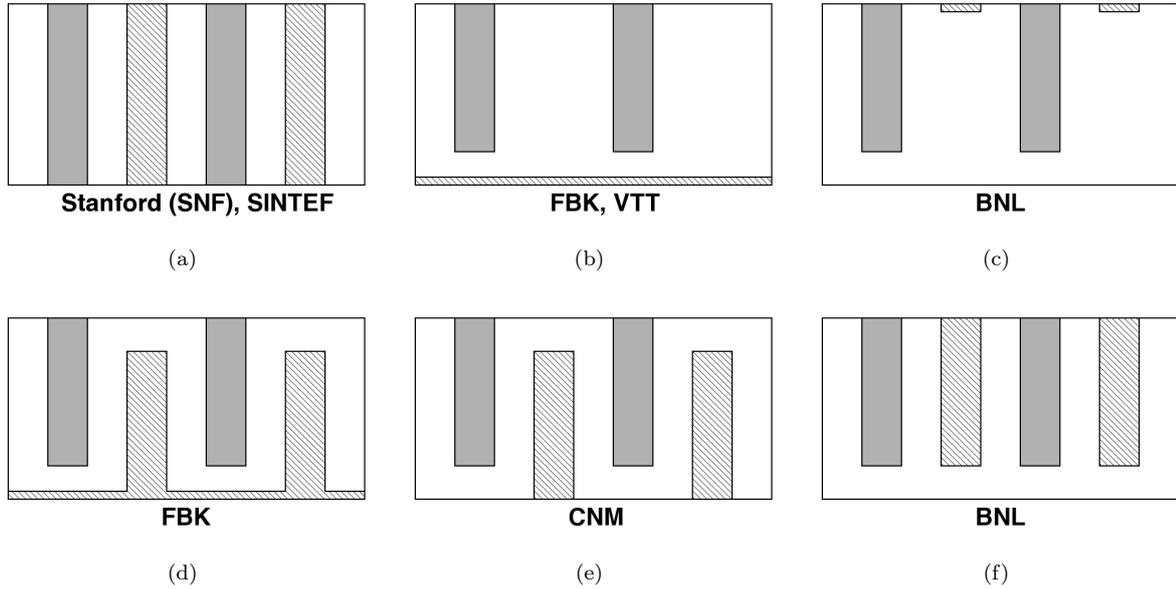


Figure 3.14: Schematic representations of all the proposed approaches to the 3D technology: the original architecture (a) is compared with: Single Type Column implementations from FBK/VTT (b) and BNL (c), Double Sided Double Type Columns from FBK (d) and from CNM (e) and finally the single sided double type column from BNL (e).

particles and feature rather large low field regions, in which free carriers must move by diffusion, thus strongly limiting the sensor performance. They were, in fact, extensively tested in laboratories and beam tests, finally proving to be not sufficiently radiation hard to be used at the fluences expected in sLHC experiments [84]. A similar STC approach was also proposed by Brookhaven National Laboratories (BNL), Upton, New York, USA [83] in collaboration with Centro Nacional de Microelectrónica (CNM), Barcelona, Spain (see Fig.3.14(c)). The main difference of this technology with respect to FBK's and VTT's, is in the fact that the planar electrode is realized and patterned on the front side, allowing to implement the so called "stripixel" configuration [83]. Mainly simulation results are available on this technology and only a few preliminary leakage current measurements.

The natural evolution of the STC technology is the realization of 3D silicon detectors with columnar electrodes of both doping type. This technology is known as *Double-sided Double Type Column (DDTC)* and was independently proposed by FBK [85] (sketched in Fig.3.14(d)), and Centro Nacional de Microelectrónica (CNM), Barcelona, Spain [86] in collaboration with the Univeristy of Glasgow (sketched in Fig.3.14(e)). These new devices feature not passing-through, empty electrodes of both doping type, etched from opposite sides of the wafer, junction columns from the front side and ohmic columns from the back side. This technology is relatively more complicated than STC but still much

easier than full 3D technology, because no support wafer is required and the filling of the electrodes is not necessary. The main differences between FBK's and CNM's technologies are related to the column depth, which, as discussed later, is not fully optimized for FBK devices, and the surface isolation, realized with a combination of p-spray/p-stop at FBK and p-stop at CNM. Moreover, columnar electrodes in CNM devices, are partially filled with polysilicon to make contact with the metal on wafer surfaces. Additional details about FBK's 3D-DDTC technology are reported in section 3.4 while, because this thesis is strongly related to FBK's technology, only a summary of the most relevant results from CNM devices are reported in section 3.5.

In addition to the discussed simplified technologies, a single sided double type column approach was proposed at BNL (Fig.3.14(f)) but no results are available.

Finally, the most recent developments at FBK led to the consolidation of a better 3D-DDTC technology with fully passing through columns, purposely designed for the ATLAS Insertable B-Layer. Latest development at FBK are fully described in Chapter 4.

3.4 3D-DDTC at FBK

To overcome performance limitation of the previous STC technology, 3D-DDTC detectors were designed at University of Trento, Italy, and fabricated at FBK. In this section the most relevant results from the electrical and functional characterization will be shown and discussed, also highlighting limitations and possible improvements.

3.4.1 Numerical device simulation

Electrical properties of DDTC devices were investigated through TCAD simulations performed on a quarter of unit cell of an n-in-p detector with $80 \mu\text{m}$ pitch between electrodes of the same doping type [85]. The simulated structure reproduces a $40 \times 40 \times 250 \mu\text{m}^3$ cell with one electrode per doping type. The bulk concentration was set to $2 \times 10^{12} \text{ cm}^{-3}$ and the p-spray surface isolation was also implemented. The electrical behavior of the device is studied by parametrizing the depth of the columns and by reverse biasing it. Results are compared to what expected for a full 3D detector. The simulated electric field distribution, extracted from the diagonal between two electrodes of opposite doping type, is reported in Fig.3.15 for different geometrical configurations. The investigated distances between the tip of the electrode and the opposite wafer surface "d", span from $0 \mu\text{m}$ (full 3D) to $75 \mu\text{m}$ in steps of $25 \mu\text{m}$. The field distribution is very uniform when columns are passing through while it gets more and more distorted when the column tip to wafer surface gap increases, strongly enlarging the low field regions inside the device.

The functional behavior of the same structures was investigated by means of transient

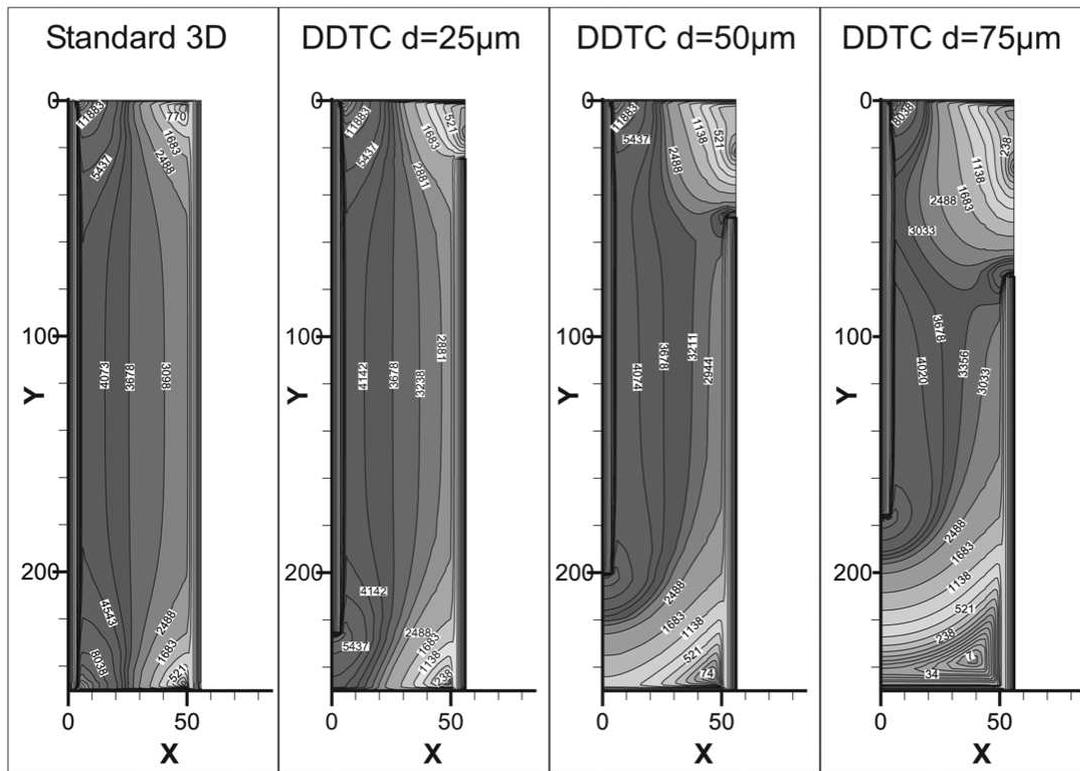


Figure 3.15: Simulated electric field distribution extracted from a plane crossing the diagonal between two electrodes of opposite doping types. The junction column is placed at $x=0 \mu\text{m}$ and the ohmic column is placed at $x=40 \mu\text{m}$. From left to right the distance between the electrode tip and opposite surface is modified from 0 to $75 \mu\text{m}$ in steps of $25 \mu\text{m}$ [85].

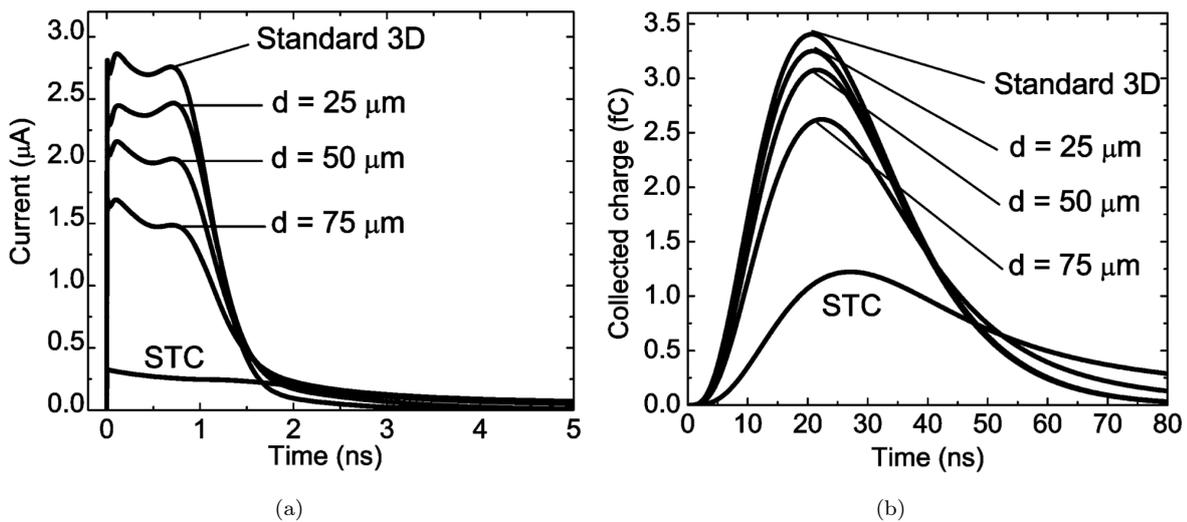


Figure 3.16: Transient simulations of 3D detectors hit by a minimum ionizing particle. Different geometries are tested differing in the tip to opposite surface distance. Applied bias voltage is 16 V. Induced signals are reported in (a) and equivalent shaped signals after a $CR\text{-}RC^3$ shaper are shown in (b) [85].

simulations with a MIP impinging the device close to the p^+ electrode. Simulated currents for the different tested solutions are reported in Fig.3.16(a) and are also compared to the response of a full 3D detector and an STC detector. The signals are then numerically integrated and elaborated to simulate a readout system with a CR-RC³ shaping amplifier with 20 ns peaking time, emulating the readout of the ATLAS SCT detector (Fig.3.16(b)). These results are extremely important because they show that, if $d \leq 25 \mu\text{m}$, devices behavior is comparable to the one of a full 3D sensor with only a 10% difference in the total collected charge.

3.4.2 Fabrication technology

Two different wafer layout were designed and fabricated on n-type and p-type FZ wafers [87]. At the time of the fabrication, the DRIE equipment was not available in house, so an external service at IBS, France, was used. Preliminary tests showed that the maximum achievable column depth, with a 10 μm diameter, was 180 μm . The first batch was realized on 300 μm thick n-type wafers, so that the column depth was not expected to be optimal. The second batch, instead, was fabricated on 200-220 μm thick p-type substrates promising a larger electrode overlap region.

The first n-type batch (also know as DTC-1), mainly contained 3D diodes and 3D strip detectors compatible with the ATLAS SCT readout [15], while the second p-type batch (also known as DTC-2) included, besides 3D diodes, 3D pixel detectors compatible with both the ATLAS FE-I3 readout chip and the CMS PSI46V2 readout chip (additional details about readout chips are reported in Chapter 1 sections 1.3.2 and 1.4.2). A summary of the main features of both batches, is reported in Tab.3.1.

The fabrication process of the two batches is almost identical, it differs only by two steps: when the bulk is p-type and the readout is n-type, an additional step is required to implant the p-spray isolation between n^+ regions; in the p-type batch n^+ columns are etched from the front side and p^+ columns from the back side and vice-versa in the n-type

Table 3.1: Main features of both batches of 3D-DDTC devices fabricated at FBK [85].

Parameter	3D DTC-1	3D DTC-2
Bulk type	n-type	p-type
Bulk thickness	300 μm	200-220 μm
Maximum column depth	180 μm	180 μm
Strip design	AC/DC coupled	AC/DC coupled
Strip pitch	80/100 μm	80/100 μm
Pixel design	ALICE, Medipix1	ATLAS, CMS

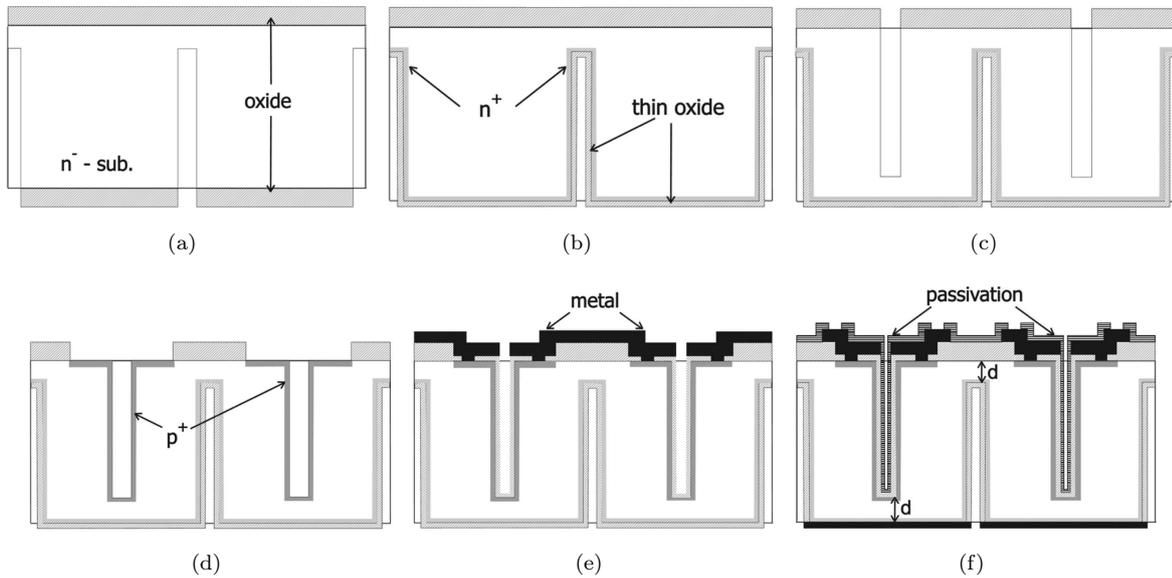


Figure 3.17: Main fabrication steps of FBK 3D-DDTC detectors realized on n-type substrate. Description in the text [85].

batch. In case p-stop is also implemented, an additional mask is required. The fabrication steps here reported are relative to the DTC-1 batch [85] and process sketches are shown in Fig.3.17:

- a. Growth of a thick oxide layer that will act as passivation and mask for the DRIE process on both wafer surfaces. Backside oxide opening and DRIE step of ohmic columnar electrodes.
- b. Removal of the oxide on the backside and doping of columns and wafer surface by phosphorus diffusion from a solid source. Growth of a thin oxide layer to prevent the dopant to diffuse out.
- c. Patterning of the front oxide and DRIE step on the front side to realize the junction columnar electrodes.
- d. Removal of the thick oxide around the columns to allow for the following boron diffusion of both holes and surface. A surface planar diffusion is needed to make contact with the metal since columns are empty.
- e. Deposition of a thin oxide to prevent the dopant to diffuse out. Contact holes are defined and etched through the oxide. Aluminum is sputtered and patterned.
- f. Deposition of the final passivation layer. Opening of the passivation to allow access to the metal pads. Uniform aluminum sputtering on the back side without passivation.

3.4.3 Experimental results from the DTC-1 batch

After the fabrication process was completed, a thorough investigation was performed on many of the available devices. The on-wafer characterization of silicon detectors typically starts from standard test structures, in order to estimate process related parameters and to test the goodness of the wafers. The focus is later moved to 3D structures of interest, in order to evaluate their electrical properties and to separate good from bad sensors. Wafers are finally cut and sent to different research groups that have the capabilities to perform a complete functional characterization. The most relevant results for the first batch of 3D-DDTC devices (DTC-1) fabricated at FBK is here reported.

Planar test structures

The wafer layout includes several standard planar test structures and among them, planar diodes with a guard-ring, MOS capacitor and gated diodes. The leakage current density was estimated to be 3.2 ± 0.3 nA/cm² and planar diodes had breakdown voltages larger than 350V. Bulk generation lifetimes, extracted from the reverse current of planar diodes, were satisfactory and in the order of 20 ns. Capacitance measurements on planar diodes returned a rather low value of bulk doping concentration of about $1.2 \pm 0.2 \times 10^{11}$ cm⁻³. Capacitance measurements on MOS capacitors allowed to extract a fixed oxide charge concentration of $4.4 \pm 0.6 \times 10^{11}$ which is higher than expected and can be attributed to the thick TEOS layers deposited on the wafer surface as mask for the DRIE step. Surface recombination velocity, extracted from gated diodes, is equal to 1.5 ± 0.7 cm/s in agreement with expected values. Additional details are available in [85].

3D diodes

To facilitate the characterization of the devices, 3D test structures were also included in the wafer layout. Considered structures are 3D diodes with a total area of 2.56 μm. Two different inter-electrode pitches are available, 80 μm and 100 μm, mimicking the geometries of strip detectors. Diodes are made of arrays of columns of 20×20 or 16×16 for the 80 μm and 100 μm pitch respectively. Columns of the same doping type are connected together by a metallization or a surface doping in order to obtain a two terminal device. Beside DTC 3D diodes, STC 3D diodes are also available on the same wafers.

Full depletion voltages can be estimated by extracting the voltage at which the capacitance value saturates. In these diodes, where columns are not passing through the entire silicon bulk, the C-V measurement typically shows a double "knee", one when the lateral depletion between electrodes is achieved, and the other one when the volume under the column tips is depleted. Full depletion voltage was found to be lower than 5 V.

Junction column depth was estimated from C-V measurements on STC 3D diodes [88] and was found to be about $190 \mu\text{m}$ over a total bulk thickness of $300 \mu\text{m}$. Since ohmic columns were not present in STC diodes, their depth was estimated from C-V measurements on DTC diodes. Measurements were fitted using a cylindrical capacitor model as explained in [85] and the column depth was found to be between 160 and $170 \mu\text{m}$. The leakage current saturated at very low voltages and was found to be as low as 0.1 pA/column in full depletion. No signs of breakdown were observable on STC diodes up to very large voltages, while some DDTC diodes showed a current rise even at low voltage that might be caused by defects in the column walls. Most important parameters for 3D structures are summarized in Tab.3.2.

Table 3.2: Summary of electrical and geometrical parameters of the first DDTC batch realized on n-type substrates extracted from test structures [85]

Parameter	unit	Value (STC)	Value (DTC)
Junction column depth	μm	180-190	180-190
Ohmic column depth	μm	n.a.	160-170
Lateral depletion voltage	V	< 0.5	< 0.5
Full depletion voltage	V	~ 1.5	~ 1
Leakage current at full depletion	pA/column	0.1-0.5	0.1-0.7
Backplane capacitance	fF/column	5-8	18-20

3D strip detectors

Functional characterization was performed on 3D strip detectors at University of Freiburg using the ATLAS SCT ABCD3T readout [15]. Device under test were strip sensors with a total area of 1 cm^2 and featuring 102 strip containing 102 columns each ($80 \mu\text{m}$ pitch between columns of the same doping type). The characterization was performed using two distinct setups. The first setup made use of a 980 nm pulsed laser, to scan the detector using motorized stages in both x and y coordinates with a precision of $1 \mu\text{m}$, in order to obtain a very precise charge collection map. The laser was focused down to $\sim 2 \mu\text{m}$ onto the detector surface with a microscope optics. The second setup used a ^{90}Sr beta source to investigate the detector response to MIP particles. The measurement was triggered by two scintillators working in coincidence and placed behind the device under test.

Laser scans performed with a $2 \mu\text{m}$ step in both x and y coordinates for two different bias voltages of 0.5 V and 40 V are reported in Fig.3.18. The investigated area corresponds to a cells of $50 \times 50 \mu\text{m}^2$. The metal pattern is visible in both images due to the reflectivity of the aluminum. When the bias voltage is low (Fig.3.18(a)), full depletion is not reached yet, and only the region close to the junction electrode in the top right corner is sufficiently

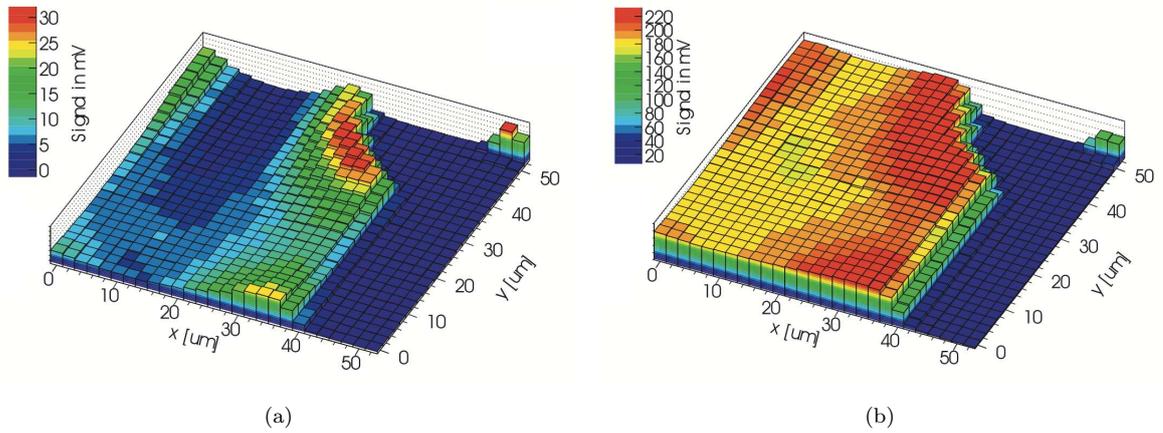


Figure 3.18: Laser scans performed at 0.5 V of bias (a) and at 40 V of bias (b). The scanned region corresponds to a cell of size $50 \times 50 \mu\text{m}^2$ and the x and y step is equal to $2 \mu\text{m}$ [84].

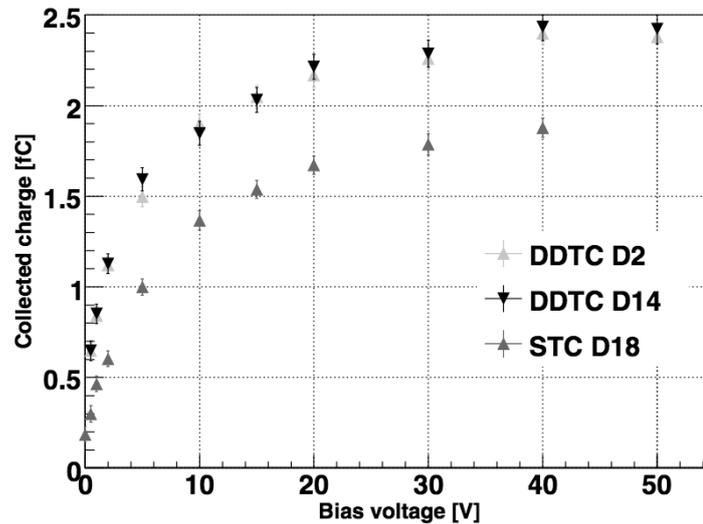


Figure 3.19: Charge collection as a function of applied bias voltage for two 3D-DDTC strip detectors in response to MIP particles. An STC device is reported for comparison [84].

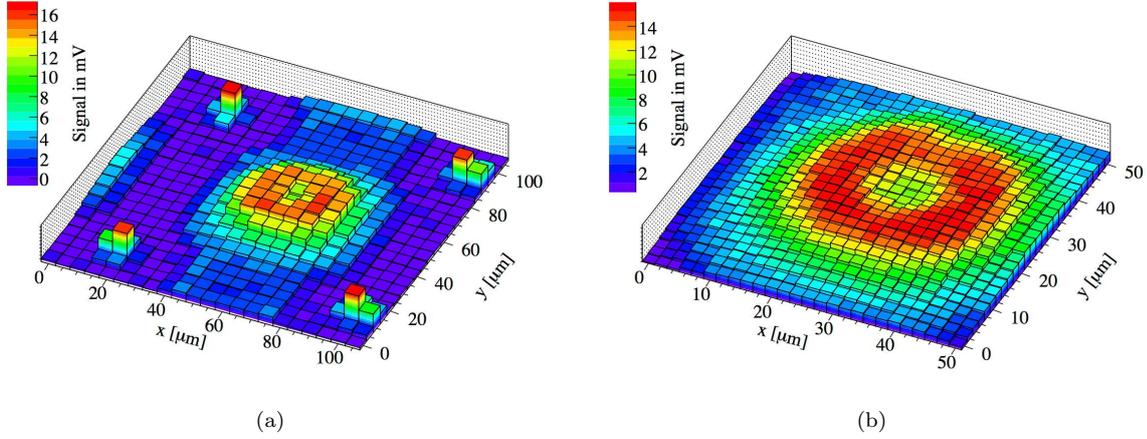


Figure 3.20: Laser scan results for a 3D strip detector irradiated at $5 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$ for a bias voltage of 10 V. Large area scan with $5 \mu\text{m}$ step (a) and finer scan of the inner region with $2 \mu\text{m}$ step (b) [84].

active. By increasing the bias up to 40 V (Fig.3.18(b)), the scanned area becomes much more uniform although the bottom left corner of the cell results less efficient because of the presence of the ohmic column etched from the opposite side.

Charge collection plots obtained with the beta particle setup are reported in Fig.3.19 also including an STC strip detector as comparison. Charge collection for both investigated 3D-DDTC devices saturates at 40 V of bias to a value of roughly 2.4 fC, lower than the expected value for devices fabricated on $300 \mu\text{m}$ thick substrates (3.5 fC). The cause of this is well understood and is related to the non-optimized column depth that cause part of the generated carriers to move in low field regions, thus causing ballistic deficit at very fast shaping times. Nevertheless 3D-DDTC devices show a great improvement with respect to the STC devices in which collected charge saturated at only 1.8 fC.

Devices under test were irradiated with 24 MeV protons at Karlsruhe Institute of Technology (KIT), at three different fluences: 5×10^{14} , 1×10^{15} and $2 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$, the last one being the expected fluence received by short strips in the ATLAS SCT after 5 year operation in sLHC conditions. After irradiation, samples were annealed for 80 minutes at $60 \text{ }^\circ\text{C}$ in order to exploit beneficial annealing. Laser scans were performed again, and the most relevant results are discussed in [84]. The scan result for the device irradiated at $5 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$ is shown in Fig.3.20. The scanned region corresponds to an area of $100 \times 100 \mu\text{m}^2$, the measurement is performed at 10 V of bias and with a scan step of $5 \mu\text{m}$. The readout columns are in the four corners and an ohmic column is in the middle. The result shown in Fig.3.20(a) shows how the bulk was type inverted after irradiation because the more efficient region is now located around the backside column, suggesting that the depletion region proceeds from the backside columns toward the front side ones.

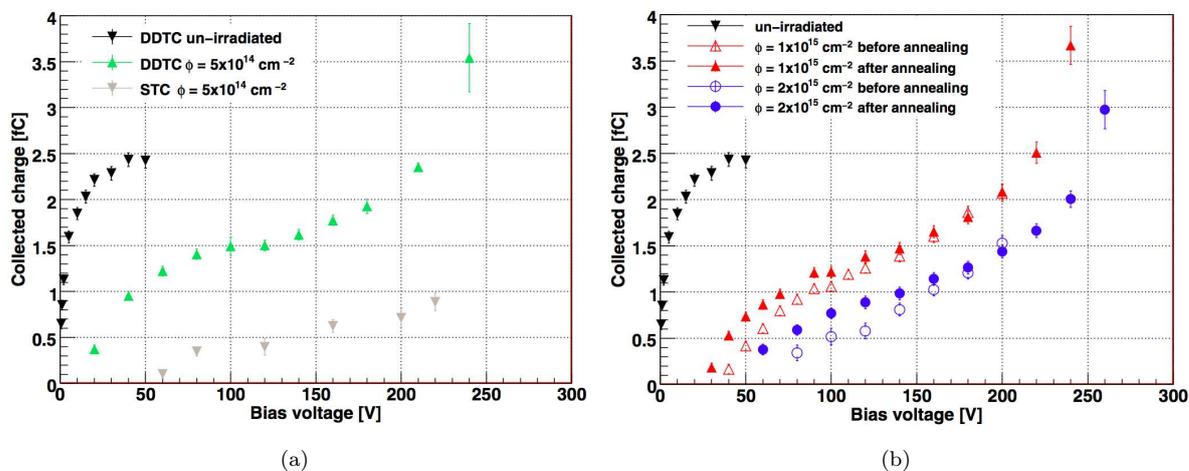


Figure 3.21: Comparison between the pre-irradiation and the post-irradiation collected charge for DTC-1 strip detectors irradiated at different fluences: $5 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$ (a) and $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ and $2 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ (b) [84].

Some peaks are also visible close to the junction columns and are probably related to the double-junction effect. A finer scan of the central region was performed with a $2 \mu\text{m}$ scan step and demonstrated that the device was not laterally depleted at this voltage, because the charge was primarily collected only from the surroundings of the backside column.

Irradiated sensors were again tested in the beta particle setup as well. The temperature was kept at $-10 \text{ }^\circ\text{C}$, allowing to lower the device leakage current and reaching high voltages without corrupting the noise performance of the system. Measurement results are reported in [84] and are briefly described here. Fig.3.21(a) shows the collected charge as a function of the bias voltage for the device irradiated at $5 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$, compared to the behavior pre-irradiation and to the result obtained with an STC strip detector irradiated at the same fluence. It is easy to understand how radiation damage causes a rather large charge loss: the collected charge tends to saturate at 1.5 fC (about 1 fC less than before) for a bias voltage of 100V (charge saturation was shifted of about 80 V). It is important to notice how 3D-DDTC technology marks a rather important improvement with respect to STC, which was not intended for this type of fluences and did not perform well. Results for the sensors irradiated at the two higher fluences are reported in Fig.3.21(b) comparing the pre-irradiation results with those after irradiation and after annealing. A large reduction in collection efficiency is visible in these conditions because of the large trapping caused by radiation: trapping times for these fluences are expected to be in the order of 1-2 ns, and only the charge generated in the column overlap region can therefore be collected without getting trapped. Despite the large reduction in collected charge, device performances are acceptable and comparable with those of planar devices but with the advantages that a

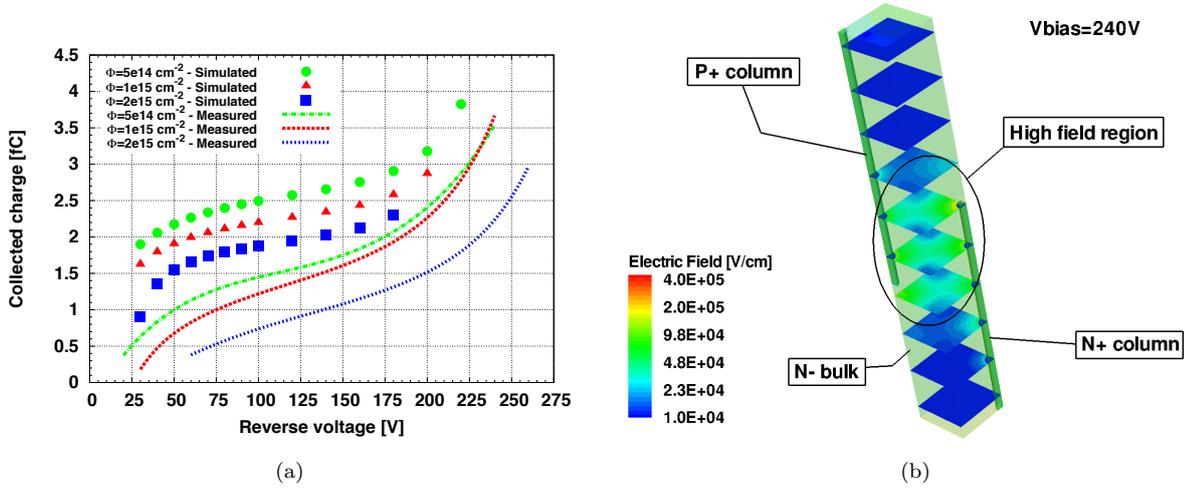


Figure 3.22: Simulated charge collection for irradiated DTC-1 strip devices with charge multiplication compared to measured results (a) and simulated electric field distribution at a bias voltage of 240 V for a device irradiated at $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ (b) [92].

much lower operating bias is needed for 3D detectors. As a comparison, in order to collect the same amount of charge in planar strip detectors irradiated at the same fluence, biases up to 1000 V were applied [89].

An interesting phenomena is observable for all irradiated devices: after charge saturation was reached, the bias voltage was increased up to the maximum level allowed and collected charge started rising again in an exponential fashion. This effect can be ascribed to charge multiplication triggered by particles.

To get a better insight into device behavior in these particular conditions, a detailed TCAD simulation campaign was performed with the aid of the Synopsys Sentaurus TCAD tools [90]. The structure editor allows to realize a 3D structure reproducing all the geometrical properties of the real device and the meshing engine creates the discrete grid of nodes and elements to be loaded into the simulator. The poisson equation, continuity equation and all the differential equation relative to silicon devices are then solved using advance numerical methods. The simulator allows to enable a vast set of physical models to better describe the simulated device and the operating conditions, in particular, traps can be inserted in the bulk in order to emulated radiation damage. The trap model used in the simulations is specifically tuned to predict charge collection in devices realized on n-type substrates; it is a 3-level model implementing two acceptor and one donor [91]. The simulated structure reproduces a quarter cell of a 3D-DDTC, p-in-n, strip detector with $80 \mu\text{m}$ pitch. A positive bias ramp is applied to the backside (n^+) electrode, keeping the frontside (p^+) electrodes grounded. Biasing conditions for specific voltages are saved and used as initial conditions for a second simulation step, a transient simulation with

a MIP impinging the structure at $t_{MIP}=0$, half way along the diagonal between the two electrodes. Simulated signals require some post-processing in order to compare them to measured collected charge: the leakage current is subtracted from the output and the signal is then fed to a script that emulates a charge sensitive preamplifier followed by a CR-RC³ shaping amplifier with a peaking time of 20 ns. The simulated collected charge is then plotted as a function of the bias voltage and is shown in Fig.3.22. The onset of the charge multiplication is predicted with a good precision but simulations seem to overestimate the values of collected charge. This is caused by mainly two factors: (i) strips are biased using the punch-trough mechanism which could affect the effective bias applied to the single strip and (ii) the simulated particle crosses the device in one of the most favorable positions, along the diagonal between two electrodes, where the electric field is maximum and therefore the trapping is less critical. It is very important to notice that, the charge multiplication effect, is typically triggered only when the electric field inside the device is sufficiently high, in the order of $1-2 \times 10^5$ V/cm. The simulated electric field distribution, for a device irradiated at 1×10^{15} n_{eq}/cm² and biased at 240 V, is reported in Fig.3.22(b). The field inside the structures is relatively low everywhere, apart from the region where columnar electrodes overlap and, in particular, around the electrode tips, where it reaches values in the order of 2×10^5 V/cm, allowing the multiplication to occur. The charge multiplication is not visible before irradiation because the maximum bias voltage is typically not sufficiently high to reach the necessary electric field values. A more detailed description of numerical simulation of 3D detectors can be found in [92] also mentioning the simulation of charge multiplication effects.

3.4.4 Experimental results from the DTC-2 batch

The second batch of 3D-DDTC sensors (DTC-2) fabricated at FBK in 2008, was produced on 200-220 μm thick, p-type substrates. Taking advantage of the higher radiation hardness delivered from n⁺ readout (see Chapter 2 subsection 2.5.2), n-in-p devices were realized. Since n⁺ readout is used, a surface isolation is needed on the front side of the wafer. This is implemented with a combination of p-stop and p-spray implantations [85]. The electrical characterization was performed on planar and 3D test structures exactly as described previously [93]. The bulk doping concentration was extracted from C-V measurements on planar diodes and was found to be equal to 1×10^{12} cm⁻³. Leakage currents were very low, in the order of few nA/cm² for both STC and DDTC 3D diodes. From C-V plots it was also possible to extract lateral depletion voltage (~ 4 V) and full depletion voltage ($\sim 15-20$ V) from both diode types. Column depths were estimated from C-V measurements as well, returning values in the order of 180-190 μm for the ohmic (p⁺) column and 100-110 μm for the junction (n⁺) column. This last value was unexpectedly low and was caused by

Table 3.3: Summary of electrical and geometrical parameters of the DTC-2 and DTC-2B batches realized on p-type substrates extracted from test structures [85].

Parameter	unit	Value (DTC-2)	Value (DTC-2B)
Substrate thickness	μm	200-200	200
Substrate doping concentration	cm^{-3}	1×10^{12}	7×10^{11}
Junction column depth	μm	100-110	140-170
Ohmic column depth	μm	180-190	180-190
Column overlap	μm	90-100	110-150
Lateral depletion voltage	V	3-4	1-2
Full depletion voltage	V	12	3-4
Leakage current at full depletion	pA/column	<1	<1
Backplane capacitance	fF/column	30-35	45-50
Bredown voltage	V	>70	>70

major problems during the DRIE step, nevertheless it allows for a total electrode overlap of about $120 \mu\text{m}$, that should provide a great performance improvement with respect to the DTC-1 batch. In addition, the same wafer layout was implemented in a recycle batch once the DRIE machine was acquired at FBK and was completed by April 2009. This recycle batch was denominated DTC-2B and was electrically characterized with the same procedure [96]. Values similar to the DTC-2 batch were found, the main discrepancy being the depth of the junction columns, which resulted deeper, delivering a higher electrode overlap. Tab.3.3 summarizes the most important electrical and geometrical parameters of the DTC-2 and DTC-2B batches.

The functional characterization of devices from this batch was mainly performed on strip and pixel detectors compatible with the FE-I3 readout chip and is reported in the following subsections.

3D strip detectors

Strip detectors from the DTC-2 batch were characterized in pre-irradiation conditions at University of Freiburg with the ATLAS SCT ABCD3T readout, using the same laser and beta particle setups previously described [94].

Laser scans were performed on an area of $100 \times 100 \mu\text{m}^2$ with a step of $2 \mu\text{m}$ in both x and y directions. The scan results for two different bias voltages (5 and 20 V) are shown in Fig.3.23. The signals for two adjacent strips are readout, summed and plotted. For low bias voltage (Fig.3.23(a)) only the region closer to the junction columns are depleted and, therefore, a rather large area of the device results inefficient. By increasing the bias voltage up to 60V (Fig.3.23(b)) more uniformity is achieved although the scan is still

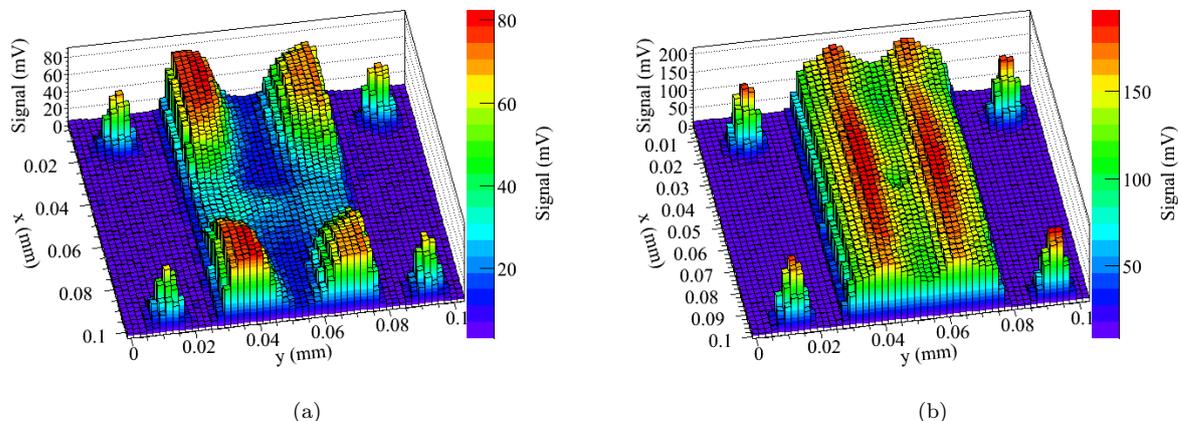


Figure 3.23: Pre-irradiation laser scans performed on a DTC-2 strip detector for two different bias voltages: 5 V (a) and 60 V (b) [94].

not fully uniform. In previous generation detectors (DTC-1), where the column overlap was not optimized, charge collection was affected by ballistic deficit at fast shaping times. This should not be the case with DTC-2 thanks to the much extended column overlap: in fact simulations indicated that the worst case signal duration is in the order of 10 ns [95]. Signal variations in the devices under test, might be scribed to several factors: (i) higher signal is expected along the p-stop strips, where the surface passivation layers are thinner and assure higher light transmission efficiency; (ii) lower signal is expected in the center of the cell where the ohmic column is present and finally, (iii) due to weighting field distribution, the non collecting strip can induce a fast signal of opposite polarity on the collecting strip thus causing a partial compensation when signals are summed.

Sensor response to minimum ionizing particles was studied by means of a ^{90}Sr beta particle source [94]. Collected charge and detection efficiency as a function of the bias voltage are shown in Fig.3.24. The charge collection plot reported in Fig.3.24(a), shows a rather slow increase with bias voltage and saturation is not clearly reached. Moreover, the expected charge for this sensor (200 μm thick) in the considered measurements setup, is equal to 2.12 ± 0.05 fC [94], larger than the maximum measured value of about 1.9 fC. This discrepancies can be explained as follows: (i) the not complete saturation of the collected charge, can be ascribed to the punch-through mechanism that, as will be explained later, was not working properly and resulted in a lower effective bias voltage applied to the strip, while (ii) the loss in total collected charge occurs because of the low value of the AC coupling capacitor integrated in the strip with respect to the other parasitic capacitances. This latter effect, is caused by a rather thick oxide layer on the wafer surface, needed as mask for the DRIE step, resulting in a non efficient charge transmission. This problem

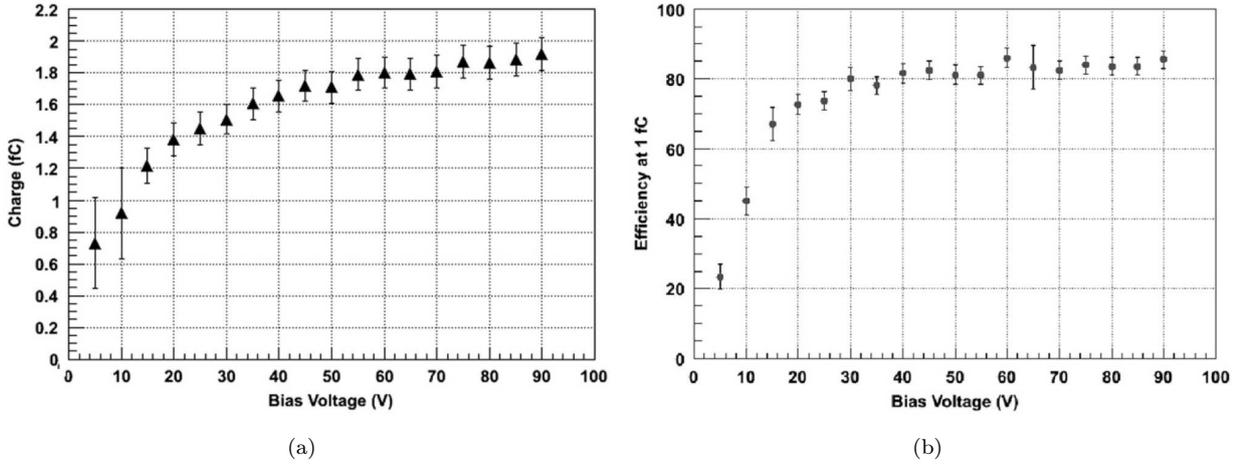


Figure 3.24: Beta particle results for a DTC-2 strip detector in pre-irradiation conditions. Collected charge (a) and sensor efficiency (b) are here shown [94].

can be solved by using external RC fan-ins, connected to the strip DC pads, while the former can only be fully correct by intervening on the sensor geometry as was done in later technologies (see Chapter 4).

The efficiency measurement reported in Fig.3.24(b), is obtained for a threshold of 1 fC and is calculated over 50 strips, corresponding to the area span of the beam profile of the beta source. The efficiency increases rapidly with bias voltage but it saturates to rather low values, about 85%. This low efficiency is caused by two dead readout channels in the region where the source intensity is high, accounting for an estimated efficiency loss of about 10%. Further efficiency losses can be ascribed to the presence of the empty columnar electrodes, that, occupying roughly a 3% of the total sensor volume, and will always prevent to reach full efficiency when the particle hit angle is 90° .

Devices were later irradiated with 24 MeV protons at KIT up to very large fluences. Unfortunately, after irradiation, it was not possible to measure any signal. Once again, the main suspect was that the punch-through mechanism was not working properly and got worse after irradiation, causing the effective strip bias to be close to zero. The solution to this problem will be discussed in Chapter 4.

3D pixel detectors

Pixel detectors available in batches DTC-2 and DTC-2B were designed to be compatible with the ATLAS FE-I3 readout chip [96]. Different configuration were made available and in particular: two junction columns per pixel (2E), three junction columns per pixel (3E) and four junction columns per pixel (4E). Pixel size and configurations together with a schematic cross-section are reported in Fig.3.25. The bump bonding of some of these

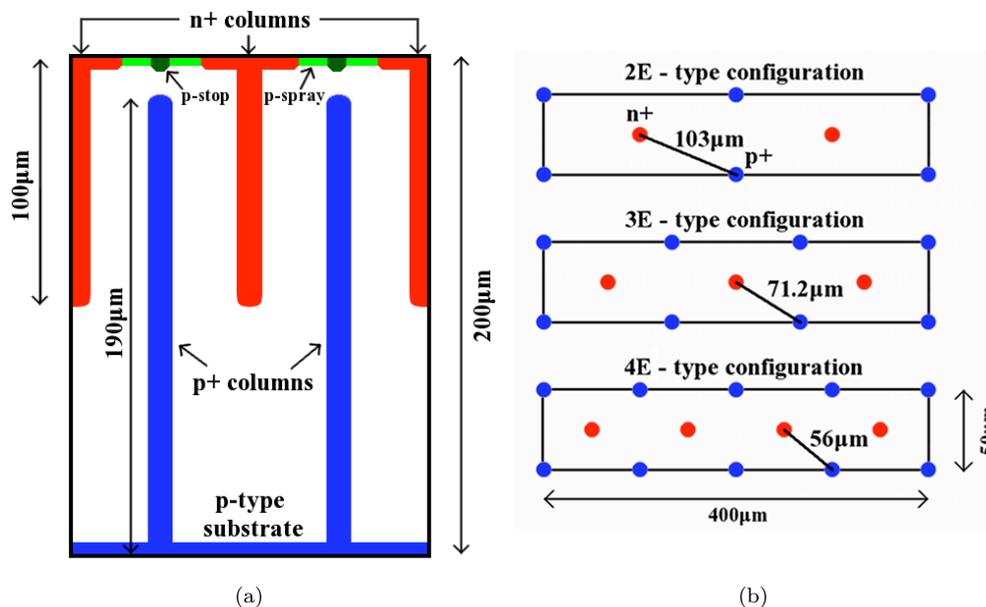


Figure 3.25: Cross-section of a 3D-DDTC device coming from the DTC-2 batch (a) and available FE-I3 pixel configurations (b) [102].

sensors was performed at SELEX SI, Rome, Italy, and assemblies were shipped to different laboratories around the world where they were tested electrically, with radioactive sources and in beam tests.

The pre-irradiation functional characterization was performed in laboratory at CERN and is extensively covered in [96]. The experimental setup was based on the TurboDAQ setup [97]. All measurements were performed in a climatic chamber at a constant temperature of 20 °C with relative humidity of 12%. Sensor I-V measurements were performed after bump bonding and found to be very good (~ 100 pA/pixel), with breakdown voltages of about 70 V, conditions that assure a proper operation of the devices.

The FE-I3 chip operates in Time over Threshold mode (see Chapter 1, subsection 1.3.2). The calibration is performed by means of on-chip charge injectors, which inject an increasing amount of charge in each pixel several times per cycle. The number of recorded hits for each cycle is registered and plotted as a function of the injected charge. In the ideal case a step function is expected but, because of electronic noise, the result is typically represented by an error function (S-curve). The 50% efficiency of the S-curve returns the threshold value for each pixel. The calibration is normally repeated a second time in order to reduce the threshold dispersion. The target threshold value with the FE-I3 chip is normally 3200 electrons. Threshold values and measured noise at 35 V of bias, for the three available pixel configurations, are reported in Tab.3.4. The threshold tuning was successful and the trend in noise is perfectly representative of theoretical expectation, increasing

Table 3.4: Summary of threshold and noise parameters for the three available pixel configurations of sensor coming from the DTC-2 batch at a bias voltage of 35 V [96]. Values are compared with expected pixel capacitance.

Sensor type	Threshold [e^-]	Noise [e^-]	Capacitance [fF]
1E	3200 ± 58.60	202.3 ± 8.96	250
2E	3318 ± 42.02	206.6 ± 8.29	310
3E	3284 ± 41.27	229.8 ± 9.87	370

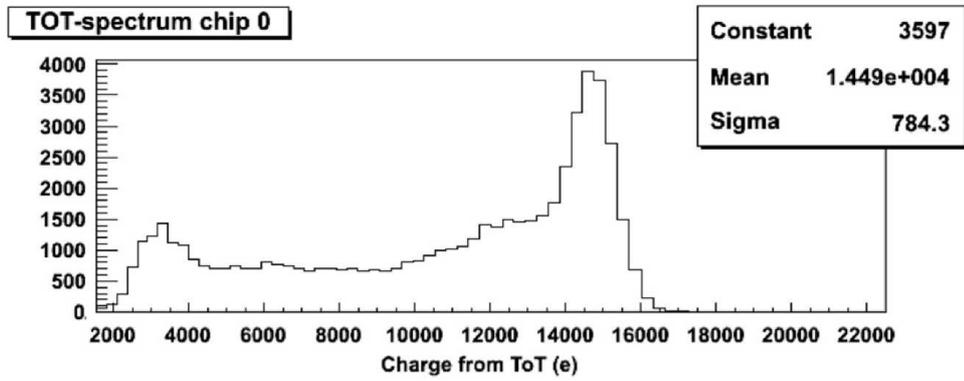
with the number of electrodes per pixel and with shorter inter-electrode distances. Noise trend with respect to bias voltage was also investigated and found in good agreement with the decrease in capacitance due to the increasing depleted volume.

The charge injectors were also used to calibrate the ToT response of a signal to charge values. The standard tuning aims at 60 ToT for an injected charge of 20 ke^- (expected charge value for a mip in a $250 \mu\text{m}$ thick sensor).

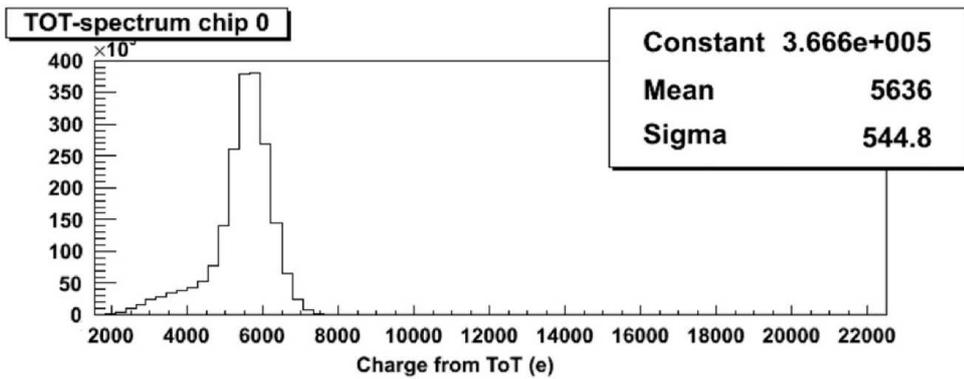
All devices from the DTC-2 batch were tuned successfully while the available devices from the DTC-2B batch, showed premature breakdown due to a few defective pixels. Unfortunately in the early 3D-DDTC technology at FBK, on-wafer chip selection was not possible and some bad pixel sensors were bump bonded as well.

The calibration of the system was performed by means of ^{241}Am and ^{109}Cd gamma sources. This test also allowed to identify dead pixel not showing any signals. The Americium and Cadmium sources emit γ -photons at 60 keV and 22 keV respectively. The photon can convert in a primary electron with the same energy anywhere in the bulk. The expected signal in case of ionization is 16.5 ke^- for the Americium source and 6.1 ke^- for the Cadmium source. If the absorption occurs in a highly doped region, part of the generated charge might be lost due to recombination, thus returning a spectral distribution with a long tail toward lower energies. This is well represented in the measurements shown in Fig.3.26 for a 2E sensor at 35 V of bias. The charge peak reconstructed from the ToT distribution is in agreement with the expectations and well within the uncertainties due to the calibration, which are estimated to be in the order of 10-15%. The tail toward lower energies is also observable.

The functional response of the devices to MIPs, was performed by means of a ^{90}Sr beta source and results for a 2E sensor at 35 V of bias are reported in Fig.3.27 for cluster size 1 (CS1, Fig.3.27(a)) and cluster size 2 (CS2, Fig.3.27(b)) distributions. The Most Probable Value (MPV) for CS1 distributions is about 14.1 ke^- and it increases up to 15.36 ke^- for CS2 distributions. Notice the presence of a low charge tail in the CS1 measurement that is not present in the CS2 result and can therefore be related to charge sharing effects. No dependence on pixel geometry was observed and the collected charge

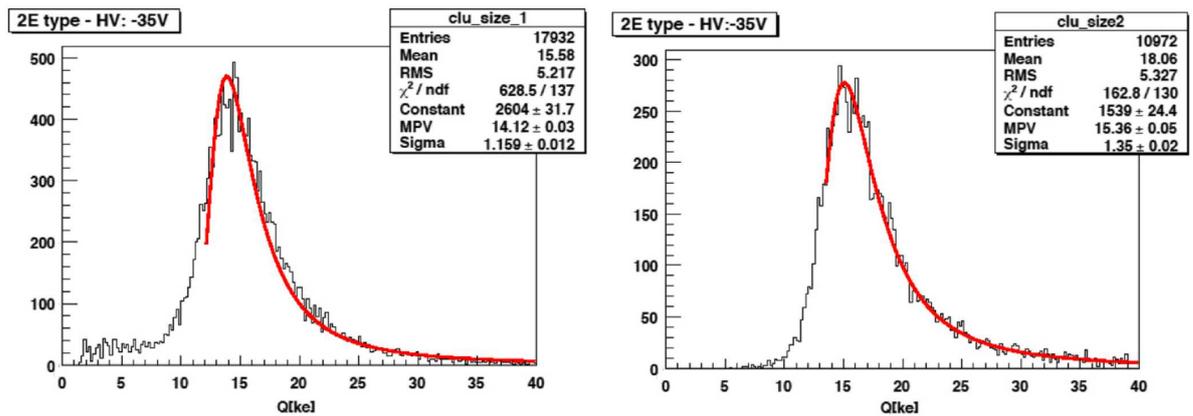


(a)



(b)

Figure 3.26: Collected charge for a 2E pixel detector biased at 35V using ^{241}Am (a) and ^{109}Cd (b) radioactive sources [96].



(a)

(b)

Figure 3.27: Landau distributions as a response of a 2E pixel detector to a ^{90}Sr beta particle source. The device was biased at 35 V and both cluster size 1 (a) and cluster size 2 (b) distributions are shown [96].

value (MPV) was in good agreement with a 250 μm reference planar sensor.

Charge collection efficiency and tracking capabilities were tested, on a DTC-2B detector, in beam tests at CERN SPS North Area, beam lines H6 and H8 [98]. Data were collected in two separate occasions, first using a 120 GeV/c pion beam and then using a 180 GeV/c pion beam which, given the high particle momentum, minimizes the multiple scattering and increases the high precision tracking measurement. Two different setups were available, based on two different telescopes: (i) the Bonn ATLAS telescope [99] and the (ii) EUDET telescope [100]. During the beam test in H8, the setup was mounted inside the Morpurgo dipole magnet, able to provide a 1.6 T vertical magnetic field at the sensor position, in order to test devices in the operating conditions they would face inside the ATLAS tracker. The track reconstruction and data analysis were performed offline and are described in [98]. Data here reported are described as comparison between the full 3D technology and the simplified FBK technology in order to highlight the differences.

The tracking efficiency is defined as the probability of detecting a hit close to a reconstructed track. Bi-dimensional maps of reconstructed data acquired with the EUDET telescope for FBK and Stanford devices are reported in Fig.3.28 and are compared with the pixel layout (3.28(a)). Fig.3.28(b) and Fig.3.28(d) represent the tracking efficiency of an FBK and a Stanford device respectively on a region containing an entire pixel. Due to premature breakdown effects, the FBK device was biased at 8 V, while the Stanford device was biased at 35 V. Nevertheless, even if under biased, the FBK device showed a good tracking efficiency. As already mentioned, electrodes in 3D detectors are partially/completely dead regions because empty (FBK) or highly doped (Stanford), therefore they appear as less efficient regions in the efficiency map. Corresponding 1D profiles extracted from lines crossing junction (blue) and ohmic (red) electrodes are reported in Fig.3.28(c) and Fig.3.28(e) for the FBK and Stanford devices respectively. The FBK device is less effected than the Stanford one because, being the electrodes not completely passing through, the bulk underneath the tips is still present and the charge generated there can be collected. An important indication comes from Fig.3.28(f) showing the tracking efficiency of the Stanford device when tilted by 10° with respect to the beam. The map appears completely uniform and the efficiency becomes almost 100%. The same behavior was obtained for FBK devices tilted by 10° [101].

Because of the geometry of 3D detectors, the magnetic field has little effect on the charge collection mechanism and charge sharing among pixels. The average ToT distribution for FBK, Stanford and a planar reference sensor are reported in Fig.3.29 for both magnet on and off conditions. For 3D detectors there is a maximum ToT value at zero degrees due to the fact that charge sharing in this condition is minimum. The charge collection slightly decreases with the tilt angle but is then fully recovered for large tilts

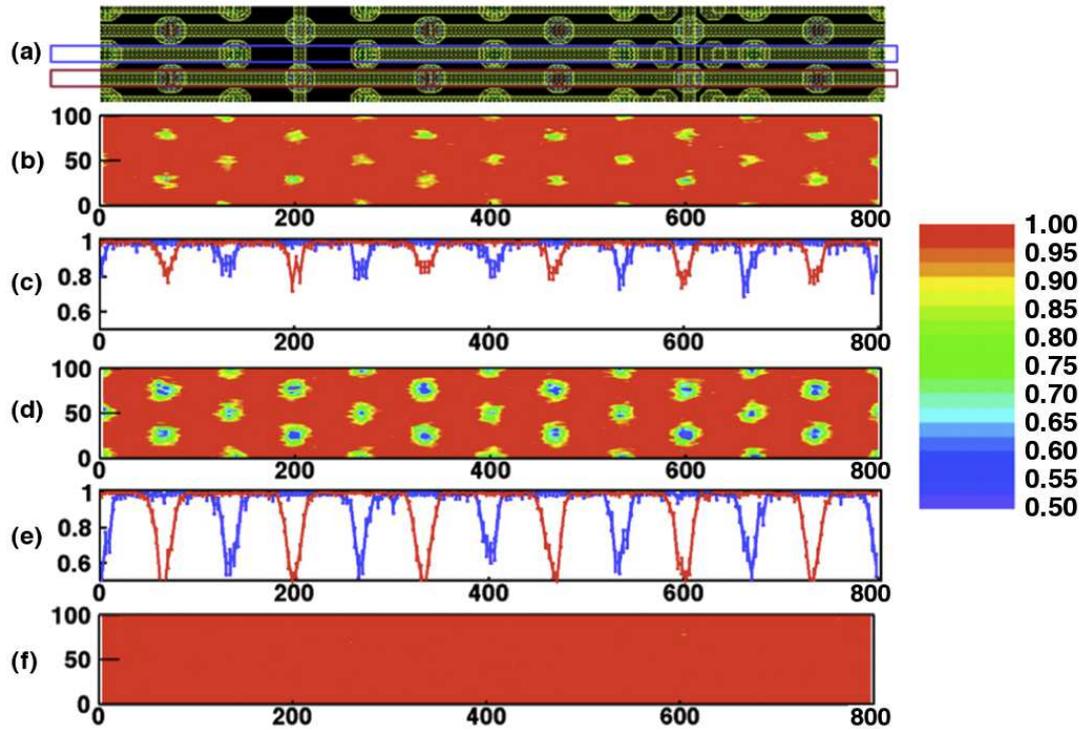


Figure 3.28: Tracking efficiency of an FBK pixel detector compared to a Stanford one. The layout of the scanned area (a) is reported for comparison. The 2D efficiency map (b) and the extracted 1D profiles (c) for the FBK sensor are compared to the same results for the Stanford device in (d) and (e) respectively. The recovered tracking efficiency for the Stanford device with a tilt angle of 10° is shown in (f) [98].

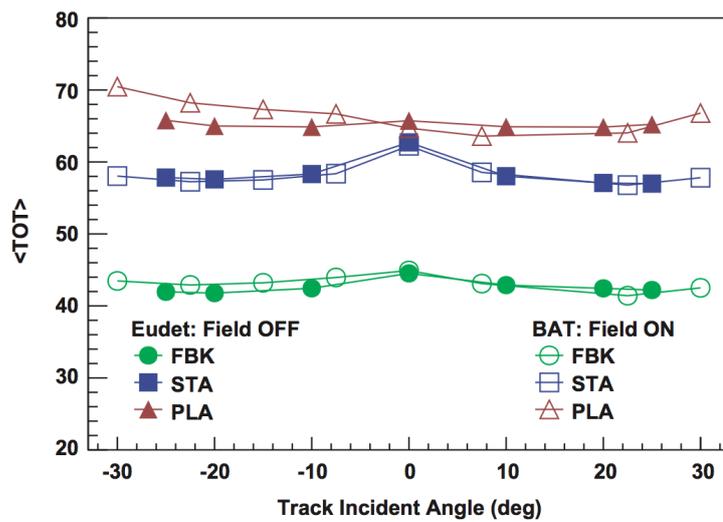


Figure 3.29: Average ToT distribution as a function of the incident angle for an FBK, a Stanford and reference planar device [98].

because of the longer particle path inside the device. The FBK device appears to collect less charge because, it was biased at 8V, which were sufficient to reach lateral depletion but not full depletion, causing the charge generated in the lower part of the device to be lost. However, as shown in Fig.3.28, this does not affect the tracking efficiency which remains quite high also in non perfect operating conditions.

The charge sharing probability as a function of the particle hit position along the short pixel edge was also investigate. It is normally defined as the number of tracks with more than one hit over the total number of tracks: $N_{tracks(>1hit)}/N_{tracks(tot)}$. Results are reported in Fig.3.30 for a hit angle of zero degrees, again comparing the same three devices. The charge sharing clearly occurs mainly in the boundary regions between two adjacent pixels. The lowest charge sharing probability was found for the Stanford device having fully passing through electrodes, while the highest charge sharing probability was measured for the planar reference device. The FBK sensor placed exactly in the middle because junction column depths were not optimized, causing the electric field distribution to deviate from the ideal condition resulting in an intermediate behavior between the planar and the full 3D detector.

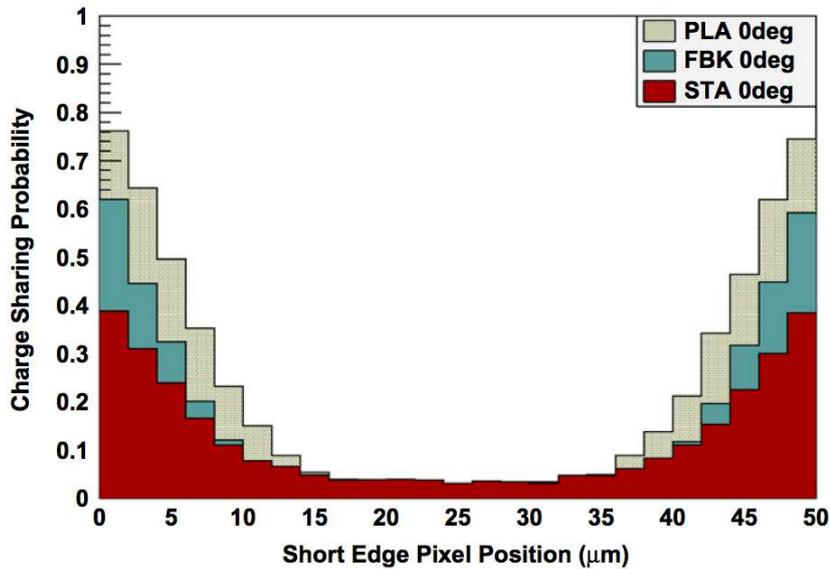


Figure 3.30: Charge sharing probability as a function of the track position along the short edge of the pixel for an FBK, a Stanford and reference planar device [98]

These results were very encouraging, proving that 3D devices might be good candidates for the upgrades of the pixel tracking layers at LHC experiments, since they perform best with high hit angles and suffer little effects from the presence of the magnetic field, conditions that are typically found in the inner layer of both ATLAS and CMS experiments

Table 3.5: Summary of irradiated DTC-2 devices. Device type, radiation fluence, type of particle used, and irradiation facility are reported. [102]

Module ID	Sensor type	Fluence (n_{eq}/cm^2)	Particle	Facility
A	2E	1×10^{15}	25 Mev proton	KIT
B	3E	1×10^{15}	25 Mev proton	KIT
C	4E	1×10^{15}	25 Mev proton	KIT
D	2E	2×10^{15}	24 GeV proton	CERN PS
E	4E	2×10^{15}	24 GeV proton	CERN PS

(see Chapter 1).

In order to prove that 3D detectors are also radiation hard, a total of five FBK DTC-2 devices were irradiated with 25 MeV protons at KIT up to fluences of $1 \times 10^{15} n_{eq}/\text{cm}^2$ and with 24 GeV protons at CERN PS up to fluences of $2 \times 10^{15} n_{eq}/\text{cm}^2$. Sensor type and received fluence are reported in Tab.3.5.

These devices were then electrically and functionally tested in laboratory with gamma and beta sources [102]. Measured leakage currents, shown in Fig.3.31, showed a large increase proportional to the received fluence as explained in Chapter 2 subsection 2.5.2. In particular, two different current levels were observed, one ($\sim 25 \mu\text{A}$) relative to devices irradiated at $1 \times 10^{15} n_{eq}/\text{cm}^2$ and the other ($\sim 35\text{-}40 \mu\text{A}$) relative to devices irradiated at $2 \times 10^{15} n_{eq}/\text{cm}^2$. Extracted damage constants, $\alpha \approx 5 \times 10^{-17} \text{ A/cm}$, were found to be in good agreement with the accepted theoretical value of $\alpha \approx 4 \times 10^{-17} \text{ A/cm}$ [49].

Breakdown voltages before irradiation were between 60 and 70 V while after irradiation most devices showed an increase of at least 10 V reaching, in most cases, operating voltages above 100 V. Only one sensor did not show the expected breakdown voltage improvement probably due to fabrication induced defects. The tuning of the irradiated assemblies was performed with the same target values as before irradiation (20 ToT at 20 ke⁻ and a threshold of 3200 e⁻) using a bias voltage sufficient to fully depleted the device (when permitted from the breakdown voltage). The tuning was successful for all the assemblies and threshold and noise values are reported in Tab.3.6. The noise does not show an increase with respect to pre-irradiation values because, although the leakage current is higher, the operating temperature of -20 °C is strongly mitigating its effects. Lower noise was observed for assemblies irradiated at higher fluences. This effect is to be attributed mainly to the electronics and not the sensor because of the different particles used in the irradiation: the Total Ionizing Dose (TID) estimated for 25 MeV protons, was equal to 144 Mrad, much higher than the 94 Mrad estimated for 24 GeV protons. Given that the FE-I3 chip was designed to sustain a maximum of about 50 Mrad, the higher TID could cause a larger degradation in noise performance for assemblies irradiated at

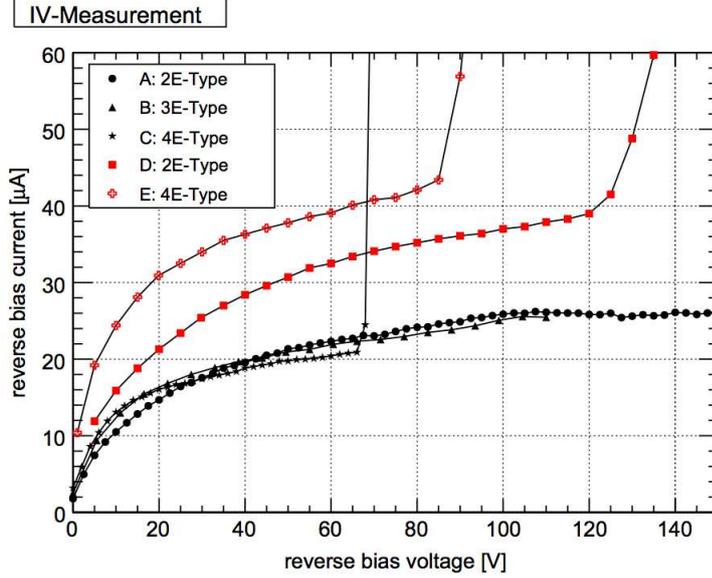


Figure 3.31: Leakage currents for the FBK pixel devices irradiated at two different fluences, 1×10^{15} (black) and 2×10^{15} n_{eq}/cm^2 (red) [102].

Table 3.6: Threshold and noise for the considered irradiated assemblies [102].

Module ID	Sensor type	Threshold [e^-]	Noise [e^-]	V_{test} [V]
A	2E	3261 ± 73	204.1 ± 11.6	120
B	3E	3158 ± 140	233.2 ± 13.4	100
C	4E	3267 ± 78	232.4 ± 12.7	60
D	2E	2950 ± 206	119.4 ± 31.5	125
E	4E	3307 ± 115	189.6 ± 19.0	80

1×10^{15} n_{eq}/cm^2 with 25 MeV protons.

The functional measurements with ^{241}Am gamma source were performed using the self-triggering capabilities of the system and were carried out only on assemblies irradiated at KIT up to 1×10^{15} n_{eq}/cm^2 (assemblies A, B, C in Tab.3.5). Mean collected charges (for the 59 keV peak) as a function of bias voltage are shown in Fig.3.32(a). Sensors in 3E and 4E configurations collect about 14.5 ke^- at the maximum bias voltage, essentially the same value observed before irradiation (see Fig.3.26(a)) while the 2E sample shows a decrease, collecting only about 12.8 ke^- . This effect is understood and is related to the larger inter-electrode distance of the 2E sample, which requires higher operating voltages for the sensor to be fully efficient, and is more affected by charge trapping due to the longer drift distances.

The results of source scans performed with the ^{90}Sr beta source for all the sensors

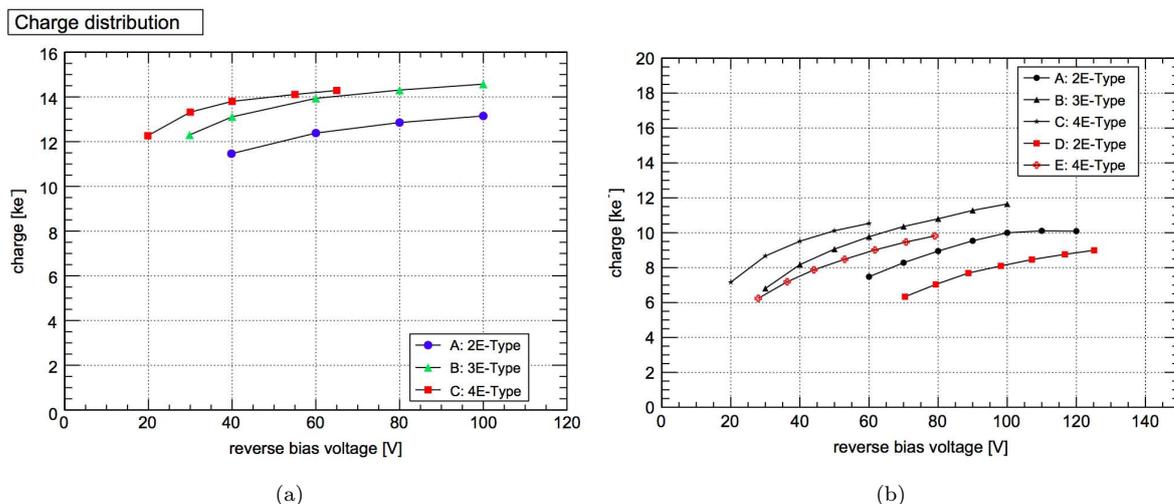


Figure 3.32: Collected charge as a function of bias voltage in response to an ^{241}Am source for the three sensors irradiated at $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ (a) and evolution of the MPV as a function of the bias voltage in response to a ^{90}Sr source for all the irradiated devices [102].

are reported in Fig.3.32(b). The figure shows the evolution of the MPV of the collected spectrum with respect to the applied bias voltage. Maximum collected charge before irradiation was about 15 ke^- , while values are considerably lower after, never exceeding 12 ke^- . The loss in collected charge is considerably larger for beta particles than for gamma rays. This is a direct consequence of how radiation interacts with silicon: in the case of gamma rays absorbed in the column overlap region, where the field is maximum, the charge generated will most likely be completely collected every time, only gamma rays absorbed in low field regions or non depleted regions will be lost. On the contrary, beta particles cross the entire device releasing charge all along their track and, if part or all the track crosses inefficient regions of the device, charge will be lost due either to trapping or to ballistic deficit. In particular, at the maximum operating voltages, the considered devices are not sufficient to fully deplete the bulk under the junction electrode tips, resulting in loss of charge. This is also confirmed by the fact that the curves in Fig.3.32(b) do not show a clear saturation for any of the devices. The trend of collected charge with respect to inter-electrode distance and radiation fluence is respected, meaning that devices irradiated at $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ show higher collected charge than devices irradiated at $2 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ and, among same fluence devices, those with shorter inter-electrode distance return higher collected charge for lower biases.

To gain a better insight into device behavior, numerical TCAD simulations were performed with the aid of the Synopsys TCAD tools [90]. Because of the peculiar geometry of the considered devices, simulations must be performed in 3D thus drastically increasing

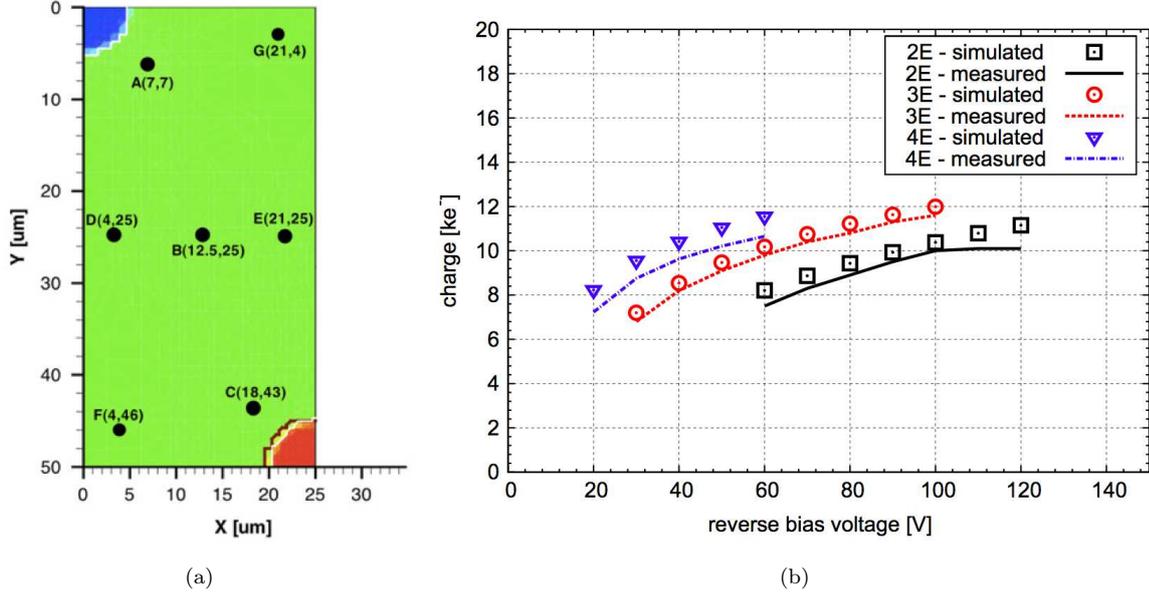


Figure 3.33: TCAD simulations of the three pixel devices irradiated at $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$. Bi-dimensional slice of the simulated structure extracted from the electrode overlap region and MIP hit positions (a) and simulation results compared to measured data (b) are shown [102].

the computational time. For this reason only one radiation fluence was investigated for all pixel geometries: $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$. The simulated structure reproduces only a part of the pixel including a quarter of columnar electrode per type and features a $200 \mu\text{m}$ thick silicon bulk. The columnar electrode depths are those shown in Tab.3.3 (DTC-2). An example for a 4E device is shown in Fig.3.33(a). Different MIP hit positions were considered (black dots in Fig.3.33(a)) and the total collection efficiency was averaged on all the points, in order to take into account both high efficiency and low efficiency regions inside the device, obtaining the simulated cluster size 1 (CS1) collected charge. Since measurements indicate that 80% of the events are CS1 and 20% are CS2, the charge sharing was also considered in the final simulated result (see reference [102] for more details on the simulation procedure). Simulation results are compared with measured values in Fig.3.33(b) showing very good agreement both in terms of absolute values and in terms of trend with bias. By extracting electric field distribution, recombination and electron and hole trapping from the simulated device, is possible to better understand the charge collection mechanism. It was demonstrated that, as suspected, the bottom part of the device, under the non optimized junction columns, was not efficient in collecting the charge due to the non sufficient applied bias. In fact most of the charge generated in this region recombines or gets trapped and is, therefore, not collected. The reader is invited to refer to reference [102] for the complete description and analysis of simulated results.

Table 3.7: Hit efficiency and charge sharing probability for the two irradiated sensors and an un-irradiated as a function of the impinging track angle for a bias voltage of 80 V [103].

Sensor type	Particle type	Fluence [n_{eq}/cm^2]	Hit efficiency [%]		Charge sharing [%]	
			$\phi=0^\circ$	$\phi=15^\circ$	$\phi=0^\circ$	$\phi=15^\circ$
3E	Protons	1×10^{15}	99.0	99.9	9.2	54.2
3E	Neutrons	1×10^{15}	97.6	98.1	7.0	25.2
3E	-	un-irrad.	98.8	99.9	12.2	62.1

Tracking capabilities after irradiation were evaluated during a test beam in June 2010 [103]. For this particular test two FBK devices were setup: both 3E, but one irradiated with protons at KIT at a fluence of $1 \times 10^{15} n_{eq}/cm^2$ and the other irradiated with neutrons at the Jozef Stefan Institute (JSI), Ljubljana, Slovenia, at the same fluence. Tests were performed in the H6 beam line at the CERN SPS North Area, with a 120 GeV/c pion beam using the EUDET telescope [100]. Devices under test were cooled down to $-20^\circ C$ in order to mitigate the radiation damage effects, and were biased at 80 V, the highest voltage before the onset of breakdown effects. Tracking efficiency results are reported in Fig.3.34 for both devices. The tracking efficiency for the proton irradiated sensor at 0° in Fig.3.34(b), shows a small efficiency loss in presence of the junction electrodes (almost negligible) and a larger one in presence of the ohmic electrodes, as already observed in previous test. This is also confirmed from the 1D profiles extracted from the measurements crossing a row of readout electrodes (red) and a row of bias electrodes (blue) (Fig.3.34(c)). When the device is tilted by 15° with respect to the beam, the efficiency is almost completely recovered (Fig.3.34(d)). Larger efficiency losses are observable for the neutron irradiated devices (Fig.3.34(e),(f) and (g)), and only the efficiency around readout electrodes is fully recovered by tilting the sensor. This is most likely caused by the higher introduction rate of stable acceptor of neutrons with respect to protons [104], causing the 80 V of bias to be not sufficient for the neutron irradiated device to be fully operative. The charge sharing among neighboring pixels was also investigated and found more probable in the boundary regions of the pixels as already observed pre-irradiation [98]. A summary of tracking efficiency and charge sharing is given in Tab.3.7 for both sensors and two different tilt angles.

Mean cluster charge and mean cluster size for the proton and neutron irradiated devices are reported in Tab.3.8 for two different tilt angles and are compared with the results for an un-irradiated FBK device. The first indication is that the proton irradiated device doesn't show charge collection losses after irradiation for both considered tilt angles,

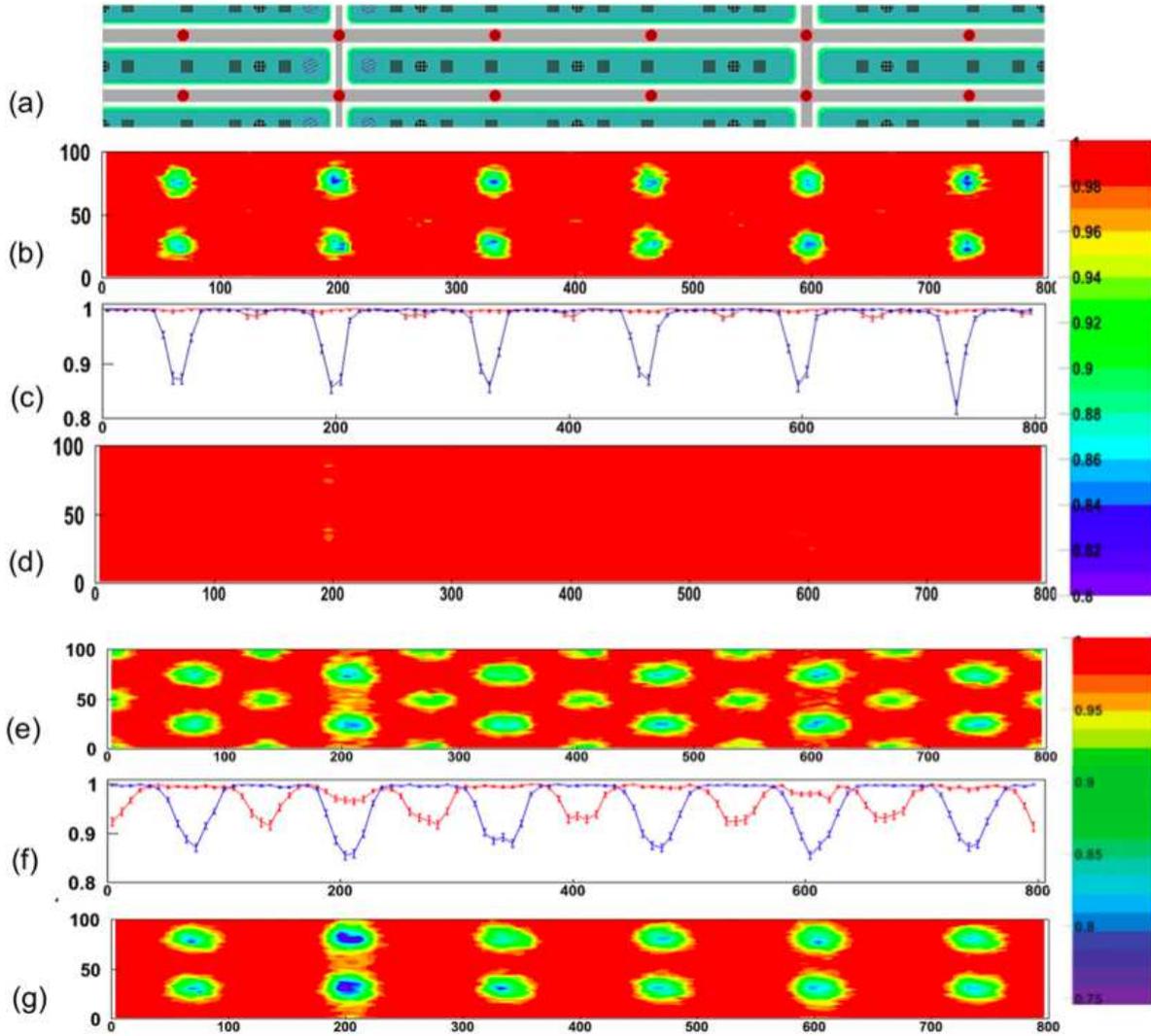


Figure 3.34: 2D map of the tracking efficiency for both the proton and the neutron irradiated devices compared to the layout of the considered region. The efficiency map of the proton irradiated device at a 0° tilt is reported in (a) and the related 1D profiles along ohmic (blue) and junction electrodes (red) are shown in (b) and compared with the 2D map for a 15° tilt (c). The same results for the proton irradiated device are also reported: 2D map at 0° (e), corresponding 1D profiles (f) and 2D map at 15° (g). The applied bias voltage was 80 V [103].

Table 3.8: Mean cluster charge and mean cluster size for the two irradiated samples with respect to an un-irradiated one at 80 V of bias [103].

Sensor type	Particle type	Fluence [n_{eq}/cm^2]	Mean cluster charge [ke^-]		Mean cluster size [%]	
			$\phi=0^\circ$	$\phi=15^\circ$	$\phi=0^\circ$	$\phi=15^\circ$
3E	Protons	1×10^{15}	16.210	15.560	1.14	1.60
3E	Neutrons	1×10^{15}	13.010	12.560	1.11	1.30
3E	-	un-irrad.	16.400	15.980	1.19	1.41

while the neutron irradiated devices shows a strong reduction (about 20%) probably caused by the different damage induced by neutrons. The mean cluster charge reduction for neutron irradiated devices is in good agreement with the measured efficiency loss. The means cluster size is coherent with the measured charge sharing.

An example of cluster charge and charge sharing distributions for both irradiated devices is reported in Fig.3.35, proton irradiated in the top row (Fig.3.35(a) and (b)) and neutron irradiated in the bottom row (Fig.3.35(c) and (d)). The MPV value of the Landau distribution is considerably lower for the neutron irradiated device and is possible to notice how the tilt angle increases the charge sharing. Further comments are available in [103].

3.5 3D-DDTC at CNM, most relevant results

In parallel with fabrication and testing performed at FBK, a similar technology was being developed independently at CNM, Barcelona, Spain. The first reported results were relevant to DDTC devices fabricated on 300 μm thick n-type substrates with a column depth of 250 μm . Preliminary electrical test showed low depletion voltages (a few volts), leakage currents in the order of ~ 1 pA/column and breakdown voltages higher than 60 V [86, 105]. Tests performed with an X-ray tube confirmed the low depletion voltage by observing the saturation of the collected charge, returning a lateral depletion equal to ~ 2 V and a full depletion of ~ 9 V [106]. The initial functional characterization was performed on Medipix2 pixel sensors with a monochromatic 15 keV X-ray beam at Diamond Light Source, Didcot, UK [107], and showed good detection efficiency and charge sharing lower than the planar reference device.

Pre-irradiation tests were performed on p-in-n, 300 μm thick, strip detectors with 80 μm pitch, in the H2 beam line at CERN SPS [108] using fast readout electronics designed for the CMS strip detector (AVP25 chip [23]). Collected charge was found to be lower than expected (20-30% less) and this was attributed to a shorter columnar electrode

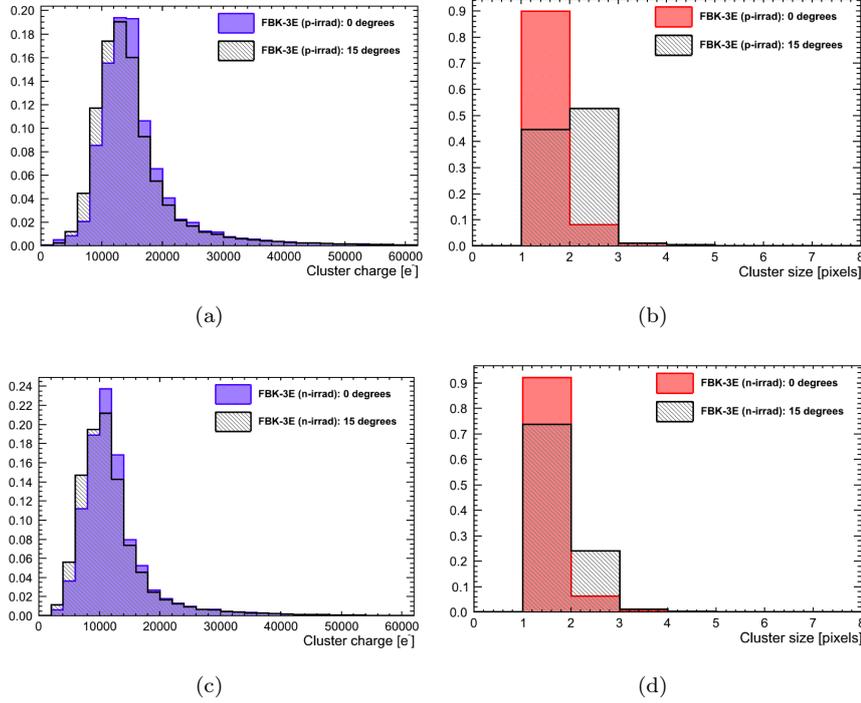


Figure 3.35: Landau distributions and cluster size plots for the proton irradiated device (a,b) and for the neutron irradiated device (c,d). The applied bias voltage was equal to 80 V [103].

depth. Charge saturation was observed at voltages larger than the expected full depletion because, at very fast shaping times, larger electric field are required to fully saturate the carrier velocity. Good uniformity was found on a single cell map of area $100 \times 100 \mu\text{m}^2$, apart from where the columnar electrodes are located. As expected, less charge sharing was detected with respect to a standard planar device and the spatial resolution was found to be better than the theoretical expectation. The total efficiency with a 1 fC threshold was measured to be $97.6 \pm 0.2\%$ for orthogonal beam incidence.

Functional characterization of irradiated strip sensors was performed in laboratory by means of laser scans and beta source measurements using the ALIBAVA readout system [109]. Both n-in-p and p-in-n detectors were investigated up to fluences of 2×10^{15} and $2 \times 10^{16} \text{ n}_{eq}/\text{cm}^2$. Liquid Nitrogen was used too cool the sensors and mitigate radiation damage effects. The n-in-p device irradiated at the lower fluence, showed lower charge collection than pre-irradiation up to about 150 V, when the onset of charge multiplication effects led to collected charges higher than pre-irradiation. The n-in-p sensor irradiated at the highest fluence, showed a rather low charge collection (about 30% less than pre irradiation) up to the maximum voltage of 425 V. The p-in-n sensors showed a similar behavior but the charge multiplication effect was less evident.

Laser scans showed lower efficiency in the regions around columnar electrodes, as expected, and confirmed the good charge collection efficiency also at extremely high radiation fluences.

With an optimized column depth with respect to FBK technology, CNM detectors further confirmed that 3D-DDTC technology is suitable for the upgrades of the LHC experiments and delivers high tracking efficiency also in very harsh environments.

3.5.1 Final consideration on the 3D-DDTC technology

The 3D-DDTC technology proved to be able to deliver very good tracking capabilities both in pre and post irradiation conditions. Performances are comparable with those of full 3D detectors, provided that the columnar electrode depth is well controlled and the tips of both column types are within $25 \mu\text{m}$ from the opposite wafer surface. Despite the more complex fabrication process, the great advantages of 3D over planar sensors are: (i) the possibility of operating at considerably lower voltages thus greatly reducing the power dissipation, (ii) the reduced carrier drift length, which results in lower trapping probability after irradiation, (iii) the small charge sharing, (iv) the negligible effects of magnetic field and particle hit angle on device operation.

For what concerns FBK devices in particular, unfortunately, due to the non optimized junction column depth, their radiation hardness was partially compromised at fluences exceeding $1\text{-}2 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$. The radiation hardness with optimized column depths was proven by CNM's devices, showing a reduction in collected charge of just 30% after being irradiated at a fluence of $2 \times 10^{16} \text{ n}_{eq}/\text{cm}^2$.

The DRIE process at FBK, was calibrated and tested several times and, as will be explained in Chapter 4, the column depth control is now very precise. In fact, latest technologies implement passing-through or "almost" passing-through electrodes.

For both FBK and CNM it is crucial to demonstrate the reproducibility of the fabrication process in order to allow for a medium volume production in reasonable times.

The first planned upgrade of the ATLAS experiment is the insertion of an additional pixel layer, the Insertable B-Layer (IBL), very close to the beam pipe. This will require extremely radiation-hard silicon sensors due the very large radiation fluence close to the interaction point. A description of the IBL and the most important sensor requirements will be addressed in the next chapter also including all the new development of 3D technology.

Chapter 4

The ATLAS IBL and 3D detectors fabricated at FBK

The current ATLAS pixel tracker is composed by 3 layers of n-in-n pixel sensors as previously described in Chapter 1 subsection 1.3.2. The ATLAS collaboration is planning to install an additional pixel layer during the long shut down of 2013-2014. This new pixel layer will be inserted between the current B-Layer and a new smaller beam pipe and is known as *Insertable B-Layer (IBL)* [110, 111]. The IBL will be placed very close to the interaction point and will sustain a very large amount of radiation during its operation. For this reason, several R&D activities were triggered in the past years, with the main objective of finding new and more radiation tolerant technologies to be used in the IBL and in the future upgrades. This chapter will describe the motivations and requirements of the IBL, and the main choices that were made in terms of electronics and sensor architectures. The main focus will then be moved to the 3D-DDTC technology specifically developed at FBK to meet the very stringent IBL requirements.

4.1 The ATLAS Insertable B-Layer (IBL)

In order to realize the full physics capabilities of the ATLAS experiment, it is essential to ensure the correct tracking of charge particles and an efficient b tagging also after the foreseen increase in luminosity. The current pixel detector is working very well but its performances will degrade with the increase of the accumulated radiation dose because silicon sensor and readout electronics will start to suffer the effects of radiation damage.

The installation of a properly designed pixel layer closer to the beam pipe, will ensure the proper operation of the tracker as the LHC goes toward full luminosity and beyond. The following subsection will cover the motivations and requirements of the IBL from the point of view of readout electronics and silicon sensors.

4.1.1 Motivations and summary of requirements

The full analysis of the motivations for the IBL would require a much deeper physics analysis that is not object of this work. The main motivations for the IBL are anyway summarized here.

The first motivation for the installation of an additional pixel layer in the ATLAS experiment comes from performance considerations on the current B-Layer. It is foreseen that, with the increasing machine luminosity and radiation damage, irreparable failure of modules will occur in the entire tracker. Although the data loss in the external layers can be partially recovered during the reconstruction, the performance of the B-Layer will affect the entire efficiency of the tracker. The redundancy provided by the IBL will assure full tracking efficiency and b tagging even after complete failure of the B-Layer.

The current pixel detector is designed for a peak luminosity of $1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, limit that will be exceeded in the next years in the High-Luminosity LHC (HL-LHC). The increased luminosity will cause a large number of event pileups leading to a high occupancy that will translate in readout inefficiencies (e.g. fake tracks). The IBL will have a relatively low occupancy and will preserve the tracking performances also with the foreseen luminosity increase. Moreover, being very close to the interaction point, the IBL will provide better quality of the impact parameters reconstruction for the tracks.

The current beam pipe would be very hard to replace in case of a vacuum failure because it was inserted in the pixel detector and installed together with it. The installation of the IBL will require to reverse this situation in order to install a smaller radius beryllium beam pipe. The needed tooling and set of operations are considered part of the IBL project. The extraction process is currently being tested on an installation mock-up.

Although the current operation of the LHC is not posing many concerns from the point of view of the accumulated dose, this problem will become more evident as the years pass. For this reason, the IBL will be a good driving force in the study and development on new radiation-hard technologies in many field such as electronics, sensors and material engineering for the new support structure and services.

The main requirements the IBL imposes on electronics and sensors will be described in more detail in the following.

4.1.2 Layout

The radial free space between the B-Layer and the current beam pipe is equal to 8.5 mm and is visible in Fig.4.1(a). By reducing the beam pipe radius by 4 mm it will be possible to fit the IBL in the resulting 12.5 mm free space as shown in Fig.4.1(b).

The layout of the IBL in the r - ϕ plane is sketched in Fig.4.2 while the most important

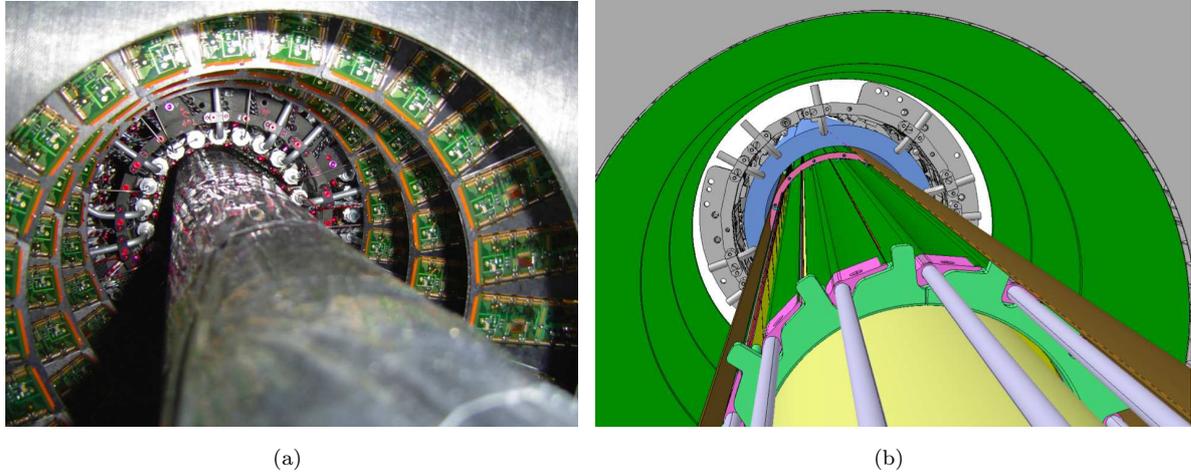


Figure 4.1: Picture of the current pixel inner layer with the inserted beam pipe (a) and rendering of the IBL insertion with the reduced radius beam pipe (b) [110].

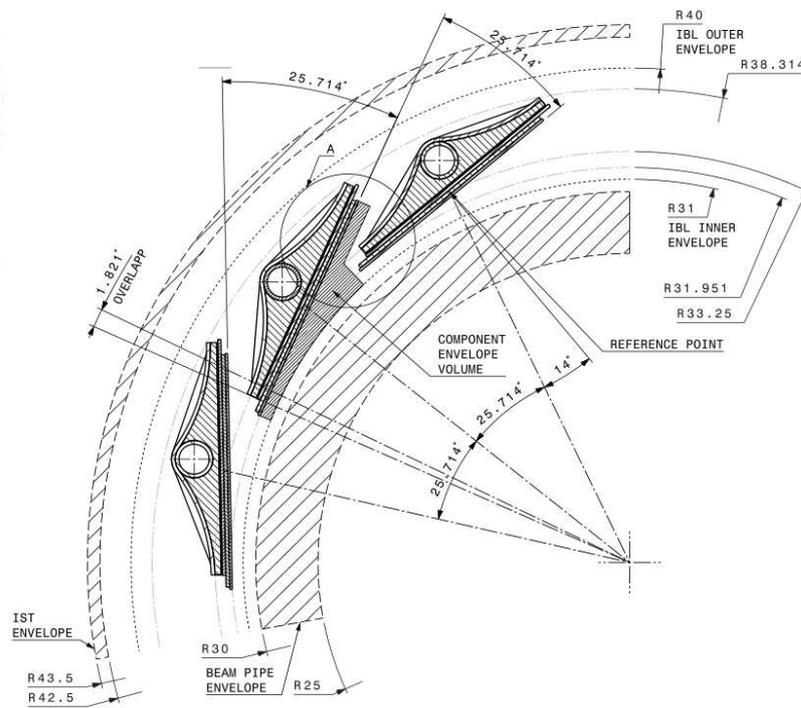


Figure 4.2: Layout of the Insertable B-Layer on the r - ϕ view [110].

Table 4.1: Most important layout parameters of the ATLAS IBL [110].

Parameter	Value	unit
Number of staves	14	-
Number of modules per stave (single/double chip)	32/16	-
Pixel size (ϕ, z)	50, 250	μm
Module active size W \times L (single/double chip)	16.8 \times 20.4/40.8	mm^2
Coverage in η , no vertex spread	$ \eta < 3.0$	-
Coverage in η , 2σ (=112 mm) vertex spread	$ \eta < 2.58$	-
Active z extent	330.15	mm
Geometrical acceptance in z (min,max)	97.4, 98.8	%
Stave tilt angle in ϕ (center of sensor, min, max)	14.00, -0.23, 27.77	degree
Overlap in ϕ	1.82	degree
Center of the sensor radius	33.25	mm
Sensor thickness (planar/3D silicon)	200/230 \pm 15	μm
Radiation length at $z=0$	1.54	% of X_0

layout parameters are reported in Tab.4.1. In order to guarantee a full coverage in ϕ for high p_T tracks, 14 staves are needed. The space constrains force the stave tilt angle in the radial direction to be in the range between 0 and 27° . Full geometrical coverage in the beam (or z) direction is not possible because there is no room to tilt and partially overlap the sensors. The gap between the modules can anyhow be minimized using active or slim-edge sensors, as will be explained later. The center of the sensor will be 33.25 mm away from the interaction point. In order to increase the tracking precision, the pixel size along the z direction was reduced from the current 400 μm to 250 μm leaving the other pixel dimension fixed to 50 μm . Depending on single or double chip module assemblies, the modules will have a width of 16.8 mm and a length of either 20.4 or 40.8 mm. Many of these parameters also affect the stave layout as will be shown in a later subsection.

4.1.3 Modules

The performance requirements for the IBL modules come mainly from considerations on detectors and electronics. A summary of the basic requirements is reported in Tab.4.2.

At beginning of July 2011, after several months of sensor and electronics testing, the sensor review panel gave the recommendation of investigating a "mixed scenario" in which, double chip planar sensors will be installed in the central part of the IBL, while 3D single chip modules will populate the highest η regions, in order to benefit from the peculiar electrode orientation in terms of better z -resolution after heavy irradiation [111]. The choice between double or single chip modules, is related to the different yields of the planar

Table 4.2: Basic performance requirements for the IBL modules. (*) After full dose; SEU stands for Single Event Upset [110].

Parameter	Value	Conditions
NIEL dose tolerance	$5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$	-
Ionizing dose tolerance	250 Mrad	-
SEU rate at peak luminosity*	$< 1/(24 \text{ hrs})$	For global configuration
Hit efficiency in active-area*	$> 97\%$	Single MIP
r- ϕ MIP resolution*	$< 10 \mu\text{m}$	2 T B-field, 15° incidence
z MIP resolution*	$72 \mu\text{m}$	Digital resolution for $250 \mu\text{m}$ pixel
Hit loss at peak luminosity	$< 1\%$	Including SEU effects
As-built bad pixels	$< 0.2\%$	Sensor + Bump + Chip defects
Maximum bias voltage	1000 V	-
Radiation thickness	$< 500 \mu\text{m}$	-

and 3D fabrication processes. The standard planar process is in fact well established and able to deliver double chip sensors with relatively high yields, while the 3D process is more complex and producing single chips will provide a more reliable yield. The two types of modules will be geometrically compatible. The bare module assemblies are dressed by gluing a flex hybrid circuit [112] on the sensor side; two similar circuits are available for single or double chip assemblies (Fig.4.3). The module flex comes with a pigtail and a test connector that are cut away before the stave loading. The stave flex wing is glued onto the module flex and connections are provided by means of wire bonding. The design of the module flex was performed taking in mind a few special precautions:

- The back of the flex (glued to the sensor) uses a $25 \mu\text{m}$ thick polyimide film based overlay, which is rated to stand $100 \text{ V}/\mu\text{m}$ and is required in order to operate planar sensor at the maximum operating voltage of 1000 V after full radiation dose. Even if not completely necessary because of the much lower bias, the same material is also used for 3D detector modules.
- The high voltage capacitors are encapsulated using an isolating resin.

Additional detail on the IBL modules can be found in [111].

Electronics, the FE-I4 readout chip

The front-end chip currently used in the ATLAS pixel detector (FE-I3 [10]) does not meet the IBL requirements for two reasons: not sufficient hit rate capabilities and radiation hardness and too small active fraction of the footprint to build a compact layer high with geometric acceptance. For this reason, a brand new chip was designed: the FE-I4 [113].

The FE-I4 is designed in a 130 nm feature size bulk CMOS process and with a

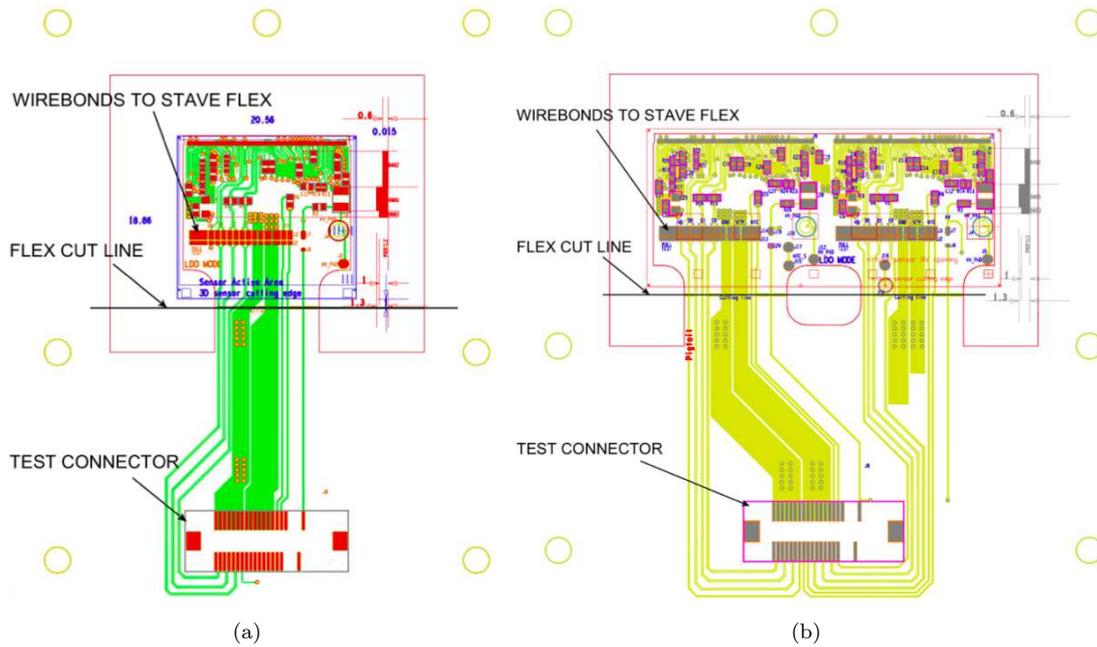


Figure 4.3: Module Flex Hybrids for single (a) and double (b) chip module. The two modules are electrically compatible [111].

pixel size of $250 \times 50 \mu\text{m}^2$, matching the IBL requirements. The smaller feature size presents several advantages: the increased circuit density allows for higher complexity to be implemented in spite of the reduced pixel area, resulting in a readout architecture able to cope with much higher hit rates. Moreover, the 130 nm CMOS process is inherently more radiation hard and, in fact, the chip is rated for a 250 Mrad Total Ionizing Radiation (TID) dose.

The most important innovation introduced with this new IC is the completely re-designed pixel matrix architecture: the storage is now made locally at the pixel level until triggering and the subsequent propagation of the trigger inside the pixel array. Physics based simulations have shown that this approach should be able to cope with the expected high hit rate for luminosities up to $3 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ at the IBL radius [114, 115].

The radiation hardness of the 130 nm CMOS process is a direct consequences of many of its intrinsic features. The gate-oxide thickness of about 2 nm reduces the total amount of positive charge trapped in the oxide resulting in lower threshold shifts after irradiation and lower damage induced leakage gate currents. Specific hardening techniques, such as enclosed layout transistors, are no longer necessary for all digital and some analog transistors. It must be stressed that processes with smaller feature sizes are not intrinsically more resistant to Single Event Upset (SEU) so care must be taken during the layout phase.

The FE-I4 readout chip is based on analog sections interleaved with digital sections

Table 4.3: Main specifications of the FE-I4 readout chip [113].

Parameter	Value	Unit (note)
Number of pixels	$80 \times 336 = 26880$	(column \times row)
Pixel unit size	250×50	μm^2 (direction $z \times r\phi$)
Last bump to physical edge on bottom	≤ 2.0	mm
Nominal analog supply voltage	1.4	V
Nominal digital supply voltage	1.2	V
Nominal analog current	12	μA
Nominal digital current	6	μA
DC leakage current tolerance per pixel	100	nA
Normal pixel input capacitance range	0-500	fF
Edge pixel input capacitance range	0-750	fF
Hit trigger association resolution	25	ns
Single channel ENC	< 300	e^-
In-time threshold within 20 ns (400 fF)	≤ 4000	e^- (at discriminator output)
Tuned threshold dispersion	< 100	e^-
Charge to Digital coding method	ToT	(on 4 bits)
Radiation tolerance (specs met at dose)	250	Mrad
Operating temperature	-40 to +60	$^\circ\text{C}$
Readout initiation	Trigger	
Maximum number of consecutive triggers	16	(internal multiplication)
Minimal time between external triggers	125	ns
Maximum trigger latency	6.4	μs
Maximum sustained trigger rate	200	kHz
I/O signals	custom LVDS	
Nominal clock input frequency (with 20% margin)	40	MHz
Nominal serial command input rate	40	Mb/s
Output data encoding	8-10	bits
Nominal data output rate	160 (up to 320)	Mb/s

and is realized using standard synthesized cells, allowing to exploit the full power of modern CAD tools. The digital logic is synthesized from a high level description language (Verilog). The decoupling of digital and analog substrates, in order to avoid degradation of the noise in the most sensitive analog sections, is performed by means of a deep n-well, available in the 130 nm CMOS process.

The main specifications of the FE-I4 readout chip are reported in Tab.4.3. The total number of pixels is equal to 26880, arranged in a matrix of 80 (in the beam or z direction) by 336 (in the azimuthal or $r\phi$ direction), with a single pixel size of $250 \times 50 \mu\text{m}^2$. The

size constrain in the $r-\phi$ direction was set by the well established bump-bonding pitch available at the assembly factories, while the other size was set in order to fit the entire new digital architecture also taking into consideration power and clock routing. The total size of a diced FE-I4 chip is equal to $18.8 \times 20.2 \text{ mm}^2$, making it the largest readout chip ever produced for high energy physics experiments. A size comparison with the FE-I3 chip can be seen in Fig.4.4. Thanks to its dimensions, the new readout will increase active

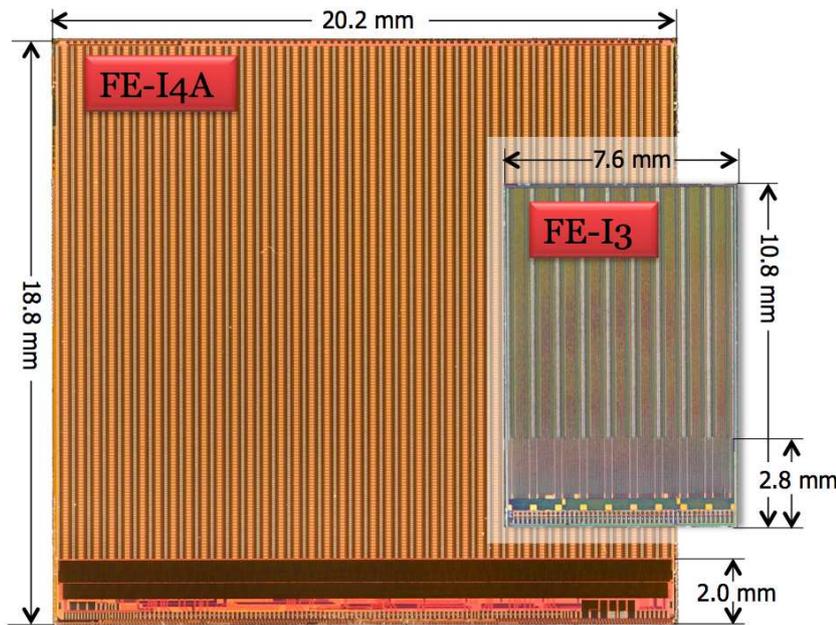


Figure 4.4: Comparison of the size of the FE-I4 chip with the one of the FE-I3 chip [113].

over total area ratio, also easing the module and stave assemblies while reducing to total material budget. Moreover, a larger chip also helps in reducing the overall cost required for the bump-bonding, greatly decreasing the amount of chips to be handled. Such a large IC chip can only be produced if a solid power distribution can be established and a satisfactory yield achieved.

The organization of the readout chip is shown in Fig.4.5. Each pixel consists of an independent analog section with continuous reset that amplifies the charge collected by the sensor. The hits are discriminated in the analog section by means of a comparator with a tunable threshold and the charge is converted to Time over Threshold (ToT) with a proportionality factor that the user can adjust by changing the return to baseline behavior of the pixel. A sketch of the analog section of the front-end is reported in Fig.4.6. It is composed by a 2-stages amplifier optimized for low power, low noise and fast rise time, followed by a discriminator. The analog section covers roughly 60% of the pixel area. The first amplification stage is a regulated cascode with a triple-well n-MOS input transistor.

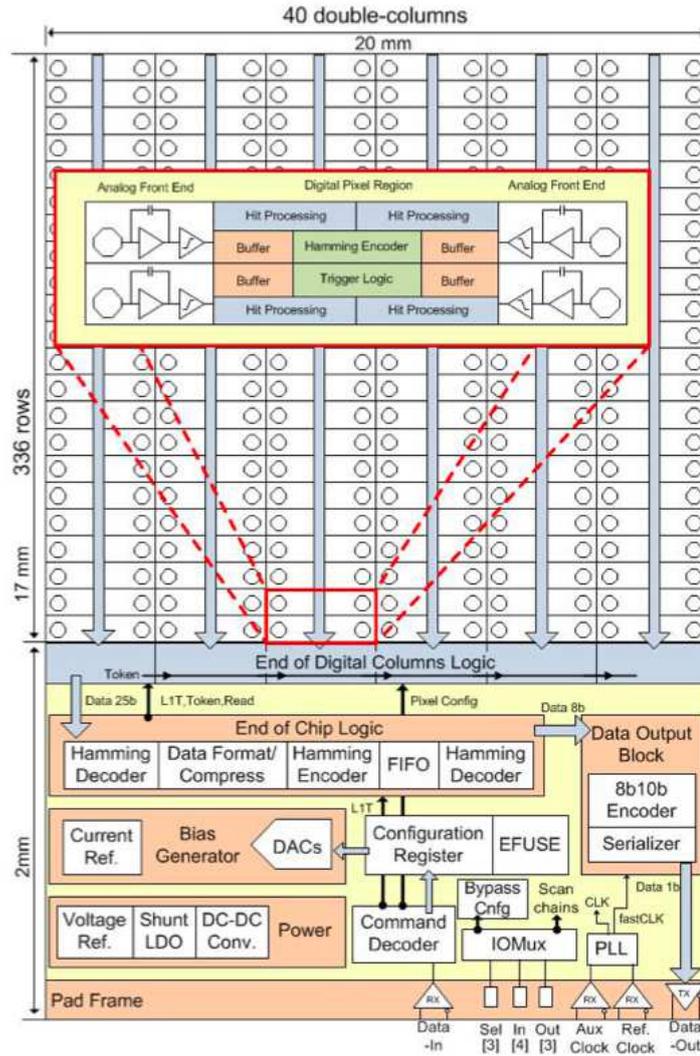


Figure 4.5: Sketch of the organization of the FE-I4 chip architecture [113].

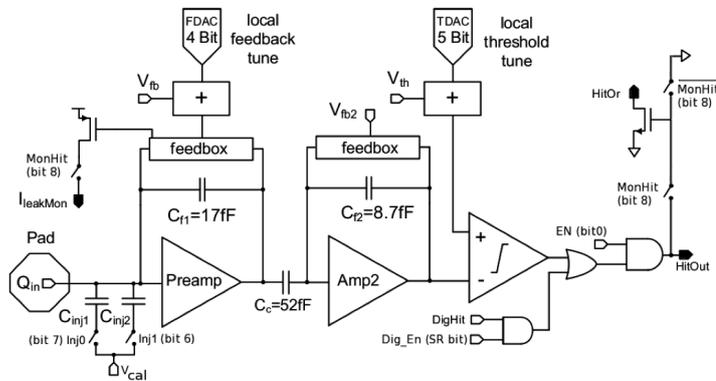


Figure 4.6: Analog section of a single pixel inside the FE-I4 readout chip [113].

The preamplifier uses a continuous current reset that gives an approximately linear ToT signal. The sensor leakage current is compensated by means of an active slow differential pair that can tolerate a maximum DC current of ~ 100 nA. The second amplification stage is AC coupled to the first and is implemented using a folded cascode configuration with a p-MOS input transistor. Besides eliminating possible DC shifts that can cause a pixel-to-pixel threshold mismatch, the AC coupling provides an additional gain factor coming from the ratio of the second stage feedback capacitor over the coupling capacitor (≈ 6). This allows to increase the feedback capacitor of the first stage with advantages in terms of charge collection efficiency, signal rise time and power consumption without affecting the noise and without degrading the signal amplitude at the discriminator input. Finally, the discriminator is realized using a classic two stage architecture.

For test and calibration purposes, it is possible to inject a test charge at the preamplifier input through a set of two injection capacitor. Hits can also be injected at the discriminator input to independently test the digital part of the pixel. The tuning of each single pixel can be stored in 13 dedicated bits: 2 bits control the injection switches, 4 bits set the local feedback current of the first stage (and so also the charge to ToT conversion), 5 bits are used to save the value of the discriminator threshold and one bit sets the MonHit output (leakage current output) and the HitOR output (global OR of all pixels). The last remaining bit is used for the masking of the pixel in case problems are detected.

The entire pixel array is organized in columns of analog pixels that are tied together in couples sharing the same digital double-column unit, centered between them. Inside the columns, four analog pixels communicate to a single *4-pixel digital region* (4-PDR). The communication is organized inside each double-column and controlled with peripheral logic.

Owing to the smaller feature size, the digital architecture was improved with respect to the FE-I3 chip and is now expected to withstand much higher hit rates. The trigger is propagated inside the array and the hits are stored locally until the triggering occurs or they need to be erased. Five buffers are available to store the ToT information for each analog pixel during the trigger latency. In the previously mentioned 4-PDR digital block, the 4 different discriminator outputs are fed to 4 separate hit processing units that provide time-stamping and ToT computation. It is also possible to add an additional discrimination level that can distinguish between small and large hits.

This architectural implementation offers the following advantages: (i) it allows for resource sharing between the pixels of a 4-PDR, (ii) the resource sharing helps in reducing power consumption together with the fact that un-triggered hits are not transferred to the chip periphery, (iii) is efficient in terms of time-walk compensation and finally (iv) it improves the active fraction of the FE-I4 since the memory is located at pixel level.

The schematic blocks of the chip periphery are shown in Fig.4.5. The following operations are implemented: communication and tuning of the IC, organization of the data read back, and fast data output serialization. Further testing capabilities, such as redundant memories and a low multi-purpose multiplexer, are also provided. The communication with the FE-I4 is performed by means of two LVDS inputs: the clock (nominally 40 MHz) and the command input Data-in (40 Mb/s). The command stream is decoded on chip into local pixel configuration, global configuration and trigger commands without the need for a separate module control chip, thus further reducing the total IBL mass. The decoded pixel configuration is sent to the pixels for storage inside the 13 local registers bits of each pixel. A total of 32 16-bit deep registers are available for the global tuning of the chip operation. Some DACs in the bias generator section convert the stored configuration values to the voltages and currents needed to tune the various sections of the chip. The decoded trigger is propagated to the "End of Chip Logic" block where the readout is initiated. When a hit is confirmed by the coincidence of a trigger with a latency counter reaching its latency inside a 4-PDR, the data stored in the 4-PDR ToT buffers is sent to the periphery and associated to the bunch-crossing corresponding to a specific trigger. The data is then re-formatted, coded, serialized at 160 Mb/s and sent outside of the chip from the Data-Output block.

In order to test bare FE-I4 chips and assembled pixel modules, a portable USB data acquisition system was designed: the USBpix [116]. The USBpix is a modular test system, developed for lab measurements with both FE-I3 and FE-I4 chips. The USB connection is provided by a micro controller mounted on a Multi-IO board which also includes an FPGA and a 2 MB memory. The Multi-IO is connected to an adapter card specific for the type of readout chip to be used, either FE-I3 or FE-I4. All the required LVDS signals are provided by the adapter card. The FE-I4 adapter card allows to route all the power and signal lines to the chip using a flat cable, or to connect them separately via an RJ45 connector chip.

The electrical and functional characterization of the FE-I4 chip was performed on wafer and with the USBpix system on both bare chip and bump-bonded assemblies. The power consumption of the analog section has mainly two contributions, from the biasing of the pre-amplifier and the discriminator and has a typical value of $16 \mu\text{W}/\text{pixel}$ ($11 \mu\text{A}$). The digital power consumption is the sum of a static contribution and a contribution directly dependent on the hit rate, and was found to be equal to $7 \mu\text{W}/\text{pixel}$ ($6 \mu\text{A}$). By multiplying both components by the number of pixels and by summing them, the total power consumption of the chip results roughly $160 \text{ mW}/\text{cm}^2$.

The measured threshold and noise are strictly related to the operating parameters of the chip and, in particular, on the global threshold value, the global feedback current and

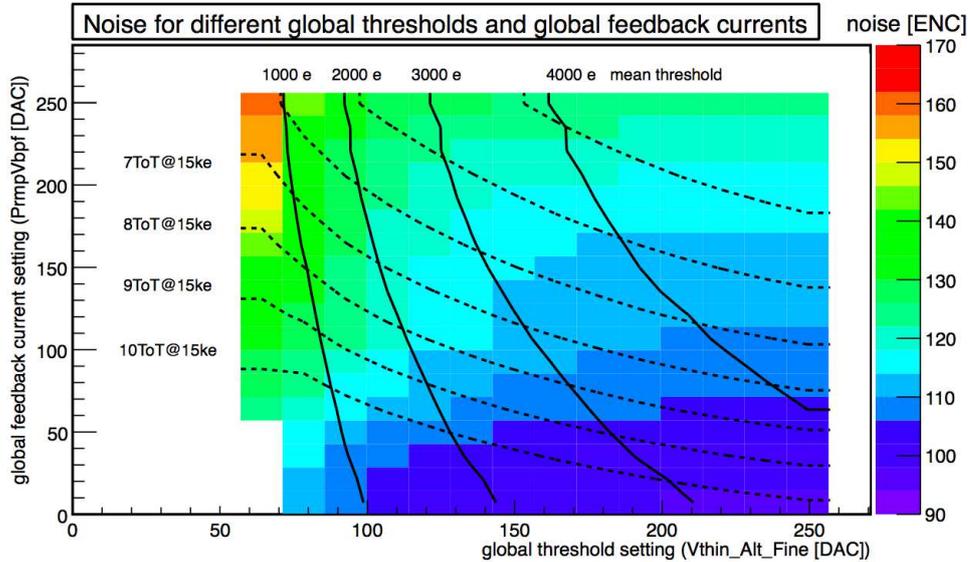


Figure 4.7: Dependence of the ENC on the global threshold settings and the global feedback current for a typical FE-I4 chip. The solid lines are representative of the mean threshold extracted using a gaussian fit, the dashed lines show the mean ToT distribution in response to an input charge of 15 ke^- [113].

the analog work point of the pre-amplifier. The measured ENC as a function of global threshold and feedback current value is shown in Fig.4.7. The bare IC shows a noise in the range of 110-120 electrons for a set threshold of 3000 e^- , while a chip bump-bonded to a sensor in typical operating conditions exhibits an ENC of about 150 electrons. The noise generally increases with reduced thresholds and larger feedback currents. The threshold dispersion inside the entire chip is about $30\text{-}40 \text{ e}^-$.

The radiation tolerance of the IC was tested by exposing some chips to different TIDs of 6, 75, and 200 Mrad in an 800 MeV proton beam at the Los Alamos Laboratory. The total threshold dispersion was found to remain unchanged after irradiation, and the noise increased by 15-25% in comparison to pre-irradiation values.

The on-wafer chip selection was performed in laboratory and was based on several selection criteria including: the analog and digital power taken by the ICs in different configuration states, global configuration scans, local pixel configuration scans, the analog and digital pixel maps and the threshold and noise pixel maps. The wafer yield, measured on a sample of 21 wafers, was found to be 70% on average.

Chosen sensor technologies

As already mentioned, sensors for the IBL were realized in the framework of the ATLAS Upgrade Planar Pixel Sensor and 3D Sensor R&D collaborations [117, 118]. Two different

detector architectures were used: standard n-in-n planar (double chip) and n-in-p 3D (single chip) . From layout and module requirements (Tab.4.1 and Tab.4.2) sensor specific requirements can be extracted:

- The impossibility of titling the modules in the beam direction results in the need for inactive edge width lower than $450\ \mu\text{m}$ for double chip sensors and lower than $225\ \mu\text{m}$ for single chip sensors. This will translate in a geometric efficiency of about 97.5%.
- In order to reduce the material budget the sensor thickness must be between 150 and $250\ \mu\text{m}$. This will also allow charge collection in planar sensors to be more efficient at very large radiation fluences.
- The power dissipation is required to be lower than $200\ \text{mW}/\text{cm}^2$ at $V_{bias}=-1000\ \text{V}$.
- The maximum leakage current the FE-I4 can compensate is $100\ \text{nA}/\text{pixel}$. The sensors must be designed in order not to overcome this value at the maximum expected fluence.
- The sensor operating temperature is $-15\ ^\circ\text{C}$ or higher at $<200\ \text{mW}/\text{cm}^2$.
- The in-time hit efficiency is requested to be greater than 97% after a benchmark fluence of $5 \times 10^{15}\ \text{n}_{eq}/\text{cm}^2$ at bias voltage lower than $1000\ \text{V}$.

The baseline IBL planar sensor is an n-in-n detector [113] and is fabricated at CiS, Erfurt, Germany. The devices were produced on n-type, FZ silicon sensors with $\langle 111 \rangle$ crystal orientation and a bulk resistivity of $2\text{-}5\ \text{k}\Omega\text{cm}$ thinned to a thickness of $200\ \mu\text{m}$. This specific thickness was chosen because of limitations imposed by the bump-bonding vendor in order to properly perform the bonding operation. All wafers were diffusion oxygenated for 24 hours at $1150\ ^\circ\text{C}$ after thinning. The segmented n^+ implantations are realized on the front side while a uniform p^+ implantation is placed on the back side together with 13 guard-rings used to gradually drop the applied high voltage toward the cut edge and extending over a $350\ \mu\text{m}$ area in order to meet IBL specifications. The adopted inter-pixel isolation is based on the moderated p-spray approach. This design is directly derived from the current ATLAS pixel sensors also fabricated at CiS [9].

Particular care was taken in the design of the edge termination aiming at the highest possible dead area reduction without affecting the efficiency of the edge pixels [119]. Edge pixels were designed to be $500\ \mu\text{m}$ long and to partially extend over the guard-ring region on the opposite wafer side by $250\ \mu\text{m}$, as shown in Fig.4.8 where the edge region of the current ATLAS pixel sensor is also report for comparison. The active area, defined by the 50 % hit efficiency, is required to be $200\ \mu\text{m}$ from the cutting edge (as shown in Fig.4.8(b)).

To ease the electrical characterization and on-wafer selection, and to avoid floating potential on pixels having an open bump connection, a punch-through network was implemented and connected to a metal bias grid [120]. The metal grid is then connected to a bias ring surrounding the entire active area. Outside the pixel matrix a uniform n^+

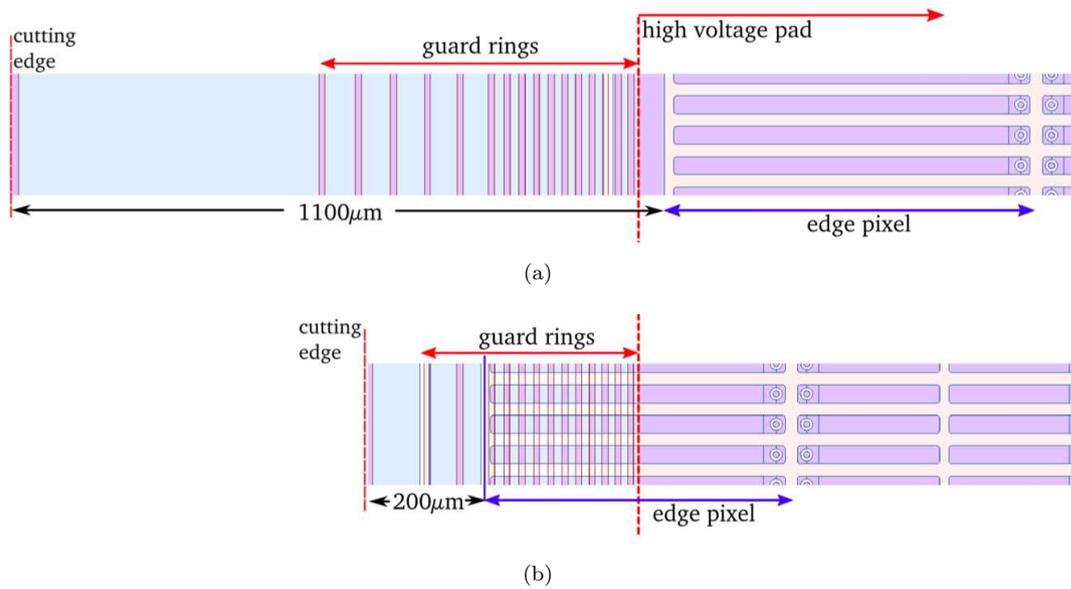


Figure 4.8: Comparison between the edge region of the current ATLAS pixel design (a) and the IBL planar sensor design (b) [111].

implantation is realized to ensure that the active area and the cutting line have the same potential.

Two different designs were implemented on the prototype wafers, a "slim-edge" one, as just described, and a "conservative" one in which the edge pixels were not extended above the guar-ring region. The two detector versions have comparable performance apart from the edge efficiency, where the conservative design showed the expected $450\ \mu\text{m}$ inactive edge. The "slim-edge" version was the choice for the final IBL production.

During the sensor qualification planar devices showed good performances both pre and after-irradiation, in agreement with the expectation and were therefore chosen to cover the central region of the IBL. Because this work is mostly related to 3D detectors the results obtained with planar detectors will not be discussed but can easily be found in literature [113].

The other technology of choice for the IBL is the 3D technology. 3D detectors have improved a lot in the past few years, especially in terms processing yield. They come in several different flavors but for reasons related to the fast track IBL schedule [111], only the so called 3D-DDTC technologies available both at FBK and CNM were investigated. Since the main focus of this thesis is on 3D detectors, all the information relative to 3D sensors for the IBL are given in sections 4.2 and 4.3. The two 3D technology of choice will be described and the main results discussed with particular attention to FBK devices that are the object of this work.

The bump-bonding and flip-chip

A key step to the assembly and integration of the IBL modules is the *flip-chip bump bonding*, connecting each pixel sensor to the corresponding FE-I4 chip. The bump bonding process has the following requirements [110]:

- bump pitch of 50 μm ;
- 80 bumps per mm^2 or 26880 bumps per readout IC;
- defect rate $<10^{-4}$;
- successful flip-chip using FE-I4 chips thinned down to less than 200 μm .

Due to the large size of the FE-I4 readout chip, the bump bonding becomes more complicated and its quality and reliability need to be properly assessed.

The present pixel detector was assembled using FE-I3 readout chip thinned down to 190 μm . This thickness assured a proper control of the chip bowing, keeping it within the bump height tolerance during the temperature change and solder reflow used in the process. Because of the large size of the FE-I4, the minimum thickness required to achieve the same bowing control would be about 400 μm which is not acceptable for the IBL specifications. The bonding process needs therefore to be modified including the use of a support wafer temporarily bonded to the thinned FE-I4 chips, which must be removed before the module assembly.

Two different bump bond technology were considered: indium and solder based (see Chapter 2 section 2.4). The first is based on evaporation of metal on both the sensor and the readout, followed by a thermo-compression step that will produce indium-indium interconnections. This method provides relatively weak mechanical strength. The second considered technology uses electroplating of eutectic solder on only one wafer, while the other one is treated with Under Bump Metallization (UBM). The interconnections are created by solder reflow at a temperature of about 250 $^{\circ}\text{C}$ to obtain lead-free solder. Solder bump technology is able to provide good reliability and smaller amount of defective bumps, while the indium based technology has an higher average number of defective connections that is also increasing during device operation. For this reason the baseline bump bonding technology for the IBL was chosen to be the solder based one (see Chapter 2 subsection 2.4.1).

The IBL solder flip-chip process consist of four main steps:

1. UBM treatment of the aluminum bump pads on both readout chip and sensor and deposition of bumps on the chip.
2. Readout chip wafer thinning to a target thickness of 200 μm or less and bonding of the thinned wafers on a carrier wafer, followed by the dicing of sensor, IC and carrier wafers.
3. Flip-chip assembly of the sensors and readout chips with micro-metric accuracy.

4. Removal of the carrier wafer from the flip-chipped assembly.

The first two steps of the process need to be performed on entire wafers but the flip-chip is normally performed on single dices. After the solder reflow no additional stress inducing steps are needed and the carrier wafer can be removed by laser exposure. The cooled down bump connections are rigid enough to maintain the assembly flat at the end of the process. Several tests were carried out and FE-I4 chips thinned down between 150 and 90 μm were successfully bump-bonded to dummy sensors [110]. As an example Fig.4.9 shows the cross-section picture of an assembly where the actual IC thickness was measured to be roughly 87 μm . The 50 μm pitch solder bumps are clearly recognizable and no signs of disconnected bumps are observed. These tests confirmed the reliability of the flip-chip process down to very low readout IC thicknesses.

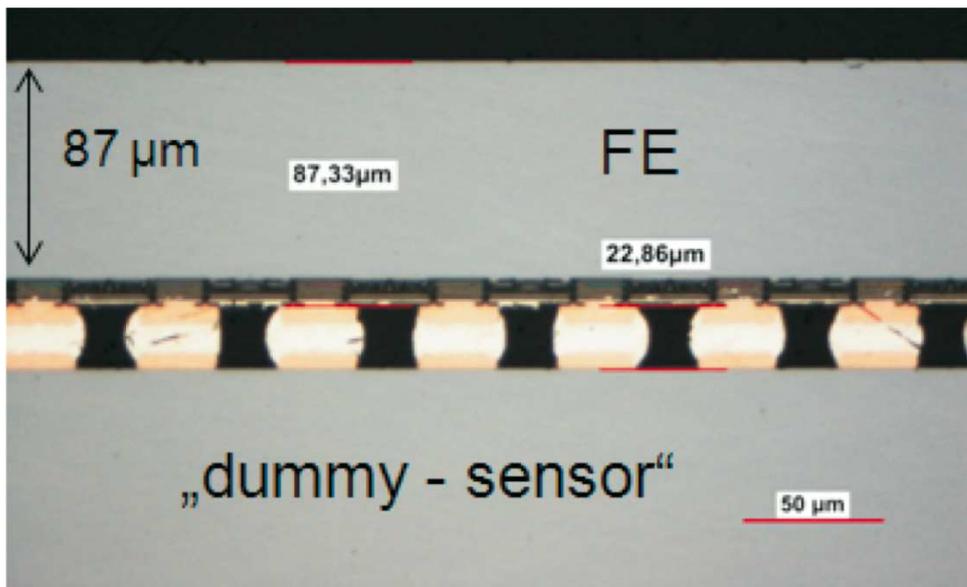


Figure 4.9: Cross-section of a bump-bonded and flip chipped assembly between a dummy sensor and an FE-I4 readout chip thinned down to about 87 μm . The space between the readout and the sensor is shown to be equal to 22.86 μm and the bump pitch is 50 μm [110].

The bump-bonding and flip-chip process needs to be fully compatible with the considered sensor technologies. For what concerns planar n-in-n sensors, the compatibility was already established during the assembly of the current ATLAS pixel detector, while for 3D it was assessed during the qualification phases and the yield of the process was found to be the same as for planar devices [113].

4.1.4 Stave layout and assembly

The stave layout in the mixed sensor scenario is reported in Fig.4.10 [111]. The area covered by double chip planar sensors corresponds to 75% (corresponding to 24 FE-I4 chips) in the center of the stave, while the area covered by single chip 3D sensor is the remaining 25% on either sides of the IBL (corresponding to 4 FE-I4 chips). The gap between modules is fixed and corresponds to $205 \mu\text{m}$.

As already mentioned, the thicknesses of the two sensor types are slightly different, $200 \mu\text{m}$ for planar and $230 \mu\text{m}$ for 3D. In addition, 3D sensors are $700 \mu\text{m}$ wider in $r-\phi$. The reason for this second difference comes from the fact that the 3D layout was arranged to be compatible also with the single sided 3D technology featuring the active-edge. In the full 3D technology the bias pad is on the same side of the sensor and must therefore be extended toward the outside. More details about the 3D sensor layout will be given in section 4.2. The extracted stave cross-sections for both a planar and a 3D modules are reported in Fig.4.11.

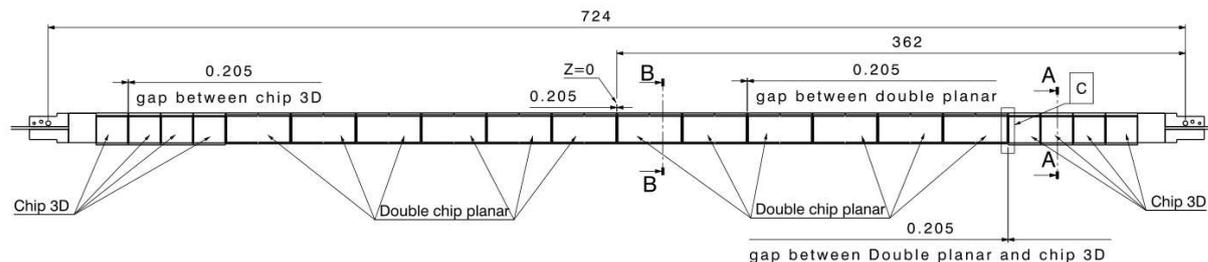


Figure 4.10: Stave layout for the mixed sensor scenario. The gap between the modules is fixed to $205 \mu\text{m}$. 3D detectors populate the two stave extremities [111].

Module loading on the stave

Each stave is mounted onto an holding frame before the modules loading and it remains on it until is integrated as a 7 m long object (stave + internal services) around the beam pipe in the IBL. The holding frame is made of carbon fiber reinforced plastic and will minimize the mechanical stress during handling and transportation. The thermal contact between modules and stave is guaranteed by a thermal grease which was previously qualified to meet the IBL radiation requirements. The module assembly to the stave is one of the most critical steps, it must be performed with great care and it is described in [111]. The procedure integrates the stave and stave-flex together with the planar and 3D detector modules, always aiming at the highest quality in terms of working pixels and modules and long term reliability. A total of 15 steps are necessary to load a module on the stave:

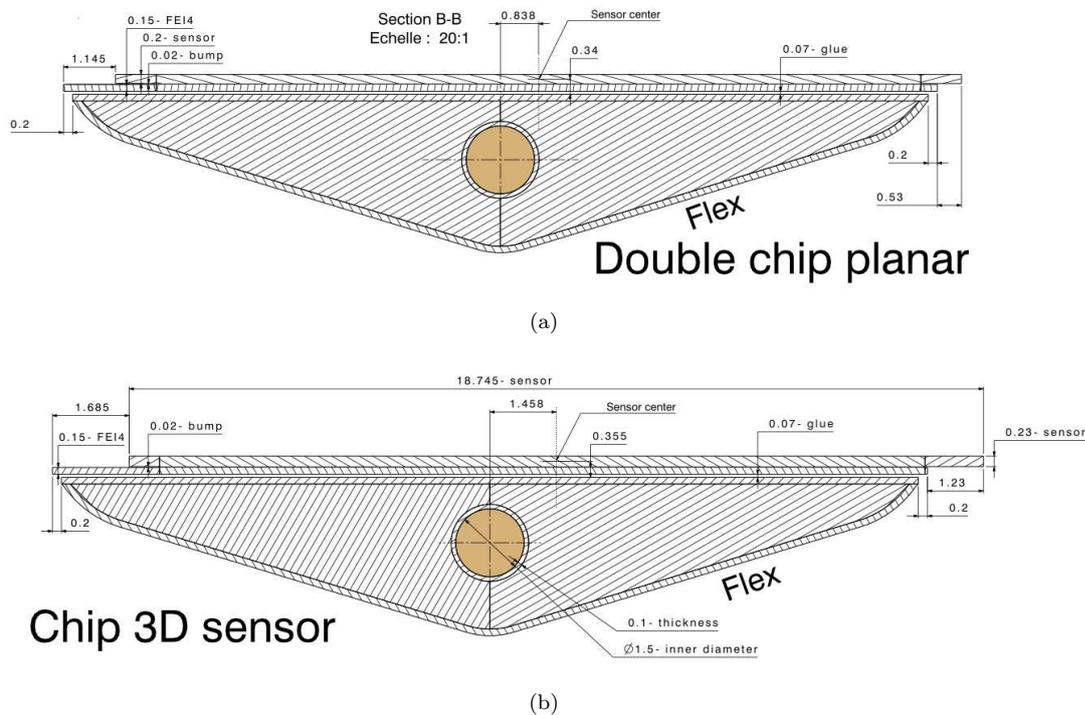


Figure 4.11: Stave cross-section extracted for two different z coordinates: across a planar module (a) and across a 3D module (b) [111].

1. The complete stave with the glued stave-flex is received at the loading site and is inspected as part of the Quality Assurance (QA) procedure. The stave is thermally cycled ten times from $-40\text{ }^{\circ}\text{C}$ to $+40\text{ }^{\circ}\text{C}$ to check that its geometry is conformal.
2. The assembled modules that passed the preliminary electrical tests are received at the loading site.
3. A "Guillotine tool" cuts away the module pigtail. The wire bonds used for test purposes are removed.
4. The first half of the stave is loaded. Six planar and four 3D detectors are accurately positioned on the stave using mechanical reference pins (dowel pins). The $205\text{ }\mu\text{m}$ gap between modules is fixed by polyimide-coated shims that have a thickness of $190\text{ }\mu\text{m}$.
5. The second half of the stave is loaded with the same technique.
6. The 32 flex-wings that were retracted during module loading are released and glued to the module flex using Araldite 2011 (epoxy glue).
7. The electrical connection between module-flex and stave-flex is performed by means of wire bonding. In order to assure redundancy, multiple wire bonds are used for each connection. The performed connections are related to FE-I4 power and I/O LVDS signals, sensor bias and connection to the NTC temperature sensors placed on the module flexes. The weight required to pull test bonds is used to assess the quality of

the bonding process.

8. The loaded stave is electrically connected to the readout system through an adapter card and is then cooled down using a CO₂ system. This will qualify the stave in near operating condition. Reworking is performed in case something went wrong during the loading.
9. The modules positions on the stave are double checked with respect to the stave reference.
10. The full stave is thermally cycled from -40 °C to +40 °C to detect assembly weaknesses and infant mortality and correct them.
11. After the thermal cycles the modules positions are double checked as in step 9. In case of displacement or distortion, rework is considered. These positions are recorded and used as initial conditions for the alignment of the modules in the completed IBL.
12. A complete functional test is performed with cooling and readout systems active. This test checks the integrity of all the modules and, in particular, bump integrity and pixel noise.
13. Adherence to the IBL envelope is checked. This is particularly critical with respect to the neighboring staves because only 0.8 mm of space will be available.
14. The last operation consists in adding an insulating spacer between module groups sharing the same sensor bias and a space to protect the wire bonds during the stave mounting in the IBL.
15. Finally, the stave is transported to CERN SR1 surface building for extensive QA test: burn-in, source scan and cosmic tests.

The electrical services of the staves are designed to be fully compatible with both considered sensor technologies. They will require to provide a maximum bias voltage of 1000 V in order to operate planar sensors after the maximum radiation fluence is reached.

3D and planar sensors will require rather different bias voltages after irradiation and for this reason they will need to be connected to separate HV supplies. As previously stated, two different flavors of 3D detectors will be mounted on the staves, FBK and CNM. They have very similar operating voltages but, for optimal control of the operational settings, each HV channel will only be connected to one type of 3D detectors.

During the qualification phase, planar and 3D detectors were found to have similar operating currents ($\sim 400 \mu\text{A}$) after the full dose of $5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ for a temperature of -15°C . The different range in bias voltage suggests to use different HV power supplies and for this reason different ISEG models were select, the only difference being in their maximum output voltage (500 V for 3D and 1000 V for planar sensors). The specific brand of power supplies was selected to maintain the full compatibility with the instruments already in use in the ATLAS detector.

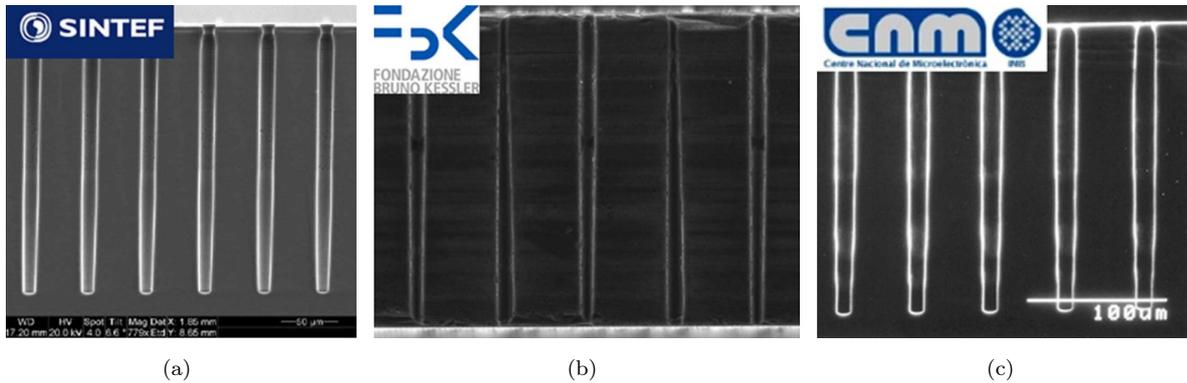


Figure 4.12: SEM micrograph of columns etched on test wafers from different fabrication facilities within the ATLAS 3D sensor collaboration: SINTEF (a), FBK (b) and CNM (c) [124].

4.2 The ATLAS 3D sensor collaboration

The *ATLAS 3D sensor collaboration* [121] was approved in 2007 with the aim to develop, test and industrialize 3D silicon sensors in different research institutes and processing facilities in Europe and USA [122]. The collaboration includes 18 institutions and 4 processing facilities: SNF (Stanford, California, USA), SINTEF (Oslo, Norway), CNM (Barcelona, Spain) and FBK (Trento, Italy). In addition VTT (Helsinki, Finland) later joined the collaboration as well.

The 3D sensor collaboration was initially put in place in order to perform accurate testing of the available 3D samples from the different processing facilities and to speed up the transition between the R&D phase and industrialization. The focus was later shifted to the design and production of 3D pixel detectors for the ATLAS IBL with the strategies described in the following subsection.

4.2.1 Processing options and manufacturers

The ATLAS 3D sensor collaboration joined efforts in 2009 to produce 3D pixel sensors compatible with the FE-I4 readout chip for the ATLAS IBL upgrade [123, 124]. The 3D technology available in the different fabrication facilities is well tested and established at least at the R&D level, as previously described in Chapter 3. The control of the etching procedures needed to fabricate the columnar electrodes is now very good and reproducible as shown in Fig.4.12. 3D sensors are typically fabricated on 4", FZ p-type silicon wafers.

Two architectural implementations of the 3D technology are available within the collaboration:

1. Full 3D detectors with active-edge: this technology was first developed at SNF and was later transferred to SINTEF in view of a medium volume production (see Chapter

3 sections 3.2). It features columnar electrodes penetrating the entire silicon bulk, etched from the front side, and ohmic trench at the edge also etched from the front side. Both the columns and the trenches are filled with polysilicon thus partially restoring the activity of the electrodes. This process makes use of the support wafer to keep all the pieces in place during fabrication but it requires additional steps for its removal.

2. 3D-DDTC with 200 μm slim edges: this approach to 3D technology is essentially a double-sided process with columns etched from opposite sides of the wafer, junction from the front and ohmic from the back. It was independently developed at FBK and CNM and its main features and results are described in Chapter 3 sections 3.4 and 3.5. It is very important to remark that FBK technology was specifically modified for the IBL qualification to have fully passing-through columns. All the details and results are given in section 4.3. Because of the double-sided nature of this approach, the active-edge is not feasible but a fence of ohmic columns was proven to be effective in reducing the dead area at the edges in order to meet IBL specifications.

Although the steps after columnar electrodes and trench etching are the same as for standard planar devices, 3D processes are intrinsically longer thus limiting the production capabilities of a single manufacturer. For this reason, the four processing facilities involved in the collaboration decided to combine efforts and expertise for the production of the required sensor volume for the IBL. After some years of successful technological evaluation (2007-2009, see Chapter 3), in June 2009 it was decided to go for a common wafer layout aiming at full mechanical compatibility while maintaining the different sensor flavors unaltered.

4.2.2 The common wafer layout

The 3D pixel sensor design for the IBL matches the geometrical dimensions of the previously described FE-I4 readout chip and it features $250 \times 50 \mu\text{m}^2$ pixels. Because the very large size of the FE-I4 poses concerns about fabrication yield, it was decided to design single chip sensor tiles. Previous tests on FE-I3 compatible pixel sensors both pre and after irradiation [73], suggested to implement a 2E pixel configuration (two n^+ electrodes per pixel) in order to obtain the optimal signal to noise ratio even after the maximum expected radiation dose. The same tests also suggested to use p-type substrates, to realize n-in-p sensors, in order to benefit from the higher electron mobility in silicon. A 230 μm sensor thickness was chosen aiming at a good trade-off between SNR and mechanical robustness of the wafers for double-sided processing. The full design specifications were defined to meet IBL requirements and are reported in Tab.4.4.

In order to assure full mechanical and electrical compatibility between the investigated

Table 4.4: Summary of the main IBL design specifications for 3D pixel detectors [124].

Parameter	Value	note
Sensor area	$20.56 \times 18.86 \text{ mm}^2$	including $80 \mu\text{m}$ scribe lines
Tile type	Single	-
Number of n^+ columns per pixel	2	2E configuration
Sensor thickness	$230 \pm 20 \mu\text{m}$	-
Column overlap	$\geq 200 \mu\text{m}$	-
Dead region on sides next to adjacent sensors	$200 \mu\text{m}$	+ scribe lines residuals
Pixel isolation technique	p-spray/p-stop	-

3D technologies some issues had to be addressed:

- a. *Sensor edges*: SNF/SINTEF detectors feature the full active-edge, whereas CNM and FBK sensors do not. Since IBL specifications require the edge extension in the beam (or z direction) to be roughly $200 \mu\text{m}$, active edges are not strictly necessary. For this reason it was decided to go for a slim-edge of $200 \mu\text{m}$ that could be achieved by all manufacturers. The edge terminations for each fabrication facility are reported in Fig.4.13. For the SNF/SINTEF case (Fig.4.13(a)) the edge pixel was increased in size to $375 \times 50 \mu\text{m}^2$, by adding an n^+ column. Outside this stretched pixel, the active-edge is present and the scribe line is placed on the outside, $200 \mu\text{m}$ from the last ohmic column of the active area. The edge termination in FBK and CNM technologies is slightly different. FBK implements a fence of ohmic columns (Fig.4.13(b)) that prevents the depletion region spreading from the last junction column to reach the cut line [125], while in CNM technology (Fig.4.13(c)) the edge is terminated by a guard-ring fence of junction columns able to sink the current generated from the cut region, surrounded by a double fence of ohmic columns. The reliability of the slim-edge was thoroughly investigated for FBK devices and will be covered in detail in the following sections.
- b. *Substrate bias*: in SNF/SINTEF devices the substrate bias needs to be supplied from a pad placed on the front side, the same side where bumps are deposited (the backside is not accessible because of the presence of the support wafer). Another option would be to perform a selective etching of the backside layer and then depositing a metal pad to perform the wire bonding, but these steps are not fully engineered yet. Instead, being FBK's and CNM's processes double-sided, the back side is accessible and the substrate bias can be provided by bringing a wire bond to a purposely designed bias tab. This makes double-sided 3D detectors electrically compatible with planar sensors. To provide the bias to SNF/SINTEF sensors from the front sides, the devices have to be extended on one side beyond the physical edge of the readout chip. The extension required to place a wire bond was estimated to be in the order of 1.5 mm and, in order

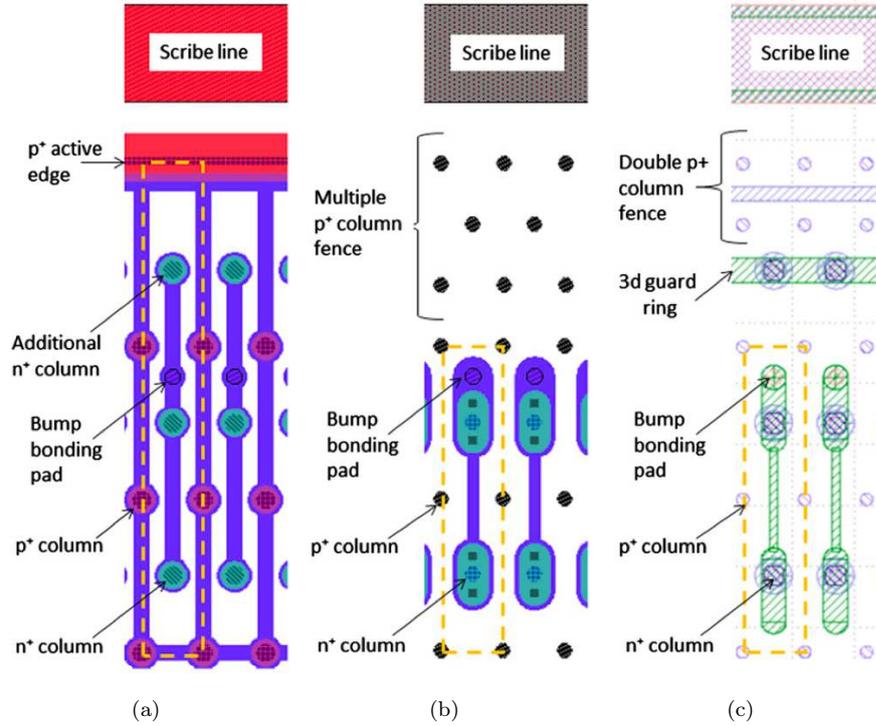


Figure 4.13: Layout of the slim-edge region of the three different designs: SINTEF (a), FBK (b) and CNM (c) [124].

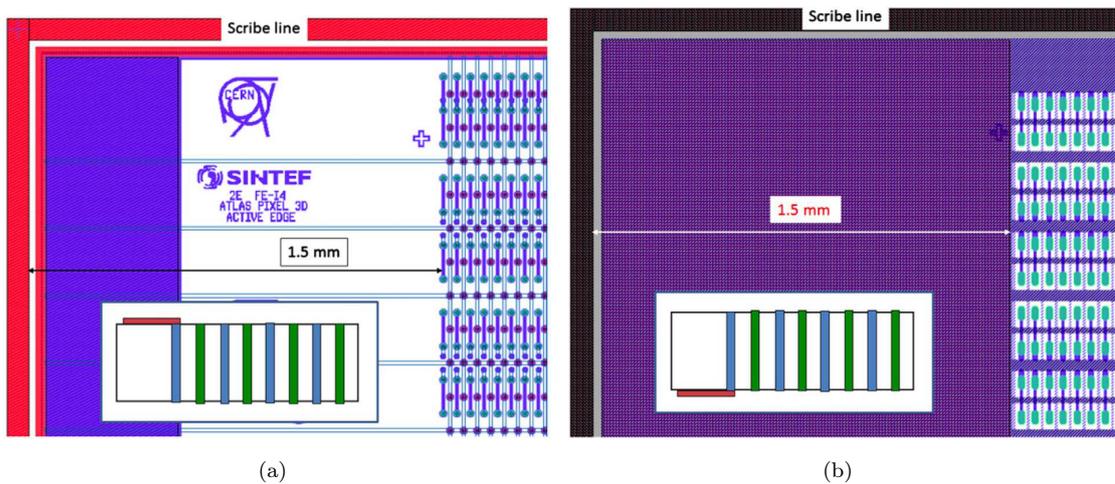


Figure 4.14: Layout details of the bias tab on sensor front side for the SNF/SINTEF technology (a) and on the back side for the FBK technology (b). The bias tab for CNM devices is equal to the FBK one [124].

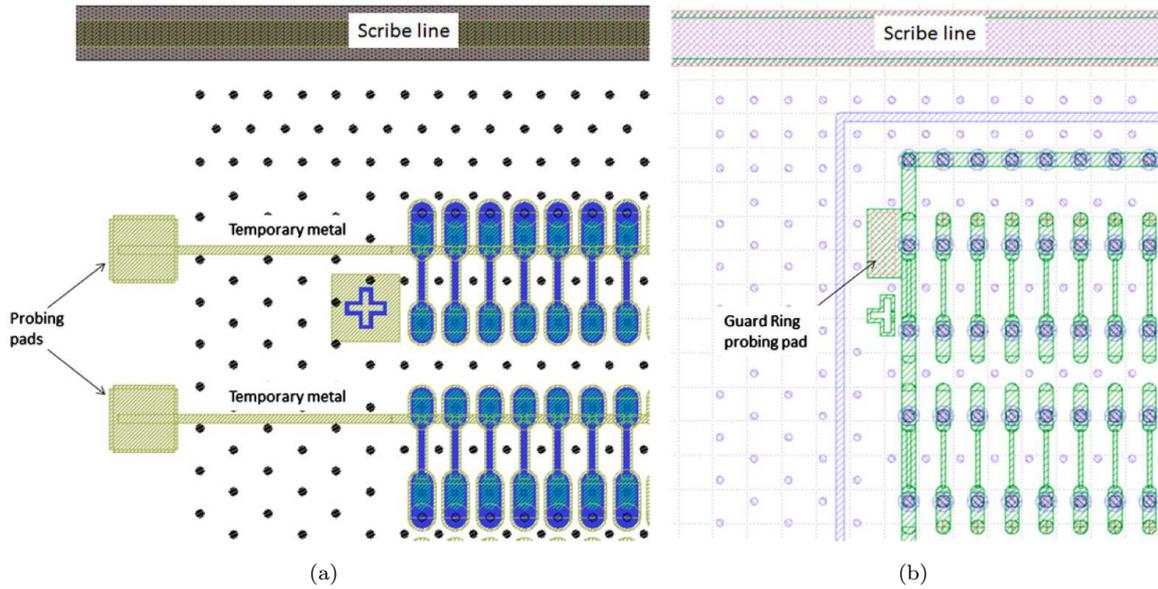


Figure 4.15: Layout of the on-wafer sensors selection structures for both FBK and CNM technologies: temporary metal current measurements for FBK (a) and guard-ring current measurements for CNM [124].

to maintain full compatibility, all 3D technologies were designed with the same bias tab extension. Fig.4.14 shows the comparison between the bias tab of an SNF/SINTEF device (on the front side) with the one of an FBK device (on the back side, the same was made for CNM devices). The extension of the sensor on one side, could be done because no slim-edge requirements were placed for the edge in the $r-\phi$ direction and, in fact, the edge opposite to the bias tab was designed to be $400\ \mu\text{m}$ wide.

- c. *On wafer electrical tests*: because of the high complexity and cost of the bump bonding process, it is essential to perform on-wafer discrimination between good and bad sensors. The punch through based test grid used for planar sensors (see subsection 4.1.3) is not compatible with SNF/SINTEF technology because of the absence of any n^+ implantation on the front surface. At the same time, although this technique might be compatible with detectors from both FBK and CNM, geometrical constrains make it very hard to reliably accommodate the punch-through structure. For this reason alternative approaches were studied: SNF/SINTEF [78] and FBK [127] deposit a temporary metal layer which allows to perform I-V test on each sensor tile, and can easily be removed one the entire wafer is characterized. For what concerns CNM, this method was not fully compatible with the testing equipment and a different selection criteria was adopted: the quality of the sensor is tested by measuring the guard ring current. Although this measurement is not representative of the full sensor leakage current, it can distinguish between good and bad sensor tiles. This method was confirmed to be effective from comparison between

before and after bump bonding currents. Fig.4.15 shows the comparison between FBK's and CNM's selection methods. Sensor selection was performed on all processed wafers and the results for all 3D technologies are described in [124] and [113]. Electrical specifications for 3D detectors and results for FBK devices will be described in more details in section 4.3.

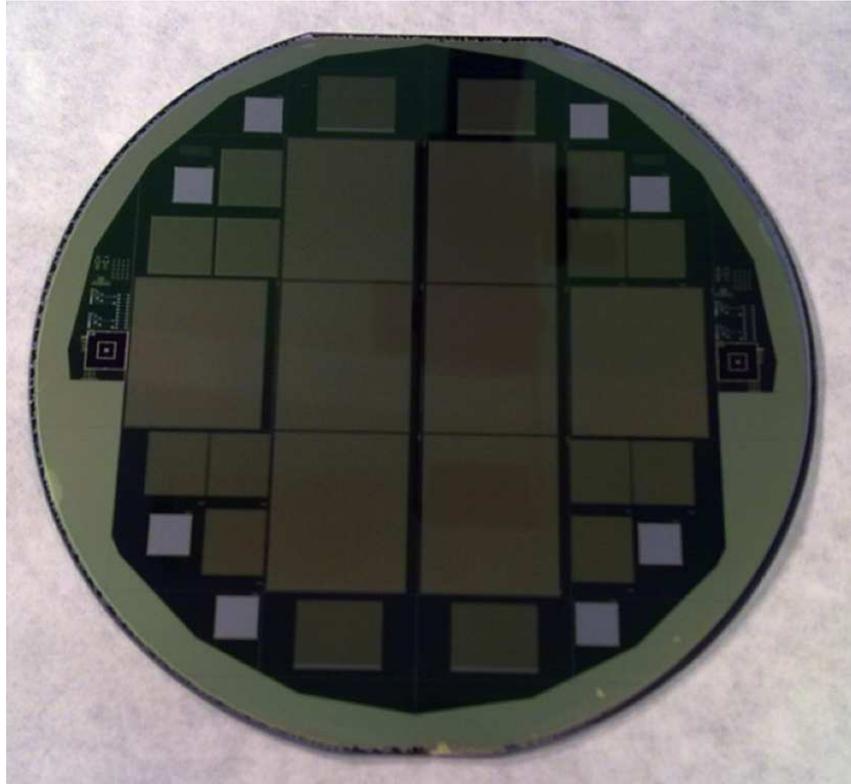


Figure 4.16: Picture of an IBL wafer produced at CNM [124].

The picture of a sensor wafer produced at CNM is reported in Fig.4.16. Given the large sensor size, 8 pixel sensors compatible with the FE-I4 readout chip could be fit on a single 4 inches wafer layout, leaving a safety margin of about 1 cm from the wafer edge. The total amount and type of sensors included in the wafer layout are:

- 8 single tile sensors matching the FE-I4 readout chip;
- 9 single chip sensors matching the FE-I3 readout chip, placed in all corners but the bottom right;
- 3 pixel sensors compatible with the CMS readout chip (PSI146V2) in the bottom right corner;
- and some planar and 3D test structures all around the wafer edge.

The qualification batch for the ATLAS IBL upgrade was started in spring 2010 at all fabrication facilities using wafers coming from the same ingot from TOPSIL. The wafers

Table 4.5: Yield of all 3D batches fabricated for the IBL [126].

Batch	Tested wafers	Selected wafers	Good sensors	Yield on selected wafers
FBK - A10	20	12	58	60.4%
FBK - A11	11	4	14	43.8%
FBK - A12	16	13	63	60.6%
FBK - A13	11	4	15	46.9%
CNM - 1	19	18	86	59.7%
CNM - 2	17	15	85	70.8%
CNM - 3	24	15	60	50.0%
OVERALL	118	81	381	58.8%

were FZ, double-sided polished, p-type, 100 mm in diameter, <100> crystal orientation and 230 μm thick, with resistivities ranging from 10 to 30 $\text{k}\Omega\text{cm}$.

The processing times were different for each processing facility, with the double-sided processes being faster. During the sensor qualification the Fast Track IBL schedule was fixed, anticipating the IBL installation to the long shutdown of 2013-2014 [111]. Because of their faster processing times, meeting the fast track IBL schedule, and the full electrical and mechanical compatibility with planar sensors, only the two double-sided technologies from FBK and CNM were finally considered for the IBL production runs. After a thorough review of the sensor layout, the sensor production started at FBK and CNM at the beginning of 2011. The production was completed in April/May 2012 with a total yield of 58.8% [126] delivering a total number of sensors equal to 381, exceeding the required 224 sensors for the IBL mixed scenario, plus a large number of spares. The yield for all the production batches at CNM and FBK is reported in Tab.4.5.

4.3 Enhanced 3D-DDTC technology at FBK

The previous technologies of FBK devices were thoroughly described in Chapter 3 section 3.4. It was understood that the effective columnar electrode overlap plays a fundamental role in the ultimate radiation hardness of the devices, and it is therefore crucial to properly calibrate the DRIE process to obtain exactly the desired column depth. The DRIE is strongly dependent on the columns diameter and even small variations of this quantity, as a consequence of imperfections of standard lithography equipments (mask aligner), can result in a column depth several micron shallower/deeper. Other issues one might encounter when etching columns from opposite wafer sides, are related to the uncertainties on wafer thickness, causing the column overlap to vary. For this reason all wafers need to be carefully measured prior to processing, adding complications to an already difficult

fabrication process.

In order to rule out any effects of the column depth uncertainty on devices behavior, an enhanced 3D technology was developed at FBK in view of the ATLAS IBL upgrade. This new approach is an evolution of the 3D-DDTC technology described in Chapter 3, the main difference being that the columnar electrodes are now fully passing through the silicon substrate. Some process steps were also modified or added in order to improve electrical and functional performances. The evolution of this new approach to 3D technology at FBK can be found in literature [128, 127, 129] and will be completely described in the next subsection. A critical analysis will be performed on technological, electrical and functional aspects.

4.3.1 Design and technological aspects

Because of the very high radiation doses expected in the IBL, the choice of fabricating n^+ readout sensors realized on p-type substrates was made. The production runs used 4", p-type, FZ wafers from TOPSIL (Frederikssund, Denmark), with a $\langle 100 \rangle$ crystal orientation and a thickness of 230 μm . A schematic cross-section is reported in Fig.4.17.

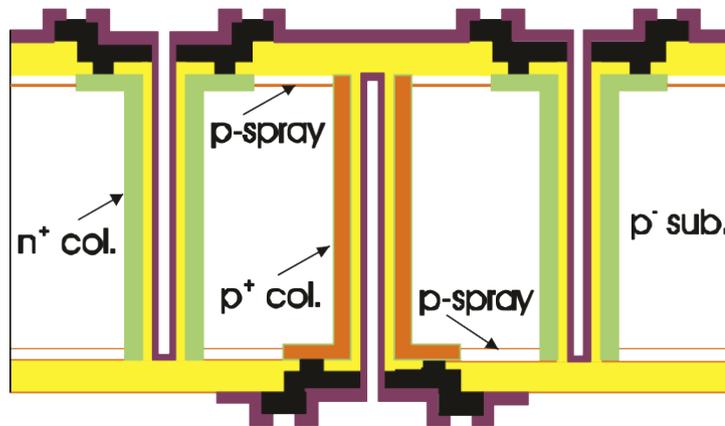


Figure 4.17: Schematic cross-section of the new 3D-DDTC technology available at FBK (not to scale) [129].

Some technological details were maintained from previous technologies and in particular:

- The column etching is performed from both wafer sides, junction columns from the front and ohmic columns from the back.
- The column doping is performed by thermal diffusion from a solid source and columns are later passivated with a thin oxide layer to prevent the dopants to diffuse out. No polysilicon filling is performed.

- Columns are hollow, therefore the contacts with the metal must be performed on the wafer surface by means of highly doped regions around the columnar electrodes.
- The support wafer is not needed thus avoiding the wafer bonding a following sacrificial wafer removal.
- The isolation between junction electrodes is performed by means of p-spray implantations and, since columns are passing through the entire bulk, the isolation must be performed on both wafer sides.

Apart from the p-spray, on the front side only n^+ implantations are present, this side will often be referred to as n-side in the following analysis (the same goes for the backside where only p^+ implants are present and will therefore be called p-side).

The peculiarity of this new process is, apart from the passing-through columns, that it is a fully double-sided process, meaning that both the front and the back sides are patterned. As previously described, the main advantage of this solution with respect to full 3D detectors, comes from the fact that the wafer back side is fully accessible thus making the devices compatible with standard planar sensors, easing the module assembly in the case of pixel detectors. On the other hand, the absence of the support wafer makes the DRIE step more critical, requiring a relatively thick stack of passivation layers on both wafer sides to act as etch stop for the column etching. Moreover, processed wafers tend to be more mechanically fragile so that special care must be taken during processing. In particular, the wafer edge should be protected against accidental damaging that could make the wafers very brittle. The edge protection was completely redesigned for this technology and will be described in the following pages.

To fabricate $12\ \mu\text{m}$ round holes on substrates up to $260\ \mu\text{m}$ thick, the parameters of the DRIE process were modified. In the standard process the lateral etch rate decreases as the depth increases. In the modified process, the etching power is gradually increased at each step in order to improve the uniformity of the etching throughout the entire process. The etch mask is composed by a combination of oxide and thick photoresist which is patterned using a standard lithography with edge bead removal. An example of columns etched from both wafer sides on a test wafer using the modified DRIE process is shown in Fig.4.18, confirming that the etching successfully penetrates the entire silicon substrate. Etched columns are not perfectly cylindrical, but tend to shrink as the etching proceeds through the bulk. The maximum etch diameter is equal to roughly $11\ \mu\text{m}$, while the minimum one is about $7\ \mu\text{m}$. The variation in diameter is not expected to seriously affect device behavior. The inset of Fig.4.18 highlights the uniformity of the etching depth and shows that no damage is present at the etch-stop membrane on the opposite wafer side.

The experience from previous 3D-DDTC batches suggested that it is crucial to properly protect the wafer edge throughout the entire fabrication in order to obtain a

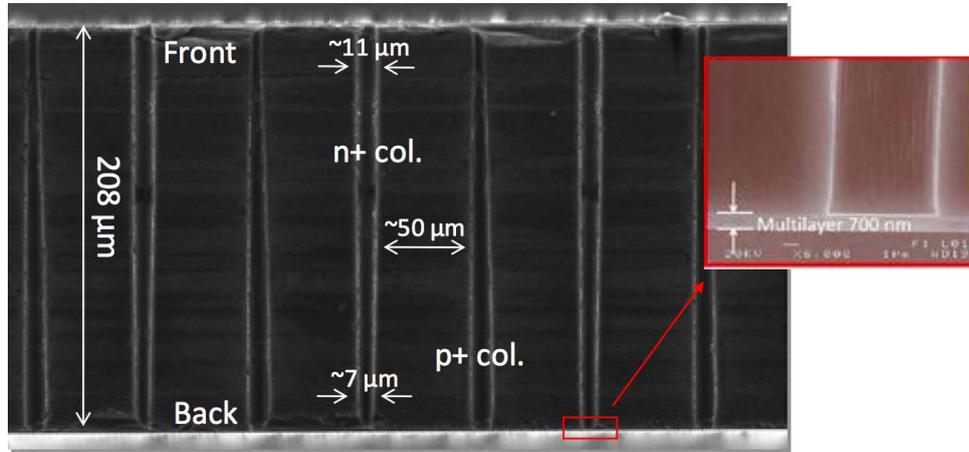


Figure 4.18: SEM micrograph of columns etched on a test wafer. The etch-stop membrane on the inset does not show any damage [129].

Table 4.6: Summary of all the R&D and IBL production batches fabricated at FBK. The different edge protection are shown together with the implanted p-spray dose. The wafer layout type for each batch is also reported [129].

Run Name	Phase	Edge protection	p-spray dose [cm^{-2}]	Layout
Batch1 (ATLAS07)	R&D	A	3×10^{12}	DTC-4
Batch2 (ATLAS08)	R&D	B	3×10^{12}	DTC-3
Batch3 (ATLAS09-I)	R&D	B	2×10^{12}	DTC-4
Batch4 (ATLAS09-II)	R&D	B	1.5×10^{12}	DTC-4
ATLAS 10-13	IBL production	B	2×10^{12}	DTC-4

sufficient mechanical yield. For this reason, a specific edge protection was implemented using different layers of dielectric materials on both wafer sides. Two versions of the edge protection were tested in the R&D batches, type "A" and type "B", finally implementing type "B" for the IBL production batches (see Tab.4.6).

Both edge protection techniques were effective in delivering a higher mechanical yield reaching peaks of 95% but with different effects on the final wafer curvature. Fig.4.19 compares the measured wafer bowing for some wafers coming from different R&D batches: it is clear that the lowest curvature is obtained for batch 2 and 3, whereas a large increase is noticeable for batch 1. This results showed how the edge protection, besides being needed for mechanical strength, also has an important influence on the final wafer bowing. The type A protection was found to be less effective in preventing the bowing because it was not perfectly balanced between the front and back surfaces. Since type B provided far better results, it was chosen for all the following batches.

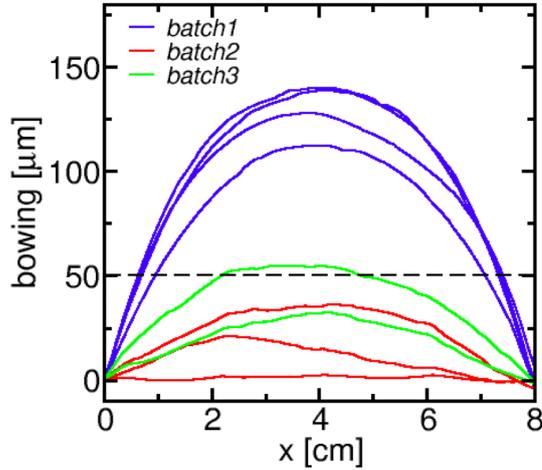


Figure 4.19: Measured wafer curvature from a subset of wafers coming from the first 3 R&D batches. The wafer center is located at $x=4$ cm. The dashed line indicates the limit on wafer bowing normally imposed by the bump-bonding facility to provide a reliable connection with the front-end [129].

The main concerns posed by the wafer curvatures are related to two different consequences:

- The large curvature can induce high mechanical stress and can ultimately cause a deformation of the silicon lattice, leading to an high bulk leakage current as will be demonstrated in section 4.4.
- Additionally, the large wafer bowing causes all the technological steps following the one causing the curvature, to be more complicated, difficult to automatize and less precise. In fact, a large misalignment between n^+ and p^+ columns etched from opposite wafer sides was found in batch 1 (see Fig.4.20(a)). This effect was less evident in the following batches, and the misalignment was found to be lower than $5 \mu\text{m}$ (see Fig.4.20(b)).

Two different wafer layouts were fabricated in the R&D batches (see Tab.4.6): the first layout (3D-DTC-3) includes pixel sensors compatible with the FE-I3 (single and double chips) and the CMS PSI46V2 readout chips (in several different configurations), strip detectors and test structures (both planar and 3D). The second wafer layout (3D-DTC-4) is fully oriented to the ATLAS 3D pixel sensors for the IBL, it is the *common layout* shared between all the processing facilities in the ATLAS 3D sensor collaboration and was previously described in subsection 4.2.2. A fabricated wafer for each layout type is reported in Fig.4.21.

As already described in previous sections, the ATLAS 3D sensor collaboration decided to adopt a 2E pixel configuration for the FE-I4 compatible sensors. This configuration includes two junction columns (n^+) per pixel, each surrounded by four p^+ columns. This

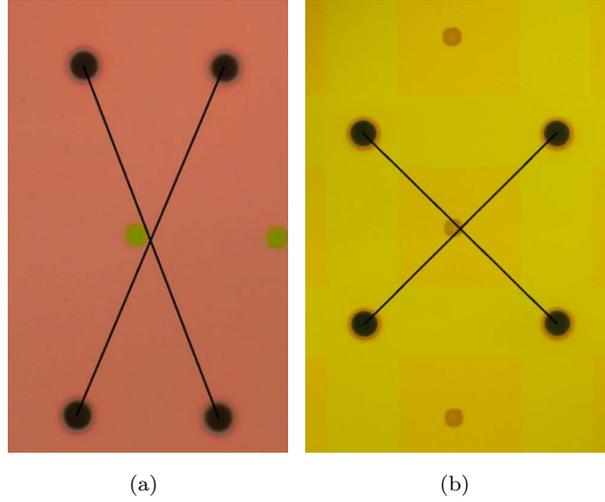


Figure 4.20: Comparison of the misalignment between columns etched from opposite wafer sides in batches exhibiting different wafer bowing: batch 1 (a) and batch 2 (b) [129].

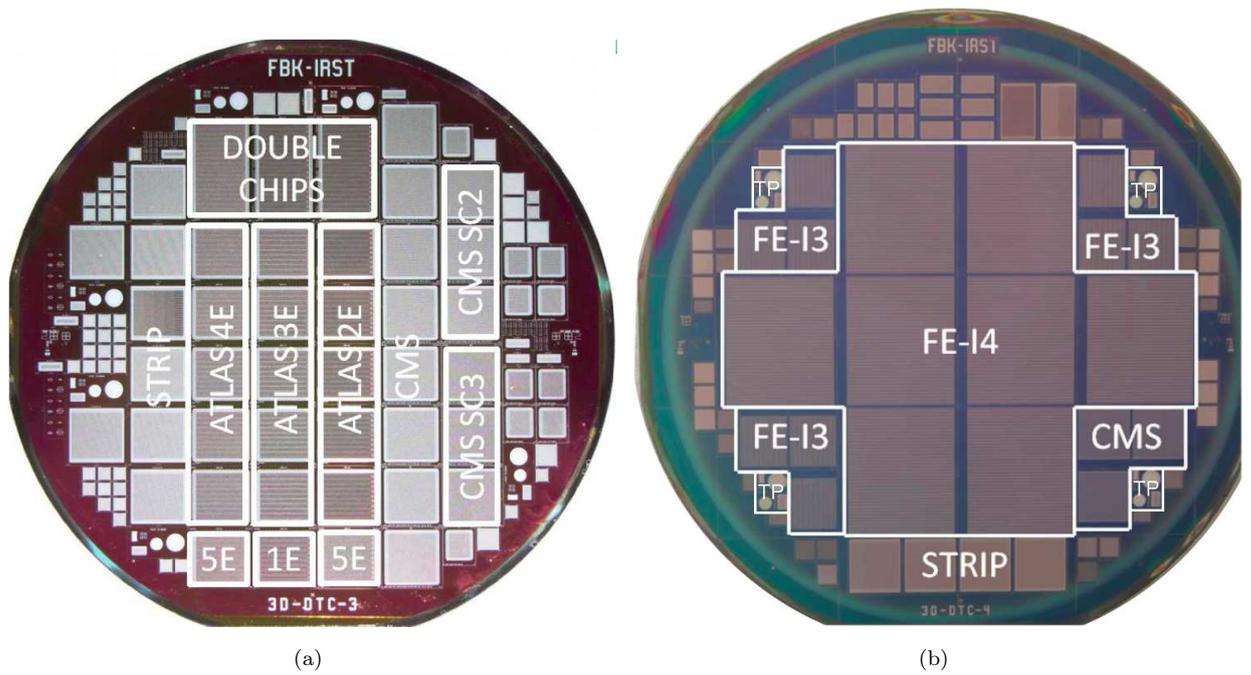


Figure 4.21: Pictures of two fabricated wafers with two different layouts: DTC-3 (a) and DTC-4 (b) [129].

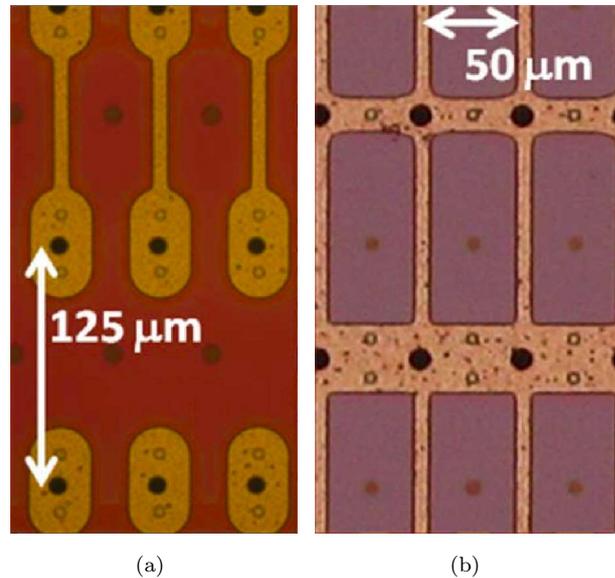


Figure 4.22: Detail of the layout of the n-side of an FE-I4 pixel detector (a), black dots are the n^+ columns etched from the front side while the brown dots are the p^+ columns etched from the backside. Detail of the p-side of the same detector (b), conversely p^+ columns are black and n^+ columns etched from the opposite side are brown [129].

means that, a pixel having a size of $250 \times 50 \mu\text{m}^2$, is composed by two identical elementary cells of $125 \times 50 \mu\text{m}^2$ having a junction column in the middle. This results in an inter-electrode distance equal to $\sim 67 \mu\text{m}$. The two n^+ columns of each pixel are connected together by means of a metallization on the front side that also provides a field-plate at the implant border (see Fig.4.22(a)). The back side is also patterned, with narrow p^+ implants and metallization connecting the ohmic columns (see Fig.4.22(b)). All the FE-I3 compatible pixel detectors on the DTC-4 layout are of 3E type (three junction columns per pixel) corresponding to an inter-electrode distance of about $71 \mu\text{m}$ that should allow to make a performance comparison between the two different ATLAS devices. The implemented CMS pixel detectors on the same batch are instead designed in 1E configuration and, as will be explained later, this configuration is not the most efficient with a maximum inter electrode distance of about $90 \mu\text{m}$.

Several 3D diodes with different layouts are present on wafers from both layouts: the DTC-3 layout only contains diodes with pitches of 80 and $100 \mu\text{m}$ between columns of same doping type, reproducing the geometries of the strip detectors, while the DTC-4 layout included one or more type of 3D diodes for each pixel/strip geometry implemented. Electrical and functional tests on 3D diodes can be fully representative of the behavior of the parent detectors and the main obtained results will be described in this work.

All devices in the DTC-4 layout are designed with slim-edges, having a total extension

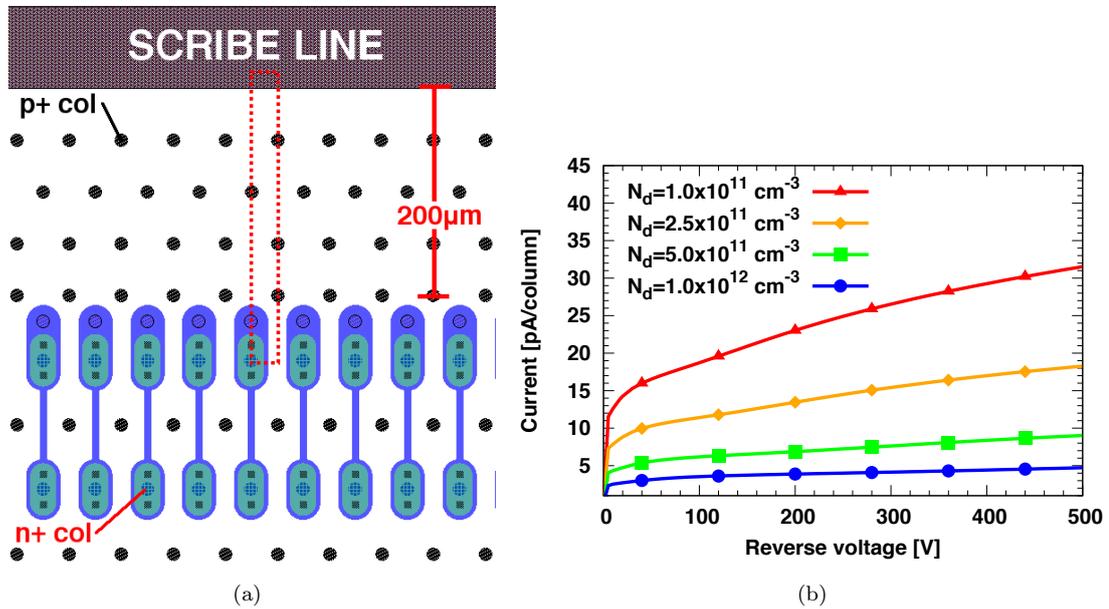


Figure 4.23: Final layout of the slim-edge for an FE-I4 pixel sensor indicating dimension and simulation domain (a), and simulation results as a function of bias voltage and bulk doping concentration [128].

ranging from the minimum $200 \mu\text{m}$ requested for the edges of the FE-I4 pixels in the z direction, to about $400 \mu\text{m}$ on other edges for which no constraints were fixed. The main idea behind the slim-edge design is to prevent the depletion region spreading from the outermost junction column to reach the highly damaged cut region. In order to make it more difficult for the depletion region to move toward the outside, a fence of ohmic columns can be placed. The position of each p^+ electrode must be carefully decided and this can be done with the aid of numerical simulations. Numerical simulations were performed by modeling the cut edge with a low lifetime region ($\tau < 1 \text{ ns}$). Different fence layouts were studied and the more promising one is shown in Fig. 4.23(a) [128]. The dashed region represents the simulation domain, including the last junction column and four ohmic electrodes. All the standard semiconductor physics models were enabled apart from the avalanche model, in order to rule out any premature discharge effects not related to the edge region. The analysis is performed by looking at the current of the n^+ column as a function of the reverse bias. Different substrate concentrations were considered in the design phase because this information was not available yet. Simulation results are reported in Fig. 4.23(b) and no premature discharge is observable before 500 V , a voltage that is well beyond the expected operating biases of 3D detectors. After irradiation edge current injections become less of an issue because it is more difficult for the depletion region to grow toward the cut due to the increased bulk concentration caused by radiation damage.

The slim-edge was intensively tested both electrically and functionally and

results are described in the next subsections. The slim-edge is not available in the DTC-3 batch where the edge termination is realized with standard planar guard-rings that are only partially effective.

4.4 Pre-irradiation electrical characterization of FBK devices

Fabricate devices were electrically characterized both on wafers and after cut. The electrical characterization starts from standard planar structures placed on the wafer to control the quality of the process parameters. The focus then moves to specific 3D structures like diodes, strip and pixel detectors with different methodologies. It is important to remember that, in the specific case of the IBL production wafers, the very first measurements performed is a current-voltage (I-V) measurement on FE-I4 pixel sensors, by means of a temporary metal, in order to distinguish between good and bad sensors. The temporary metal is then removed and the other measurements performed. This section will discuss all the most important findings regarding all the investigated sensor geometries in pre-irradiation conditions.

4.4.1 Planar test structures

All the available wafer layouts include several test pads, mainly composed by standard planar test structures, used to evaluate the goodness of the process by extracting the most important parameters from electrical measurements. Fig.4.24 shows the detail of one of the test pads included in the IBL production wafers, that are also highlighted with TP in Fig.4.21(b). Many different structures were designed in order to measure different

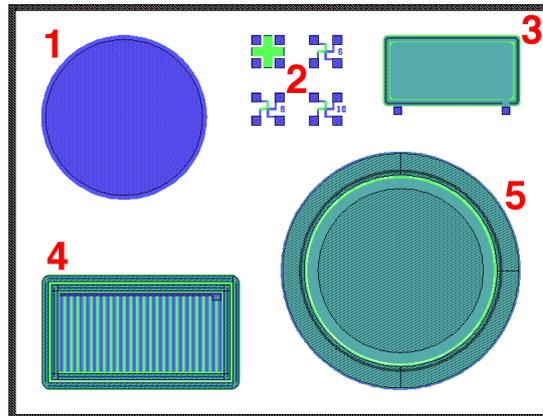


Figure 4.24: Available planar test structures: a MOS capacitor (1), some Van der Pauw structures (2), a MOS capacitor realized on a highly doped substrate (3), a gated diode (4) and a planar diode with one guard ring (5).

Table 4.7: Available planar test structures and their size. The parameters extracted from electrical characterization are also reported: t_{ox} and Q_{ox} are the oxide thickness and the oxide charge concentration, $R_{implant}$ and $R_{contact}$ are the resistivity and the Hall coefficient of the n^+ implantations and the contact, C_{AC} is the value of the MOS capacitor realized on a highly doped substrate, s_0 is the surface recombination velocity and J_{bulk} , V_{FD} and N_{bulk} are the bulk leakage current density, the full depletion voltage and the bulk doping concentration.

Structure	Extracted parameters	Size (note)
MOS capacitor	t_{ox} , Q_{ox}	0.03 cm ²
Van der Pauw	$R_{implant}$, $R_{contact}$	-
Coupling capacitor	C_{AC}	0.01 cm ²
Gated diode	s_0	0.01 cm ² (gate)
Planar diode with guard-ring	J_{bulk} , $\tau_{n,p}$, V_{FD} , N_{bulk}	0.04 cm ² (diode)

parameters:

1. *MOS capacitor*: used to measure oxide thickness (t_{ox}) and oxide charge concentration (Q_{ox}) by means of capacitance-voltage (C-V) measurements.
2. *Van der Pauw structures*: allow to measure the resistivity and the Hall coefficients of the n^+ implantations and also provide important informations on the contact resistance.
3. *Coupling capacitor*: used to obtain an estimation of the value of the integrated coupling capacitor realized on strip detectors.
4. *Gated diode*: estimation of the surface recombination velocity (s_0) by means of particular I-V measurements.
5. *Planar diode with one guard-ring*: allows to extract several different parameters and, among them, the bulk leakage current density and the carrier lifetimes in the bulk (I-V), the full depletion voltage (C-V) and the bulk doping concentration (C-V).

A summary of all the available structures together with the process parameters that are possible to extract and their size is reported in Tab.4.7. The measurement procedures will be discussed and the most relevant results are reported in Tab.4.8 for all the available sensor batches.

Measurements on planar diodes are performed on-wafer at the probe station using a semiconductor parameter analyzer (I-V) or an LCR meter (C-V). For I-V measurements, the diode and the guard-ring are grounded while the backside p^+ implantation is swept from zero to large reverse biases. The diode and guard-ring currents are recorded and plotted separately. The breakdown typically occurs on the outer guard-ring junction, where the n^+ implantation is in contact with the highly doped p -spray region. After the diode current saturates and well before the appearance of possible avalanche breakdown

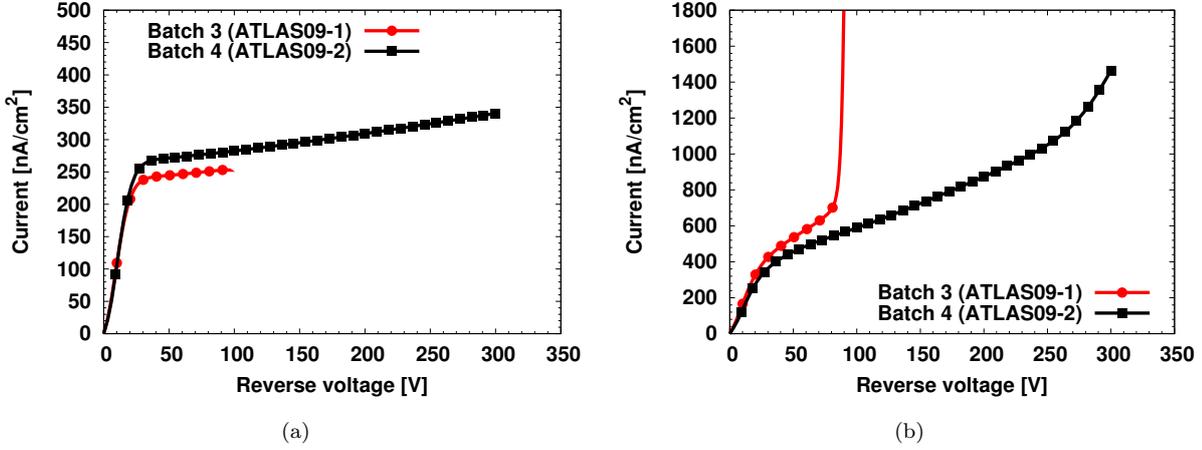


Figure 4.25: I-V measurements performed on two planar diodes from batch 3 (ATLAS09-1) and batch 4 (ATLAS09-2) featuring two different p-spray implant doses: diode current (a) and guard-ring current (b).

effects, the current density value (J_{bulk}) allows to extract the carrier lifetimes inside the bulk.

The leakage current densities for batch 1 (ATLAS07) were found to be in the order of $1 \mu\text{A}/\text{cm}^2$, much larger than what obtained in older 3D-DDTC technologies (see Chapter 3 subsections 3.4.3 and 3.4.4). This was caused by the high mechanical stress wafer sustained during fabrication, which is strictly related to the large wafer bowing observed as a consequence of an unbalanced edge protection. In subsequent batches the wafer curvature was limited and the current density decreased by one order of magnitude, leading to much better carrier lifetimes.

The breakdown voltage of all planar diodes was found to be strictly dependent on the implanted p-spray dose, as expected. Batch 1 (ATLAS07) and batch 2 (ATLAS08) had rather high p-spray doses and the breakdown voltage was found to be very low. This was later corrected, starting from batch 3 (ATLAS09-1), by decreasing the p-spray implanted dose. Breakdown voltages of planar diodes were found to increase up to more than 300 V (the lowest p-spray dose is equal to $1.5 \times 10^{12} \text{ cm}^{-2}$ for batch 4). The p-spray dose was finally fixed to a value of $2 \times 10^{12} \text{ cm}^{-2}$, a value that was believed to be able to maintain pixel isolation up to and beyond IBL radiation fluences. The pixel isolation was tested after several irradiation campaign and results will be described in section 4.5. An example of diode and guard-ring currents measured on planar test diodes is reported in Fig.4.25 for two devices coming from batch 3 (ATLAS09-1) and batch 4 (ATLAS09-2) featuring two different p-spray doses. The difference in the p-spray doping manifests itself with a large difference in breakdown voltage. Diode current densities (Fig.4.25(a)) are equal to about $250 \text{ nA}/\text{cm}^2$ while the guard-ring current densities (Fig.4.25(b)) are larger because

Table 4.8: Summary of the extracted process parameters measured from standard planar test structures for all the batches with passing through columns. Reported values are: the leakage current density J_{bulk} , the carrier lifetimes $\tau_{n,p}$, the breakdown voltage V_{BD} , the surface recombination velocity s_0 and the oxide charge concentration Q_{ox} [129].

Run name	J_{bulk}	$\tau_{n,p}$	V_{BD}	s_0	Q_{ox}
	$[\mu A/cm^2]$	$[\mu s]$	$[V]$	$[cm/s]$	$[10^{11} q/cm^2]$
Batch 1 (ATLAS07)	1	57	45	30	2-6
Batch 2 (ATLAS08)	0.1	570	40	50	7-10
Batch 3 (ATLAS09-1)	0.25	230	100	5	3-4
Batch 4 (ATLAS09-2)	0.25	230	>300	5	3-4
ATLAS 10-13	0.15	382	100	5	3-4
p-spray-test (dose=2.5e12 cm ⁻²)	3	19	54		
p-spray-test (dose=3.0e12 cm ⁻²)	3	19	44	30	2-6
p-spray-test (dose=3.5e12 cm ⁻²)	3	19	36		
p-spray-test (dose=4.0e12 cm ⁻²)	2	28	32		

the guard-ring tends to deplete a larger volume being on the outside. The full depletion voltage can be estimated to be around 30 V from the knee of the diode current.

In order to rule out the dependence of the bulk leakage current on the DRIE process, and to study the relation between the breakdown voltage and the p-spray implanted dose, some test wafers were processed skipping both column etchings. The results for these wafers are reported in Tab.4.7 and are referred to as "p-spray-test". As can be observed, the process parameters remain essentially the same as for the other cases, confirming that the DRIE step does not affect the process quality. Moreover, the clear dependence of V_{BD} from the p-spray dose was confirmed, with increasing discharge voltages occurring for lower p-spray doses. As reported in Chapter 2, subsection 2.1.2, the breakdown voltage of a pn-junction is strictly dependent on the doping concentration of the less doped region (Eq.2.29), thus increasing the doping concentration of the p-spray will cause the discharge voltage to decrease.

The bulk doping concentration was estimated from C-V measurements on planar diodes and was found to be about $7-8 \times 10^{11} \text{ cm}^{-3}$, common to all batches, because the wafers came from the same ingot. The full depletion voltage estimated from the position of the knee in the C-V measurement was found to be about 27-28 V, in good agreement with what observed in planar diode reverse currents. An example of C-V measurement on two devices from batch 3 and batch 4 is reported in Fig.4.26. The saturated capacitance is $\sim 2 \text{ pF}$ (Fig.4.26(a)), anyway it is very hard to extract the full depletion voltage from the simple C-V measurement. For this reason the $1/C^2$ curve is extracted and plotted clearly

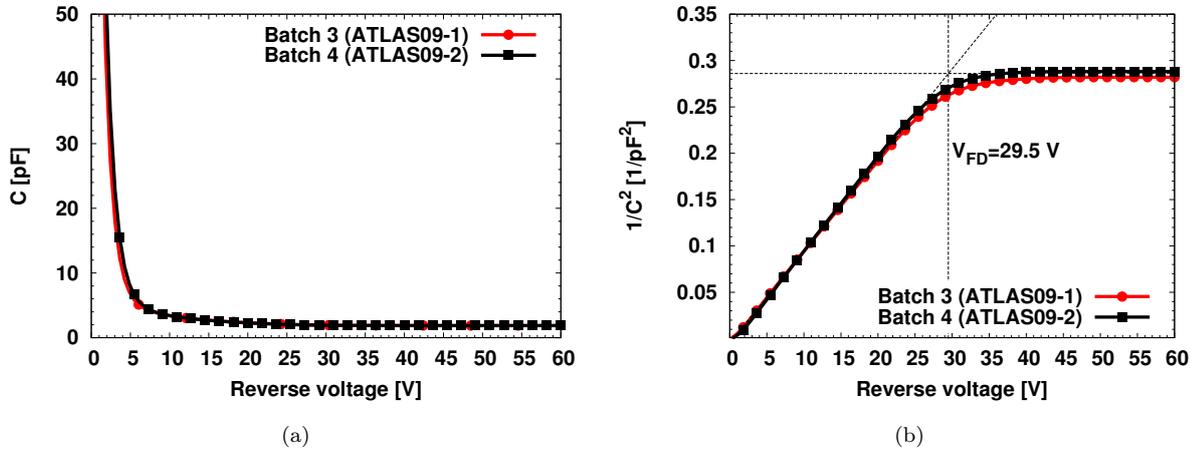


Figure 4.26: Capacitance-voltage measurements on devices from batch 3 and batch 4 (a) and $1/C^2$ measurement for the same devices (b). The extracted full depletion voltage is also indicated in the $1/C^2$ plot.

showing the knee in the capacitance measurement (Fig.4.26(b)).

As for surface related parameters, values for both Q_{ox} and s_0 were found to be quite high in the first two R&D batches, fact that was ascribed to the non optimized edge protection. After the optimization of the latter, from batch 3 on, s_0 was reduced to low values, as expected on $<100>$ wafer, and a Q_{ox} returned to the values measured in previous 3D-DDTC technologies. Oxide thicknesses were found to be quite large, ranging between 1 and 1.3 μm , as expected due to the thick surface passivation layers used as etch stop for the DRIE step.

The measured contact resistance on batch 1 was found to be rather large, in the order of a few hundred kilo ohms. This effect was ascribed to a partial over etch inside the contact holes. Although this problem was less evident in following batches, for security measure it was decided to add an additional process step performing a low energy phosphorus implantation inside the contacts to increase their quality. This was seen to restore the contact resistance to less than a few hundred ohms.

4.4.2 3D-diodes

The high leakage current caused by the wafer bowing and the strong dependence of breakdown voltage from the implanted p-spray dose was observed also on 3D test structures. The 3D test structures available are so-called *3D diodes*, featuring arrays of columns of both doping types, etched from the front (n^+) and from the back (p^+), connected together by a combination of highly doped surface implantations or metal links (or a combination of both). These devices are intended for a simpler electrical and functional characterization

Table 4.9: Summary of the most important parameters of devices under test [130].

Parameter	Unit	FE-I4 FP	FE-I4	80 μm	CMS
Device active area	mm^2	9.30	9.30	9.73	8.27
Elementary cell size	μm^2	125×50	125×50	80×80	100×150
Number of cells	-	61×24	61×24	39×39	19×29
Minimum cell size	μm^2	62.5×25	62.5×25	40×40	75×50
Inter-electrode distance	μm	67.31	67.31	56.57	79.06
N ⁺ to P ⁺ min. distance	μm	14	38	19	18
Field-plate width	μm	5	n.p.	5	n.p.
N ⁺ links	-	Yes	No	Yes	No

with respect to larger detectors. In fact, having only two terminals, the testing procedures are much more immediate than for pixels or strip detectors.

For the measurements on 3D diodes to be fully representative of the behavior of parent detectors, devices must be designed to reproduce all the layout details present in pixel/strip sensors. On the DTC-4 wafer layout (IBL production), four different types of 3D diodes were implemented. A basic description of each device is here reported, important layout parameters are summarized in Tab.4.9 and the layouts of the front and back side are shown in Fig.4.27:

- *FE-I4 diode with field-plate* (FE-I4 FP): it reproduces the geometry of the FE-I4 pixel detector. It features a field-plate (extension of the metal outside the implant region and above the oxide) and columns of the same type are connected together with both metal and highly doped implantations.
- *FE-I4 diode without field-plate* (FE-I4): same geometry of the previous diode but columns of the same doping type are here connected only by metal links on the front side while the back side remains unchanged. The field-plate is not present.
- *80 μm pitch diode* (80 μm): representative of the strip detector geometry this 3D diode configuration features a very regular layout. The field-plate is implemented and columns of the same doping type are connected together by both metal and implantations.
- *1E CMS diode* (CMS): the geometry of the 1E CMS pixel detectors is reproduced on this devices. The elementary cell only features one n⁺ column surrounded by six p⁺ columns. Electrodes are connected by metal links on the front side and by both metal and implantations on the back.

Because columnar electrodes are hollow, a surface implanted "island" is necessary to perform contact with the metal. This implantation is differently shaped in each device and, as will be described shortly, it strongly influences its electrical behavior.

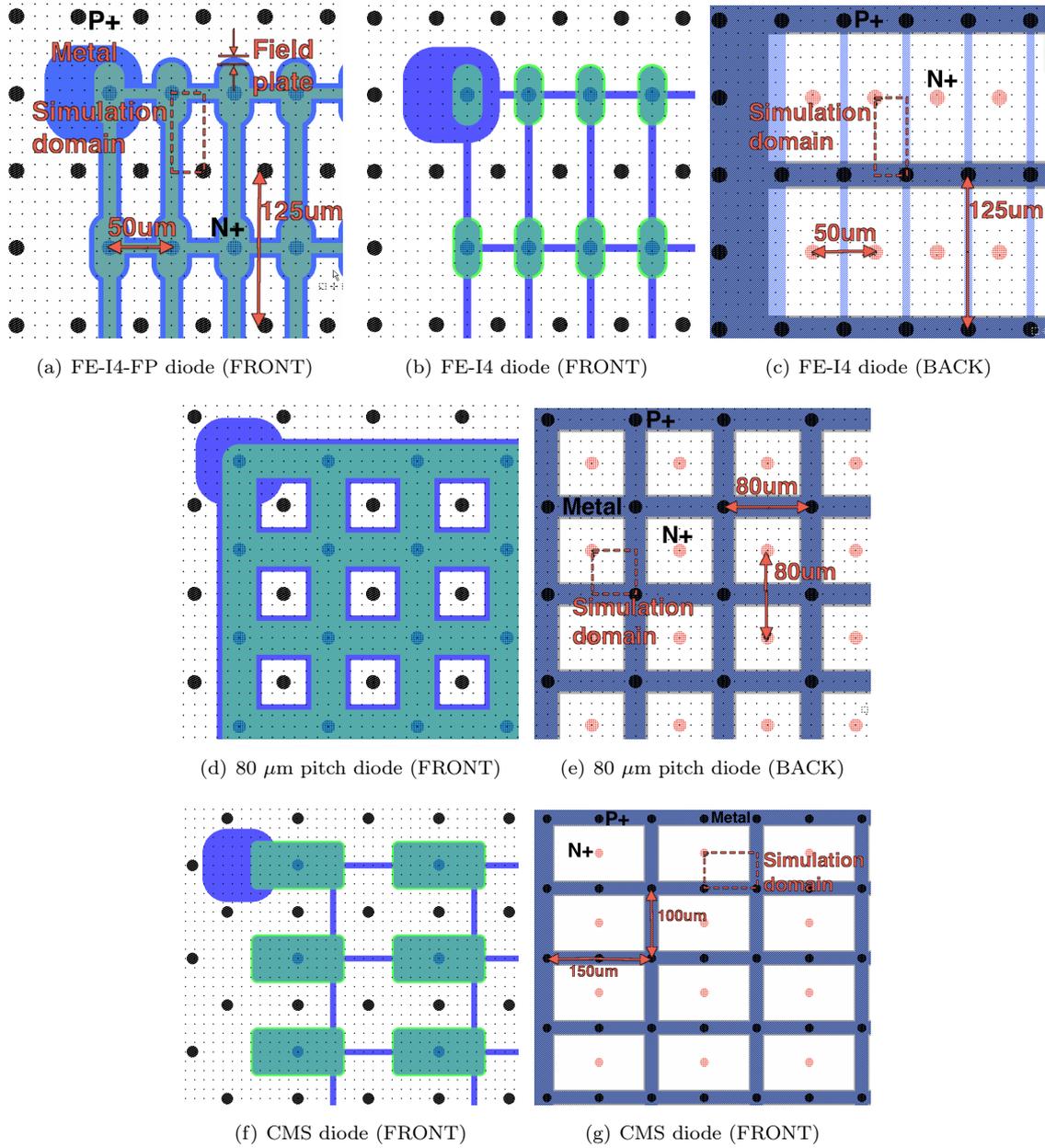


Figure 4.27: Layouts of the 3D diodes available on the DTC-4 layout used for the IBL production. Two FE-I4 diodes with different frontside layout (a,b) and same backside (c), a diode with 80 μm pitch between columns of the same doping type (d) and (e), and a CMS diode in 1E configuration (f) and (g). Basic dimensions, layout details and simulation domain are also reported.

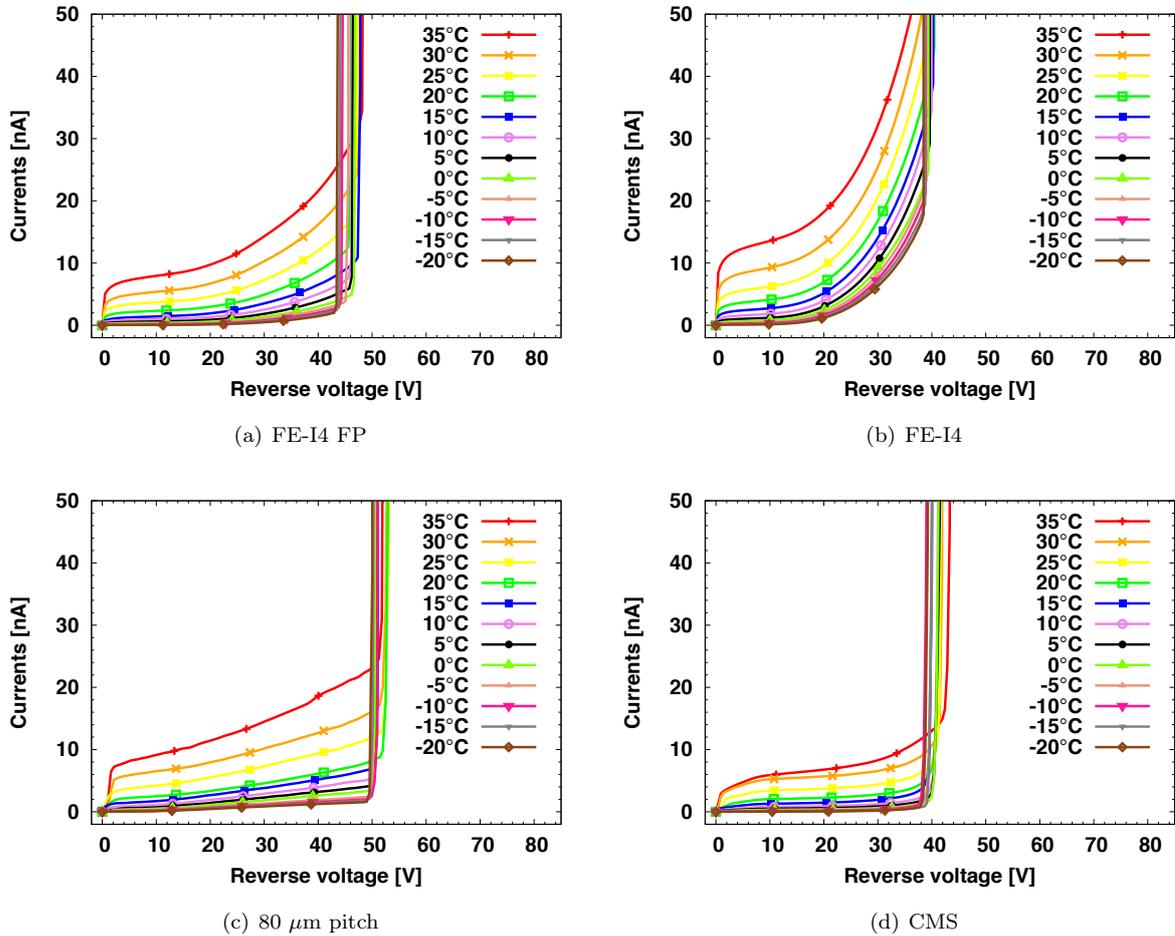


Figure 4.28: I-V measurements performed on all 3D diode layouts available with variable temperature. FE-I4 diode with field-plate (a) and without field-plate (b), 80 μm pitch (c) and a CMS diode (d).

A large campaign of electrical measurements and numerical simulations (I-V and C-V) was performed on each device type [130]. Several devices were tested on-wafer and those with better property were cut, glued and wire bonded to some home-made PCBs in order to perform a full electrical characterization as a function of the operational temperature. The devices here examined came from Batch 1 (ATLAS09-1), wafer 20. The measurement setup was composed by a climatic chamber, a semiconductor parameter analyzer HP4145 and an Agilent LCR meter 4284a. The temperature variation was in the range from -20°C to 35°C .

The measured reverse currents for each device type are reported in Fig.4.28. The trend of the leakage current with temperature is following the expectations (increasing for larger temperatures) and the break down voltage is in good agreement with the values found on other devices from the same batch and with the expectations related to the high

p-spray dose. It is important to remember that, although the discharge occurs rather early with respect to standard devices, the full depletion of these sensors is always lower than 10 V for all the examined configurations (observing the currents in Fig.4.28, the knee always manifests itself before 10 V). As will be explained later, the low breakdown voltage is combination of different effects, the already mentioned high p-spray concentration and the fact the p^+ columns coming from the back side bring the bias directly to the p-spray on the front side.

In order to gain a deeper insight into the device behavior and to exclude the presence of undesired effects, a deep data analysis was performed. Breakdown voltages were plotted as a function of the temperature and linearly fitted to extract the rate of increase/decrease. The discharge voltage was defined as the voltage for which a factor 10 increase in current was observed. The increasing trend with temperature of the breakdown voltage found in this study is in good agreement with the generally accepted values for the considered p-spray doping concentration [131]. The results are reported in Fig.4.29, clearly showing

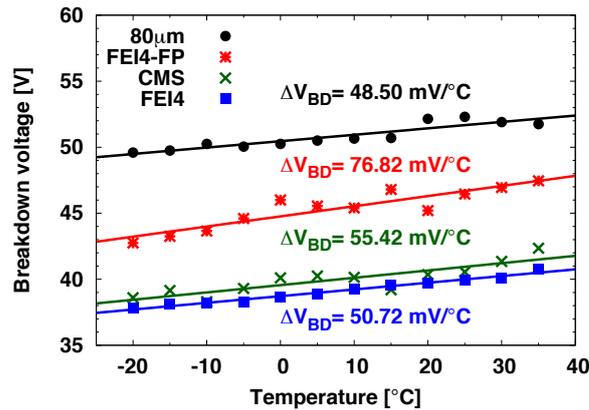


Figure 4.29: Trend of breakdown voltages for all the considered 3D diodes as a function of temperature [130].

a layout dependence. The two devices featuring the field-plate have larger maximum operating voltages, thus suggesting that this layout detail plays an important role. This is particularly evident when comparing the two FE-I4 layouts, with and without field plate, where a 5 V difference in breakdown voltage can be observed. The 80 μm diode, besides implementing the field-plate, also features a very regular layout without sharp corners, allowing it to intrinsically handle larger voltages. The CMS diode seems to be the more critical, slightly worse than the FE-I4, and this can be attributed to the shape of the n^+ surface implantation, which is very large and has rather sharp corners that enhance the high field peaks at the n^+ to p-spray junction on the front side. An additional remark to be made is related to the breakdown of the FE-I4 diode without field-plate:

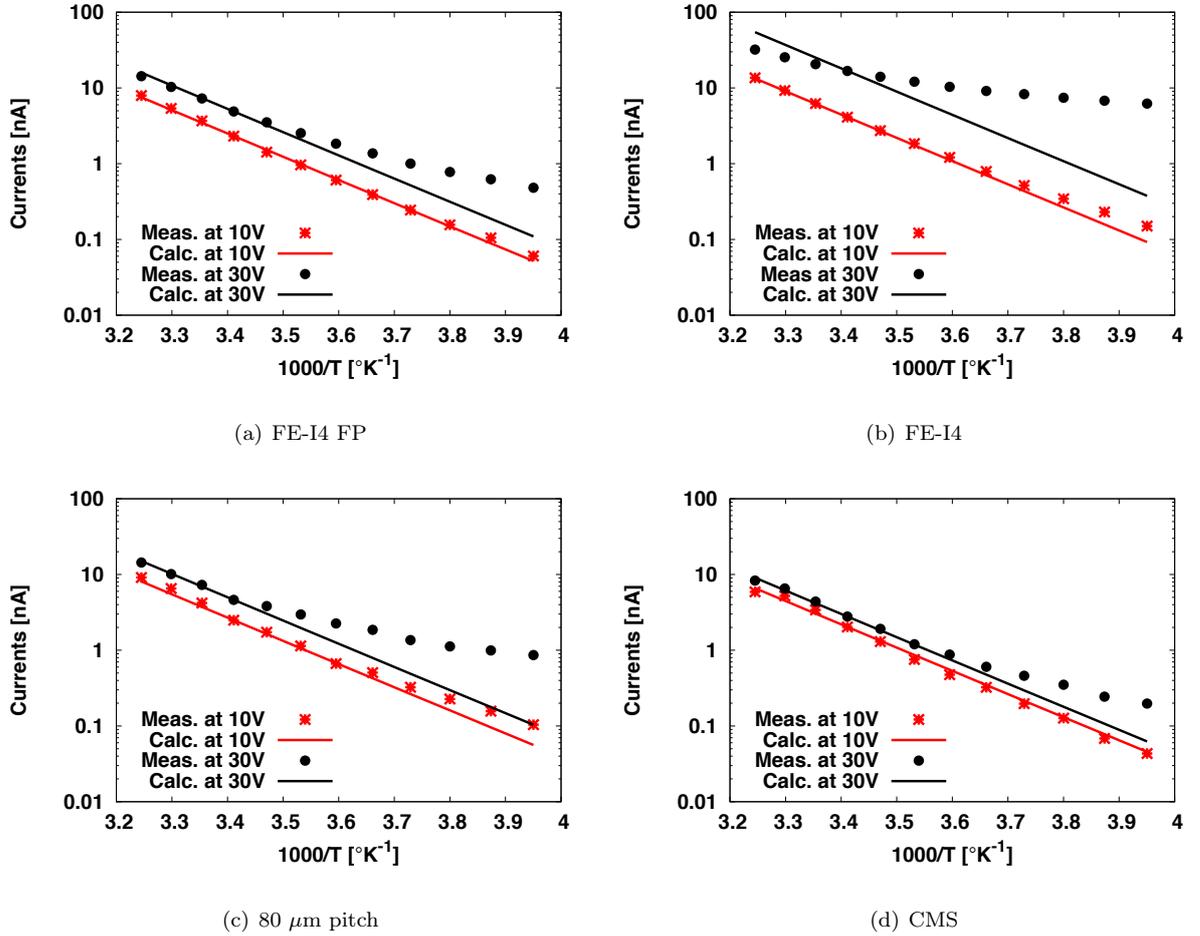


Figure 4.30: Comparison between measured (symbols) and calculated (solid lines) values of leakage current at two different bias voltages (10 V (a) and 30 V (b)) for each available diode layout: FE-I4 diode with field-plate (a) and without field-plate (b), 80 μm pitch (c) and a CMS diode (d).

although the reverse discharge is expected to occur earlier than in the devices with the same layout but with field-plate, the slope of the currents in Fig.4.28(b) is much higher than for other devices, fact that suggests the possible presence of defects triggering early avalanche effects.

In order to verify if the reverse current was mainly due to SRH generation, the measured current values were compared with the theoretical calculation for different temperatures and different biases. As previously described in Chapter 2 subsection 2.1.2, in case of a purely SRH behavior, it is possible to predict the expected reverse current at a certain temperature T_2 by knowing the current for a reference temperature T_1 and applying Eq.2.28. The results obtained for each device are shown in Fig.4.30, where the Arrhenius plots of measured and calculated data are compared for two different bias

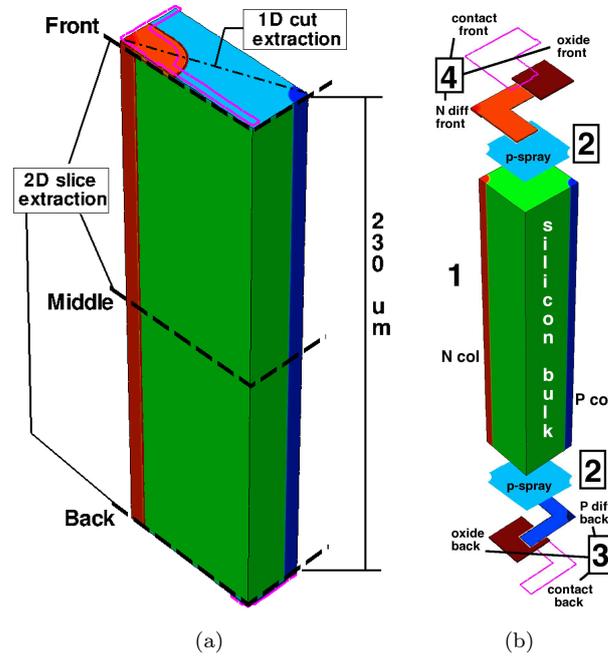


Figure 4.31: Example of simulated structures for the two used operational procedure: a full structure of an FE-I4 diode showing the 1D and 2D extraction planes/lines (a) and the "exploded" structure for an $80\ \mu\text{m}$ pitch diode indicating all the components gradually added in the correct order.

voltages, 10 and 30 V. The lower bias value is chosen just above full depletion of all four devices, and measurement and calculations are in very good agreement. As the reverse voltage is increased up to 30 V, devices get closer to breakdown and measured current values deviate strongly from the theoretical expectations, especially for lower temperatures (right region of the plots). This effect is enhanced by decreasing temperatures because of the lowering of the breakdown voltage previously shown in Fig.4.29. The FE-I4 diode is the one showing the largest deviation, in good agreement with the large slope of the reverse current observed in Fig.4.28(b).

To confirm the findings of the electrical measurements and gain better insight into the device behavior, numerical simulations were performed with the aid of the Synopsys TCAD tools. Thanks to the symmetry of the devices it is possible to only simulate a quarter of an elementary cell thus reducing the number of nodes and the computational time. The simulation results are then scaled to match the full size of the sensor. The simulation domain is highlighted in Fig.4.27 for all the devices. In order to properly model the sensors, all the most important process related parameters were included in the simulation according to the values reported in Tab.4.8. Standard physics models were enabled together with the avalanche generation model driven by the electric field component parallel to the carrier direction, and the band-to-band recombination model.

Table 4.10: Summary of measured and simulated values of breakdown voltage, leakage current/slope and capacitance [130].

Parameter	unit	FE-I4 FP	FE-I4	80 μ m	CMS
V_{BD-sim}	V	44.0	37.8	48.0	39.0
$V_{BD-meas}$	V	46.5	39.9	52.3	40.6
$I_{@10V-sim}$	nA	4.8	4.4	4.4	3.4
$I_{@10V-meas}$	nA	3.7	6.2	4.2	3.4
$I_{@20V-sim}$	nA	5.4	5.0	4.6	4.1
$I_{@20V-meas}$	nA	7.3	20.6	7.3	4.4
$[I_{@20V}/I_{@15V}]_{sim}$	-	1.02	1.03	1.01	1.02
$[I_{@20V}/I_{@15V}]_{meas}$	-	1.15	1.31	1.16	1.02
$C_{@10V-sim}$	pF	195.0	160.0	186.0	89.4
$C_{@10V-meas}$	pF	203.0	151.8	189.3	89.7
$C_{@40V-sim}$	pF	121.0	133.0	113.0	72.2
$C_{@40V-meas}$	pF	149.0	127.4	135.0	73.9

The simulation procedure was divided in two steps investigating different effects: the first step was to perform an I-V simulation of the entire structure in order to compare the simulation results with measurements and observe the distribution of all the most important electrical quantities inside the device. The second simulation step was aimed at understanding how every layout component of the device affects the total capacitance. For this reason the structure was split in several parts that were added in sequence. The example structures for both simulation steps are reported in Fig.4.31.

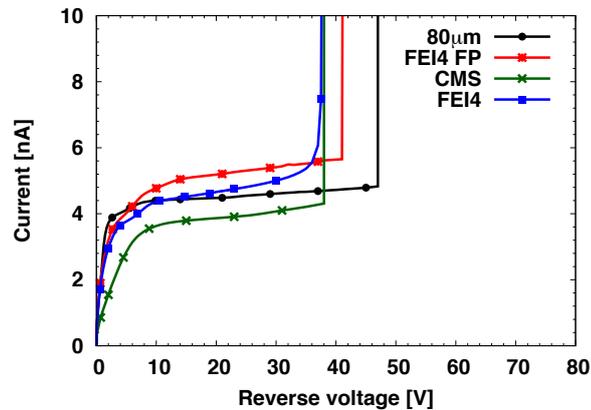


Figure 4.32: Simulated leakage currents for all the investigated devices at a temperature of 25 °C [130].

Simulated leakage currents are reported in Fig.4.32 for all devices and at a temperature

of 25 °C. The comparison with measured values are reported in Tab.4.10. Simulated breakdown voltages are in agreement with measurements. Leakage currents, instead, correctly represent the absolute current value immediately after full depletion, while do not match the slope observed in the measurements. This effect is believed to be related to interface states that were not included in the simulation and might be responsible for the slope of the measured currents. Further investigations on this are currently on going but the extraction of the properties of the surface states from test structures are not simple and require proper instruments.

Besides the mismatch in the current slope, simulation can return important informations related to the distribution of the electrical quantities inside the sensor for the different layout implementations. For the sake of conciseness only the distribution of the electric field in the most critical regions of the devices is reported in Fig.4.33 for a bias voltage of 35 V, not far from breakdown. As already discussed, the breakdown is believed to occur where the highly doped p-spray is in contact with an n^+ region. The main findings can be summarized as follows:

- all structures have two high electric field regions: (i) the n^+ to p-spray junction on the front side and (ii) the n^+ column to p-spray junction on the back side, the former begin typically more critical if the field-plate is not implemented.
- the effect of the field-plate on the front side is to split the main electric field-peak into two lower peaks, thus enhancing the voltage handling capabilities of the device. Mono-dimensional electric field profiles extracted front the diagonal of the device connecting the n^+ and the p^+ electrodes close to the surface are shown in Fig.4.34. The effect of the field plate is evident: without field plate the most critical region is the curvature of the n^+ "island" on the front side, whereas if the field-plate is implemented the breakdown occurs on the backside (e.g. the peak electric field in Fig.4.33(a) is larger on the right picture than on the left picture).
- the 80 μm pitch diode is the less critical because its layout only features concave corners and, additionally, the field-plate is present.
- the CMS diodes suffers from very high electric field peaks on the front side, at the corners of the n^+ "island" which are rather sharp and cause early discharge. In addition the field-plate is not implemented.

The C-V simulations were performed for all the devices with very similar results. For this reason only the simulation results for the FE-I4 sensor with field-plate are here reported (Fig.4.35). A total of five simulation steps were performed, each adding a different layout detail:

1. Only the substrate and the columnar electrodes are implemented.
2. The p-spray is added on both wafer surface.

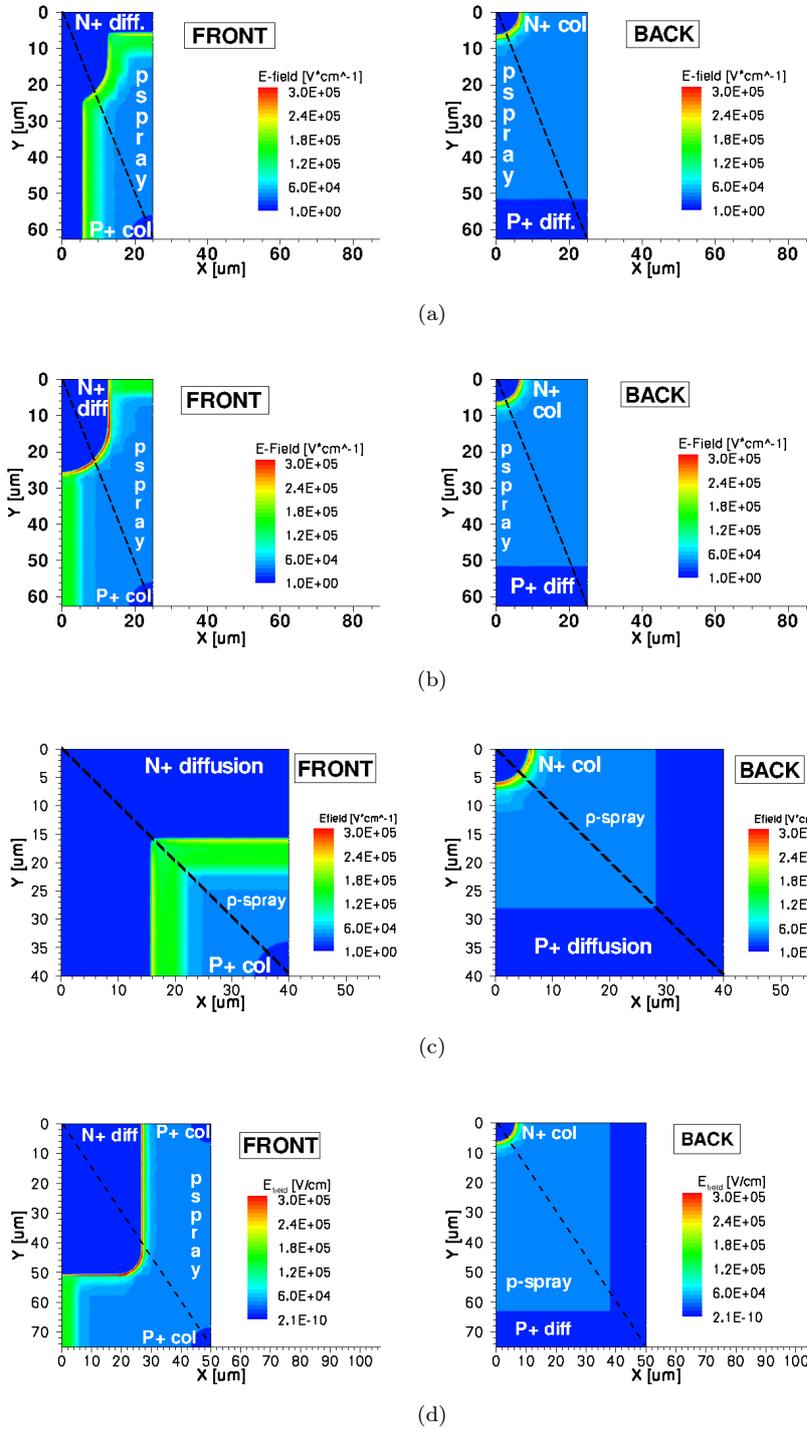


Figure 4.33: Bi-dimensional simulated electric field distributions for all the considered structures extracted from the front (left) and back (right) surfaces for a bias voltage of 35 V: FE-I4 with field-plate (a), FE-I4 without field-plate (b), 80 μm pitch (c) and CMS (d).

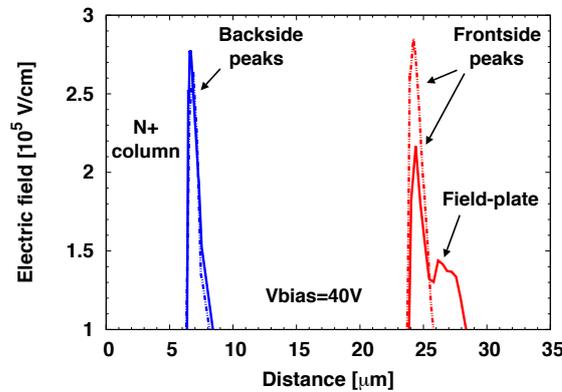


Figure 4.34: Comparison between the simulated electric field distribution on the front (right) and on the back (left) sides of the two FE-I4 diodes biased at 40 V. The field plate case is plotted (solid lines) against the case without field plate (dashed lines). Data were extracted from the diagonal connecting two electrodes of opposite doping types close to both sensor surfaces [130].

3. The p^+ implantation on the back side is added.
4. The n^+ implantation on the front side is added after removing the previously added p^+ implantation.
5. All the steps are combined into the full structure.

The basic structure composed by only the bulk and the columns, presents a capacitance of roughly 51.4 pF, corresponding to about half of the final device capacitance. Adding the p-spray on both wafer sides causes an increase in capacitance of 30 pF because of the n^+ column to p-spray junctions. The p^+ implantation on the back side only marginally affects the detector capacitance. What strongly affects the the shape of the C-V curve is the layout of the front side: the n^+ island has a very large perimeter which is in contact with the p-spray. At low bias voltages, a sizable difference in capacitance is observable with respect to the previous cases. As the bias is incremented, it is possible to partially deplete the p-spray and reduce the capacitance that eventually saturates at around 50 V. The simulation of the full structure does not show any capacitance differences from the previous step thus confirming the dominant component added by the n^+ implantation on the front side.

The measured curve, also reported in Fig.4.35, is in very good agreement with simulations for low biases, whereas a slight difference is observed a higher voltages. This discrepancy is well understood and is related to the additional capacitance component added by the depletion region proceeding outside of the active area of the device after full depletion, entering the slim-edge. This effect was not taken into account in the simulations because of the need to keep the number of grid points low enough to obtain reasonable

computational times.

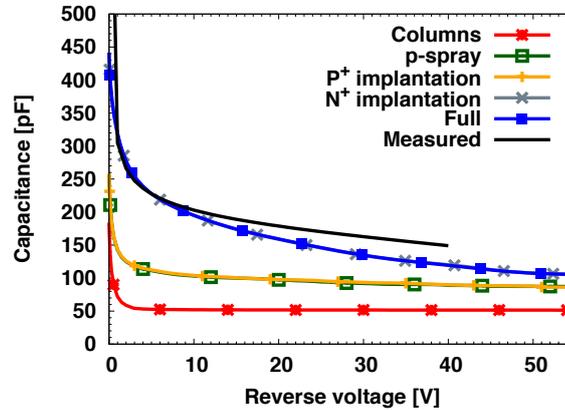


Figure 4.35: Evolution of the simulated detector capacitance after adding each layout detail for an FE-I4 devices with field-plate [130].

The slim-edge, designed for FE-I4 pixel detector to satisfy the IBL requirements, is also implemented in all 3D diodes for testing purposes. The electrical operation of the slim-edge was tested on 3D diodes to assure that no current injection from the cut edges could be observed. To do so, a specific test was performed at FBK using a diamond saw [125]: 3D diodes exhibiting good electrical characteristics were extracted from the wafer by means of a diamond saw cut following the scribe line. After a quick current measurement on cut devices, the cutting procedure was repeated by dicing closer to the active area. Currents were later remeasured to assess the effects of the cut on the devices. This procedure was repeated several times, cutting closer to the active area at each step using as reference the ohmic columns of the slim-edge fence. The very first test was performed on diodes coming from batch 1, featuring a low breakdown voltage due to the high p-spray dose, and were later repeated on sensors from batch 3 featuring much larger reverse discharges. Results here reported were obtained from 80 μm pitch 3D diodes: the performed cuts are sketched in Fig.4.36(a) and the measured leakage currents after each cut are shown in Fig.4.36(b) for the device from batch 1 and in Fig.4.36(c) for the devices from batch 3. These tests returned very good results, in fact no cut related increase in leakage current was observed up to the fourth cut, not only confirming that the slim-edge works properly, but also suggesting that there is room for improvement. Since the intrinsic breakdown voltage of diodes from batch 1 was rather low, the tests were repeated also on devices with higher breakdown (from batch 3) to be sure that the full operation of the devices was possible up to a larger voltage.

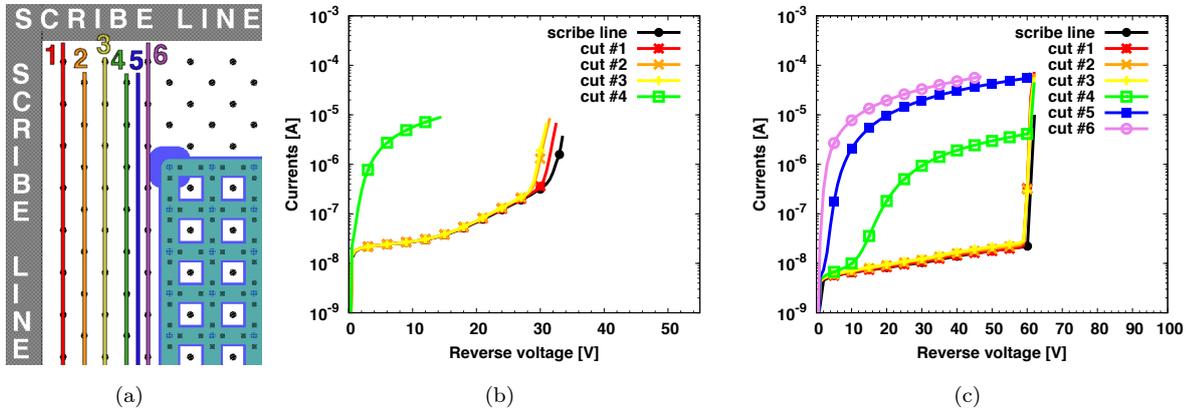


Figure 4.36: Electrical testing of the slim-edge on $80 \mu\text{m}$ pitch 3D diodes: performed cuts (a) and measured leakage currents for devices from batch 1 (ATLAS07) (b) and batch 3 (ATLAS09) (c) [125].

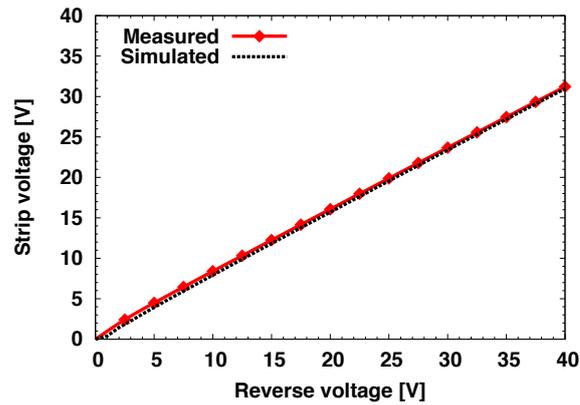


Figure 4.37: Electrical measurements of the voltage of a single strip in a device coming from the DTC-2 batch as a function of the applied bias, compared to the numerical simulation of the same structure.

4.4.3 Strip detectors

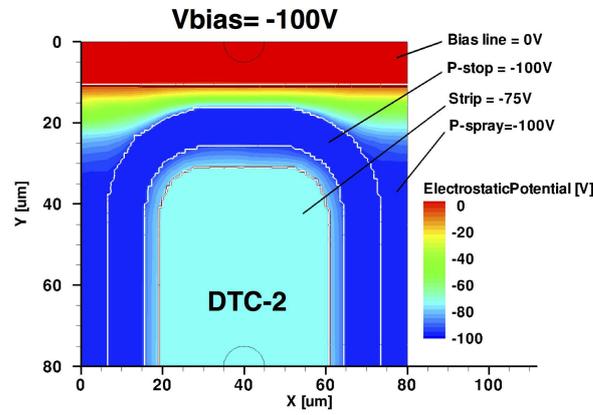
As already mentioned in Chapter 3 subsection 3.4.4, strip detectors from the DTC-2 batch exhibited some performance issues that were believed to be caused by the malfunctioning of the punch-through biasing mechanism. When designing strip devices for the new batches a thorough investigation was performed: the operation of the punch-through bias was re-measured on old wafers in order to compare the results with numerical simulations. The first results are reported in Fig.4.37, where the actual strip voltage is plotted with respect to the simulated one. As can be observed, no saturation is observed and the strip voltage follows the bulk voltage almost with the same trend. In fact, for an applied bias of 40 V, the strip voltage is equal to roughly 30 V, translating into an actual bias on the strip of only 10 V. To better understand the motivation to this poor performance of the

punch through bias, the 3D and 2D distributions of the electrostatic potential inside the simulated device were analyzed. Fig.4.38(a) shows the potential distribution on the upper surface of the detector (where the punch-through should occur) for a bias voltage of 100 V. The avalanche model was turned off in the simulation because not strictly necessary for the intended investigation. It is possible to notice that almost the entire p-spray/p-stop layers are biased to the same potential of the backside and the strip itself reaches a potential of 80 V. This effect is caused by the fact that in the DTC-2 technology, the ohmic column depth was much more optimized (almost 190 μm on bulk thickness of 200 μm). Because of this small gap between the p⁺ column tip and the opposite wafer surface, the coupling between the ohmic columns and the p-spray is very strong even for low biases, and the potential is brought almost unaltered to the front side. This causes the strip to follow the potential of the bulk instead of the potential of the bias line. Thanks to the powerful simulation tools available, successive modifications were applied to the simulated device in order to obtain a punch-through structure working as expected:

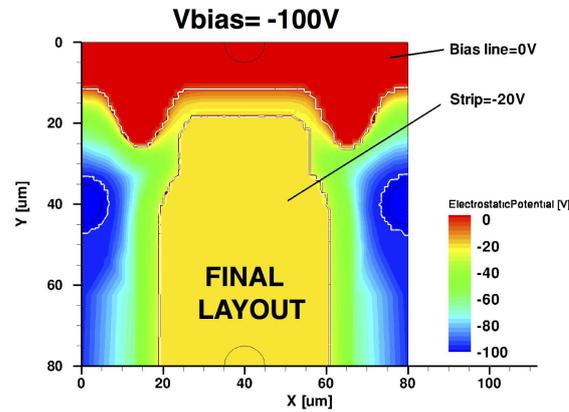
1. *P-stop removal*: the p-stop was not needed and was not leaving any space to realize full passing-through ohmic electrodes so it was removed, also hoping to obtain a preliminary improvement of the punch through bias.
2. *Full columnar electrodes*: all columnar electrodes were made to be completely passing through.
3. *Reduced strip to bias line distance*: in order to increase the coupling between the strip and the bias line, their mutual distance was reduced down to $\sim 5 \mu\text{m}$.
4. *Modified bias line geometry*: to further increase the coupling between strip and bias line, the geometrical configuration of the latter was modified in order to almost "encapsulate" the strip itself.

As can be observed in Fig.4.38(c), each small modification was tested and lead to an incremental improvement of the punch-through mechanism. In fact, the strip voltage for the final device implementation is roughly 20 V for an applied bias of 100 V, leading to an actual strip bias of ~ 80 V. The electrostatic potential distribution on the front surface of the final simulated structure is reported in Fig.4.38(b). Differently from what observed for the DTC-2 device in Fig.4.38(a), this time a smaller portion of the front surface is biased to the same potential applied to the backside and the strip voltage is considerably lower. The new strip detectors were then designed and fabricated with the same simulated geometry shown in Fig.4.38(b).

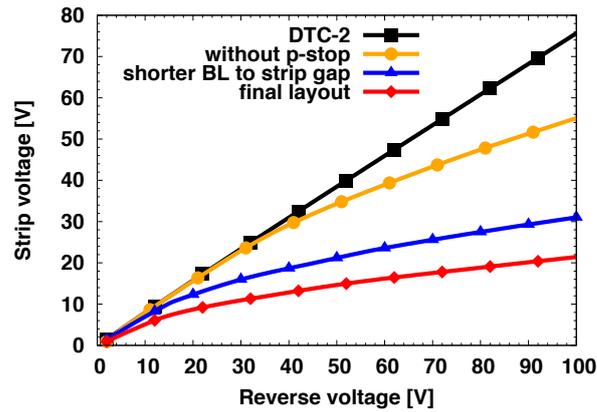
In the DTC-4 batch (common layout for the IBL), four strip detectors were included. The pitch between the strips and the columns of the same doping type was 80 μm and the strips are biased using the newly designed punch-through structures. Both DC and AC pads are available. Layout detail can be observed in Fig.4.39. The electrical characterization



(a)



(b)



(c)

Figure 4.38: Numerical simulation results of the punch-through mechanism in 3D strip detectors: electrostatic potential distribution on the front side of a DTC-2 strip detector for a bias voltage of 100 V (a) compared with the same result for a DTC-4 detector in the same conditions (b) and evolution of the simulated punch-through mechanisms for the incremental applied modifications (c).

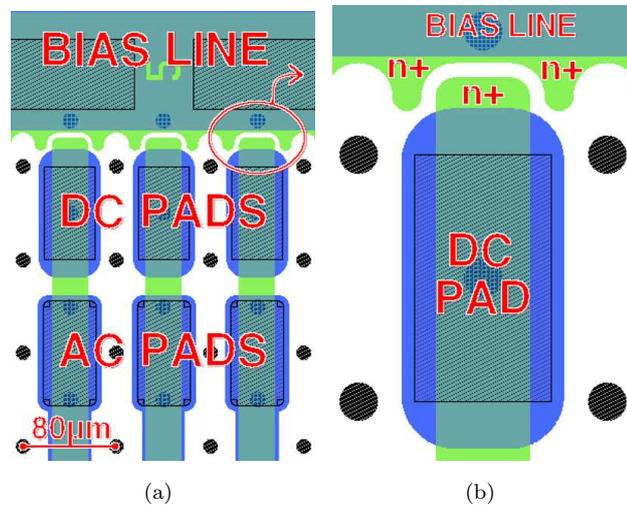


Figure 4.39: Layout details of the $80\ \mu\text{m}$ strip detectors included in the DTC-4 wafer layout [132].

was performed on wafer using a probe station and by means of I-V and C-V measurements. The devices here discussed come from some wafers of the batch ATLAS10 (IBL production) that were not eligible for bump-bonding because of the not sufficient amount of good pixel devices. The very first test performed, was a quick current measurement of the device in order to separate good from bad ones. Fig.4.40 shows the obtained reverse currents, for good devices from wafers 9, 19, 21 and 24. The reverse current at full depletion was found to be $1.96\ \text{pA}/\text{column}$, slightly higher than in previous batches (as already expected). The full depletion extracted from the knee in the reverse current plot, is believed to be well below $10\ \text{V}$, and numerical simulations confirmed that it was indeed $\sim 6\ \text{V}$. The breakdown occurs at about $40\ \text{V}$ for most of the devices.

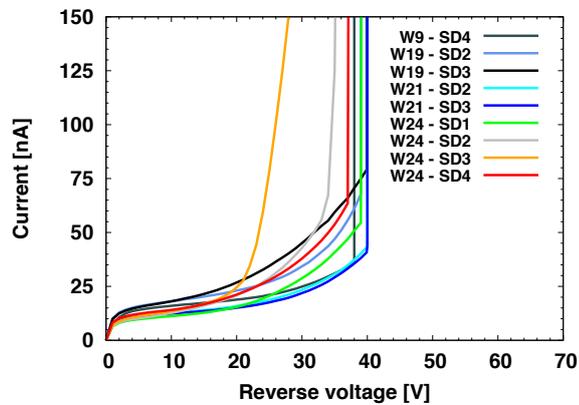


Figure 4.40: Measured leakage currents for good 3D strip detectors coming from the ATLAS10 batch [132].

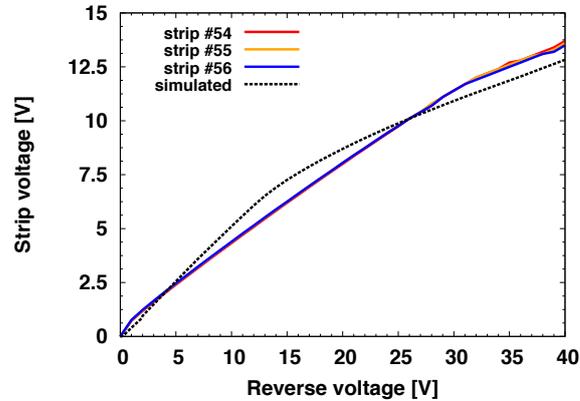


Figure 4.41: Measured versus simulated strip voltage as a function of the applied electrostatic potential on 3D strip sensors coming from one of the IBL production batches [132].

In order to prove that the design of the new punch-through structure was effective, the voltage of a few strips was monitored as a function of the applied bias. Results are reported in Fig.4.41 where they are also compared with the performed numerical simulations. The agreement is very good and confirms the correct operation of the strip biasing mechanism.

In order to predict what to expect in terms of noise and device operation a complete capacitance characterization was also performed. The strip to back capacitance was measured from the DC pad with an LCR meter while grounding both the bias line and the two neighboring strips. An example measurement is reported in Fig.4.42(a). A sharp decrease in capacitance was observed at low biases with the knee occurring before 10 V. Full saturation is not reached because as the bias increases, a larger portion of the p-spray on both wafer surfaces can be depleted. This effect was also observed in both measurements and simulations on 3D diodes as previously described (see subsection 4.4.2).

The inter-strip capacitance was measured between a strip and the two neighboring ones while grounding the bias line and increasing the bias voltage applied to the back-side. A frequency sweep was performed in order to evaluate if the parasitic capacitance could have different effects on the different signal components. The measurement was repeated for several applied bias voltages and results are reported in Fig.4.42(b). The capacitance is roughly constant to a value of ~ 0.9 pF in the frequency range 1-100 kHz. At higher frequency a decrease in capacitance is observed but this is believed to not affect the sensor signal.

As mentioned in subsection 4.4.1, the oxide thickness on both wafer sides was found to be roughly $1.3 \mu\text{m}$. The oxide on the upper surface is used as a dielectric for the strip integrated coupling capacitor. A cross-section of a strip is reported in Fig.4.43(a): the

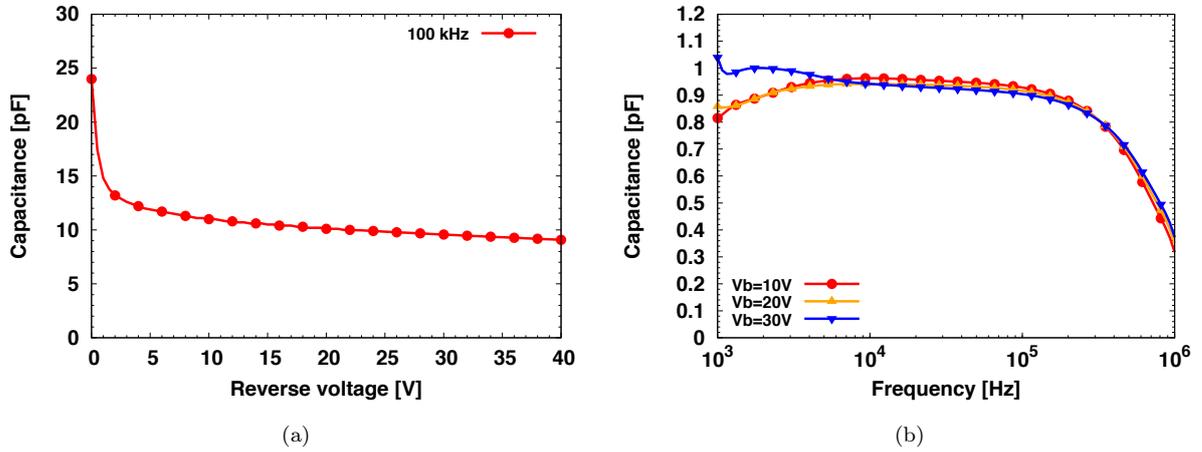


Figure 4.42: C-V measurements performed on 3D strip detectors from the IBL production batches: strip to back capacitance (a) and inter-strip capacitance (b) [132].

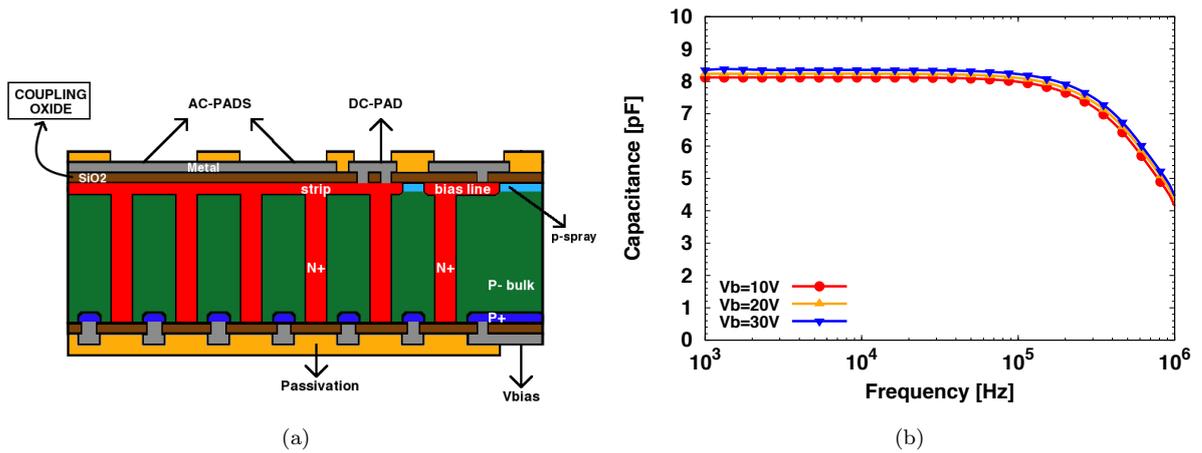


Figure 4.43: 3D strip cross-section (along the strip) showing the implementation of the AC coupling capacitor using the front side oxide (a) and measured value for the AC coupling capacitor [132].

Table 4.11: Summary of the main electrical parameters of the considered 3D strip detectors [132]

Parameter	unit	Value
Full depletion voltage	V	~6
Breakdown voltage	V	~40
Strip current @ full depletion	pA/column	1.96
Strip to back capacitance @ full depletion	pF	9.0-10.0
Interstrip capacitance @ full depletion	pF	0.9
Coupling capacitance	pF	8.1

DC pad is connected directly to the n^+ strip implantation while the two AC pads are isolated from the strip by means of the silicon oxide. By assimilating this structure to a parallel plate capacitor, it is known that the capacitance value is directly proportional to the plate area and inversely proportional to the inter-plate distance. If this distance becomes larger, the capacitance value decreases. The integrated coupling capacitor was measured by connecting one LCR meter channel to the DC pad and the other one to the AC pad. The applied signal frequency was swept from 1 kHz to 1 MHz for different bias voltages. The obtained results are shown in Fig.4.43(b): the capacitance value (~ 8.1 pF) was indeed found to be rather low, comparable with the strip to back capacitance and not too far from the parasitic (inter-strip) capacitance. This will translate into a non effective signal transmission in response to impinging radiation. This can be corrected by wire bonding the sensor DC pads to the readout electronics using an RC fan-in, as will be discussed later.

All the most important device parameters extracted from the electrical characterization are collected in Tab.4.11 and can be compared to the ones found in previous technologies

Devices will be irradiated with 25 MeV protons at the Karlsruhe Institute of Technology Synchrotron up to large fluences and the characterization will be repeated.

4.4.4 ATLAS FE-I4 Pixel detectors

All the process parameters were extracted from standard planar and 3D structures that also allowed, by means of comparison with simulations, to fully understand the electrical behavior of the sensors. The electrical characterization was also performed on pixel sensors but mainly for one reason: being the bump bonding and flip-chip very expensive, with a cost increasing with the number of wafer on which the UBM must be deposited, it is crucial to perform an on-wafer selection in order to distinguish good from bad sensors. In order to do so, a strict set of electrical specifications was fixed to decide which sensors

Table 4.12: Electrical specifications for the on-wafer electrical selection of the pixel sensors for the IBL [124].

Parameter	Symbol	Value
Operation temperature	T_{op}	20-24 °C
Depletion voltage	V_{depl}	<15 V
Operation voltage	V_{op}	$\geq V_{depl} + 10$ V
Leakage current at operation voltage	$I(V_{op})$	<2 μ A
Breakdown voltage	V_{bd}	>25 V
Leakage current "slope"	$I(V_{op})/I(V_{op}-5V)$	<2

were to be considered good from on-wafer measurements in pre-irradiation conditions. The specifications are reported in Tab.4.12. The operation temperature to be set in the test was decided to be between 20 and 24 °C. The required full depletion voltage was requested to be lower than 15 V, and simulations confirmed that, for FBK devices, it was roughly 8 V [130]. The desired operating voltage was set to be 10 V higher than the full depletion voltage in order to be able to use the sensors in over-depletion. The limit on sensor current at the operating voltage was set to be 2 μ A and the breakdown voltage limit to consider the sensor good was imposed at 25 V. In order to perform the requested on-wafer selection, a specific testing method was developed at FBK, allowing to measure the current of all the 80 rows of 336 pixels making up the sensor at once [129]. This was obtained with the use of a temporary metal layer deposited over the passivation on the front side and patterned in strips, contacting the underlying pixels through the openings in the passivations within the bump pads. Each strip is terminated with a pad to perform the desired I-V measurement. The deposited secondary metal strips with their pads are shown in Fig.4.44(a) while a detail of a single pixel is reported in Fig.4.44(b). In order to minimize the risk of damage and contamination during the tests, the wafers are protected on the backside with a passivation layer that will be patterned after the completion of the tests. Since the bulk contact (p^+) on the backside is not available due to the presence of the passivation layer, and is not present on the front side, the bias is provided by forward biasing a n^+ /substrate junction on the n-side. The value of the forward bias, typically a few tenths of volt, is fixed by the sum of the leakage currents of all the reverse biased pixel/substrate junctions. This method was proven to be effective and reliable by measuring 3D diodes on un-passivated wafers providing the bias either from the back or the front side, obtaining essentially the same results. The 80 I-V measurements (one per strip of pixels) are performed at room temperature (~ 23 °C) on an automatic probe station by means of a probe-card. The current of the entire sensor is then obtained as the sum of all the 80 strip currents. The measurements performed on two wafers from

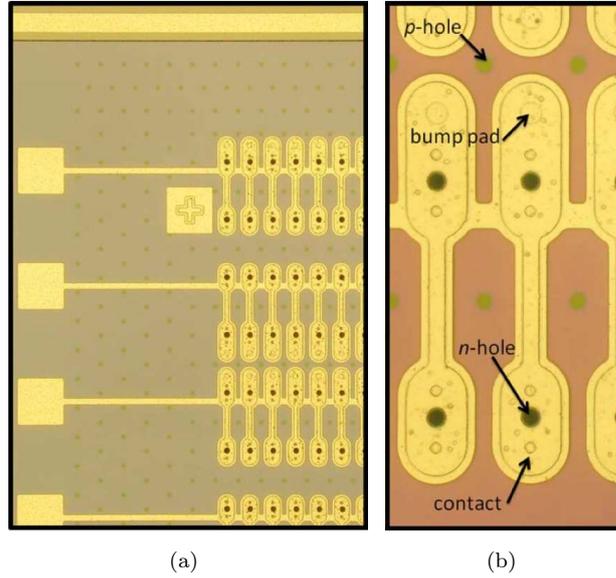


Figure 4.44: Pictures of the temporary metal layer deposited on the sensors to perform the on-wafer selection: a view of the metal strips and their pads (a) and the detail of a pixel with the deposited metal (b) [129].

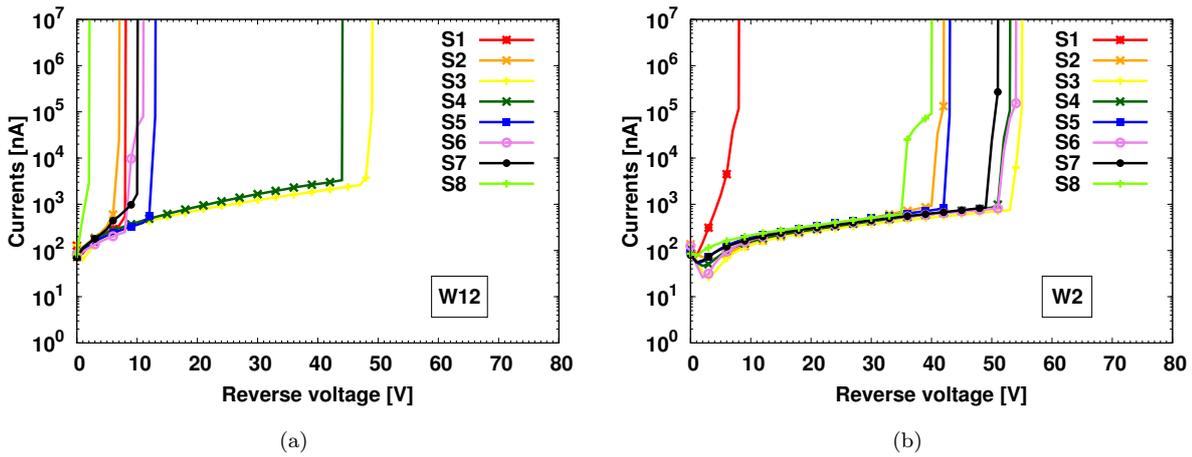


Figure 4.45: FE-I4 pixel sensor leakage currents measured for two different wafers coming from the IBL production batch ATLAS12: wafer W12 with only two sensor respecting specifications (a) and wafer W2 with seven sensors in specification.

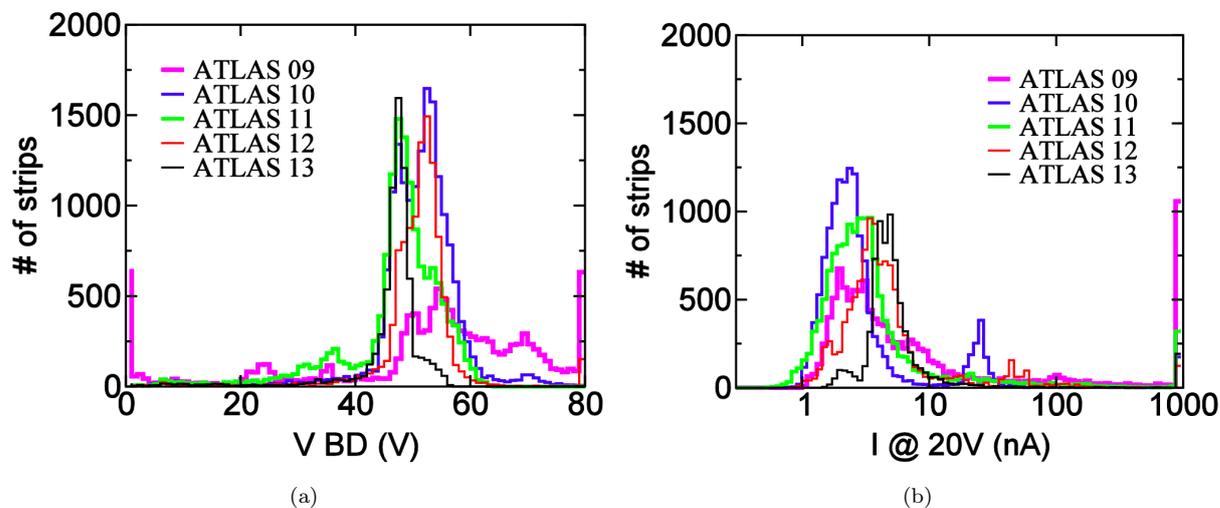


Figure 4.46: Statistical distributions of breakdown voltages and leakage currents (at 20 V) of each measured strip connecting 336 pixels in an FE-I4 sensor, as measured in the automatic tests [129].

the IBL production batch called ATLAS12 are reported in Fig.4.45. Wafer number 12 (Fig.4.45(a)) only exhibits two sensors compliant with the electrical specifications while wafer number 2 features a total of seven sensors in specification. In order to contain the costs, it was decided that only wafers featuring three or more good sensors were going to be sent for bump bonding [124]. In the cases examined in Fig.4.45 only W2 was considered good.

All the wafers from the IBL pre-production and production runs at FBK were tested with this method. Because of the large number of measured strips (80 strips \times 8 sensors \times number of wafers), the distributions of the obtained results are statistically significant. The distributions of breakdown voltages and leakage currents at a bias voltage of 20 V are reported in Fig.4.46 for each completed DTC-4 batch. The breakdown voltage distribution reported in Fig.4.46(a) was found to be very uniform from batch to batch, with most average values ranging from 45 to 55 V. It can be observed that most strips can be considered good because they discharge occurs in this range of voltages. Only a part of the strips from the ATLAS09 seem to be more defective than the others, with breakdown voltages close to zero. It must be stressed that these tests highlighted the fact that even a single strip containing defects, can cause the entire sensor to be discarded because the total leakage follows the behavior of the weakest strip. This suggests that it is of paramount importance to be able to control and reduce the total amount of process induced defects. The distribution of the leakage currents of the strips measured at a bias voltage of 20 V (considered operation voltage) is reported in Fig.4.46(a). Most strip exhibit currents in the order of 2-6 nA (depending on the batch), corresponding to values of 6-18 pA/pixel.

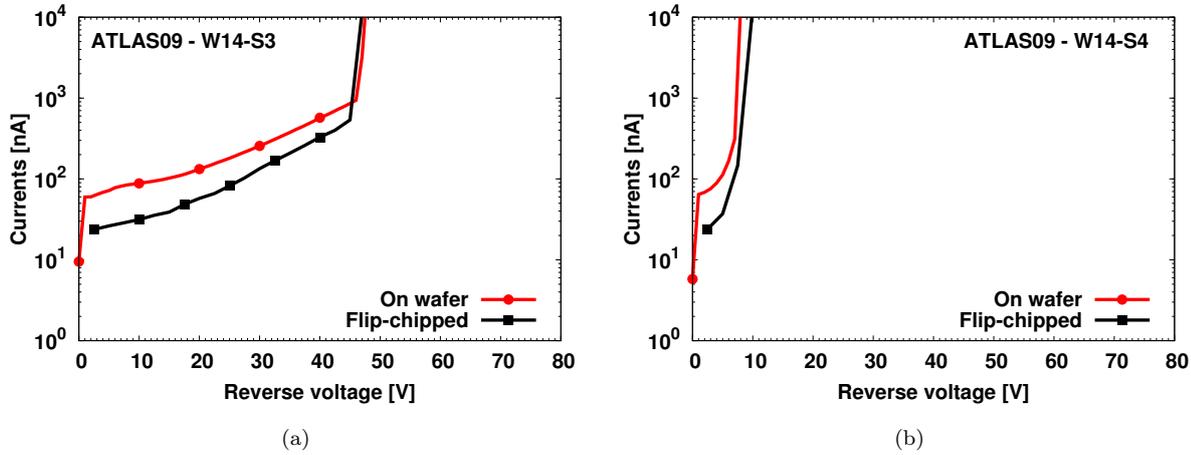


Figure 4.47: Comparison between on-wafer electrical tests and the same measurements repeated after flip-chip for two FE-I4 pixel detectors: a good sensor is shown in (a) and a bad sensor in (b).

These values are slightly larger than those measured on 3D diodes, this is believed to be caused by additional surface contributions (MOS effects) to the current added by the temporary metal layer. The number of strips exhibiting large values is rather contained, mainly for strips from the ATLAS09 batch, and is correlated to the low-breakdown strips observable in Fig.4.46(a). In the IBL production batches (ATLAS10-13) the amount of defective strips was much lower. The slope of the strip currents was found to be within the requested value of 2, and was never a major concern with respect to the other sensor requirements.

After the electrical tests are completed, the temporary metal is removed and the backside passivation is opened. This two steps do not affect the final quality of the wafers and this was demonstrated by measuring the sensor currents after bump bonding and flip-chip [124]. Fig.4.47 shows the comparison between before and after bump bonding currents measured on both a good (Fig.4.47(a)) and a bad sensor (Fig.4.47(b)). The good agreement between the two measurements demonstrates that the selection method is reliable and can be fully thrusted: the breakdown voltage is not affected at all and the current level slightly decreases probably because of a small stress release after cut and a different testing procedure. Moreover, these results also confirm that the sensor selection is able to correctly distinguish between good and bad sensors.

4.5 Post-irradiation electrical characterization of FBK devices

In order to fully qualify the newly developed 3D technology, it is crucial to demonstrate that sensor operation will be guaranteed even after heavy irradiation. In order to do so,

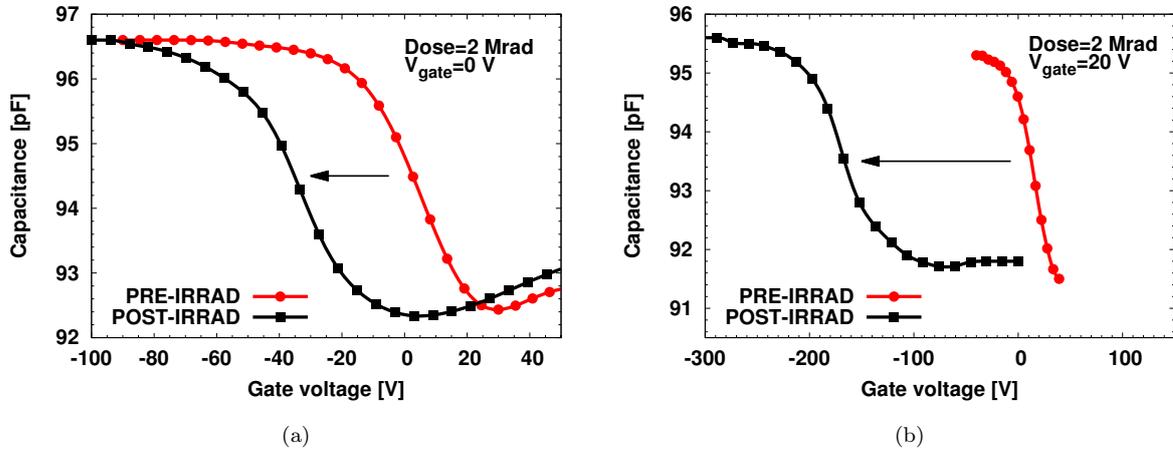


Figure 4.48: C-V measurements performed on MOS capacitor before and after irradiation without bias (a) and with 20 V bias (b).

the typical procedure is to irradiate the investigated devices with different kinds of high energetic particles and then replicate the electrical characterization.

The irradiation and testing of pixel detectors can be quite difficult because it is necessary to perform the bump-bonding, the irradiation and the final assembly to the readout system, considerably slowing the testing procedure. To this purpose 3D diodes are incredibly useful, after a quick on-wafer I-V to check their basic properties, they can be cut and sent to the irradiation facility. In addition, the assembly to the readout system is very easy, thanks to the fact that they only have two terminals and are quite small.

Different kinds of irradiations were performed on several types of 3D diodes and a summary of the obtain results is here reported.

4.5.1 Surface X-ray irradiation of planar test structures and 3D-diodes

Due to the very high p-spray dose needed to fully isolate the junction electrodes the measured breakdown voltages of 3D devices resulted to be rather low. In order to investigate how the increase in oxide charge caused by Ionizing Energy Loss in the SiO_2 layers affects the breakdown voltage and, therefore, the sensor operation, different runs of surface irradiations were performed on devices fabricated at FBK.

The irradiations were performed at Laboratori Nazionali di Legnaro (LNL), Padova, Italy, using a low energy X-ray tube able to the deliver a dose of roughly 2 Mrad in two hours. Using low energy X-rays assure to only damage superficial layers and not the bulk. Because of the well known amplifying effect of the bias voltage on irradiation effects (see Chapter 2 subsection 2.5.1), two different irradiations were performed: (i) without bias and (ii) with an applied bias voltage of 20 V. To monitor the modification of the basic

Table 4.13: Comparison between oxide charge values before and after irradiation, without (a) and with bias (b).

	Q_{ox} [cm^{-2}] (Unbiased)	Q_{ox} [cm^{-2}] ($V_{\text{bias}}=20$ V)
PRE-irradiation	1.82×10^{11}	8.67×10^{10}
AFTER 2 Mrad	1.17×10^{12}	3.91×10^{12}

technological parameters, the same irradiations were also performed on different planar test structures. In order to properly interpret the results on 3D diodes it is necessary to estimate the total accumulated charge during irradiation, and, to do so, C-V measurements on MOS capacitors were performed pre and post-irradiation. The results are shown in Fig.4.48. The measurement is performed by grounding the p^+ contact on the backside and sweeping the gate of the device while measuring the total capacitance. The main noticeable difference between the two cases is the much larger shift toward higher voltages for the device irradiated under bias (Fig.4.48(b)) with respect to the one irradiated without bias (Fig.4.48(a)).

These measurements allow to extract the final value of the oxide charge after irradiation. The results are reported in Tab.4.13 and compared to the values measured before irradiation. Before irradiation the charge concentration was well within the expected values for devices fabricated on $\langle 100 \rangle$ substrates and equal to roughly $1 \times 10^{11} \text{ cm}^{-2}$. After irradiation, the charge saturated to a rather low value when the bias was not applied, just a little above $1 \times 10^{12} \text{ cm}^{-2}$, while, with the bias applied, the final charge value was roughly 3.5 times larger, almost $4 \times 10^{12} \text{ cm}^{-2}$, possibly causing concerns for the inter-electrode isolation (the final charge was larger than the implanted p-spray dose, thus the concern). It is important to notice that these results are in almost perfect agreement with the theoretical expectations (see Fig.2.17). Keeping this result in mind, it should be noted that it is very important to perform irradiation under bias even on pixel and strip devices (if possible) when evaluating a new technology, in order to completely exclude any surface related issue after irradiation .

As far as the isolation was concerned, a specific test was performed on one of the irradiated test pads: on the front surface different n^+ regions are available, and it is possible to measure the surface resistance by trying to flow a current between them. This test was performed between the guard-ring of the planar diode and the guard-ring of the gated diode (number 5 and number 4 respectively in Fig.4.24). The inter-electrode resistance was estimated by simply applying Ohm's law and calculating $\Delta V / \Delta I$ over the investigated voltage range. In both cases the value of this resistance was found to range from hundreds of $M\Omega$ to $G\Omega$ thus confirming the proper isolation of the chosen p-spray

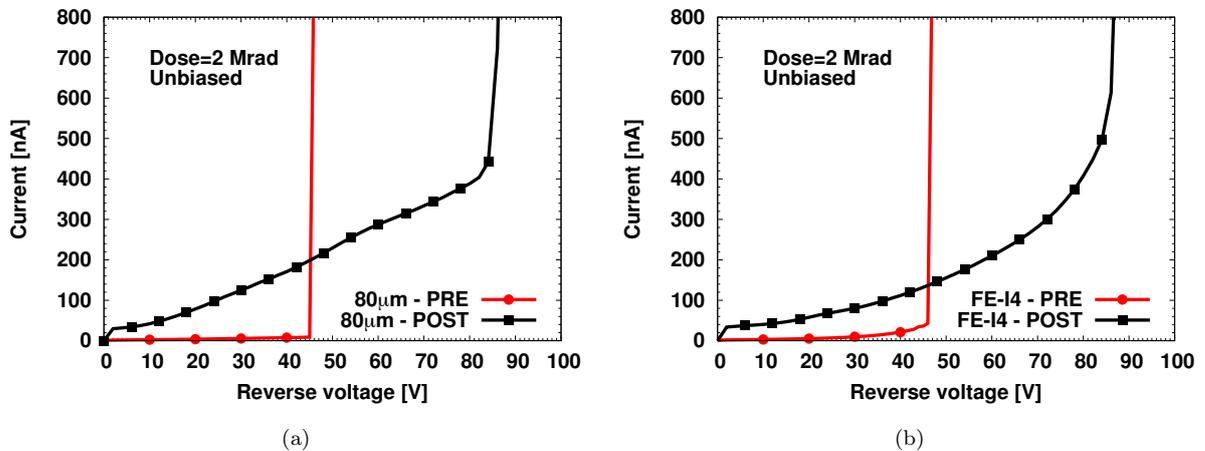


Figure 4.49: I-V measurements performed on two types of 3D diodes after X-ray surface irradiation without bias: 80 μm pitch diode (a) and FE-I4 diode (b).

implantation. The fact that the isolation is guaranteed even after the oxide charge reaches very large values can be explained by the fact that, while damaging the oxide, interface states are produced as well. These states behave as acceptors and increase the effective p-spray concentration helping to maintain the isolation.

Given the rather large increase in oxide charge, the increase in breakdown voltage for 3D diodes was expected to be large as well. I-V measurements were performed on all irradiated devices and compared with the pre-irradiation results.

Fig.4.49 shows the measurements performed on an 80 μm pitch diode (Fig.4.49(a)) and an FE-I4 diode (Fig.4.49(b)) before and after irradiation without bias. The increase in breakdown voltage is noticeable on both devices and is in the range of roughly 40 V, but is actually lower than expected. This fact is well understood and was previously described using numerical simulations in subsection 4.4.2: 3D devices with fully passing through columns exhibit two electric field peaks, one on each wafer side, caused by the high p-spray concentration. By irradiating only the front surface it is possible to get rid of the problem only on the front-side and the final breakdown voltage remains rather low.

The described effect was also confirmed after irradiation under bias (Fig.4.50) for the same diode types. Having a much larger oxide charge one would expect to have a greater compensation of the p-spray layer and thus a much larger breakdown voltage. This does not happen because the maximum operating voltage is again limited by the n^+ column to p-spray junction on the backside. In fact, although the oxide charge in this second case was much larger, the increase in breakdown voltage was even lower, in the order of 30 V. In order to ultimately prove this theory, an irradiation under bias on both devices sides is planned for the beginning of 2013.

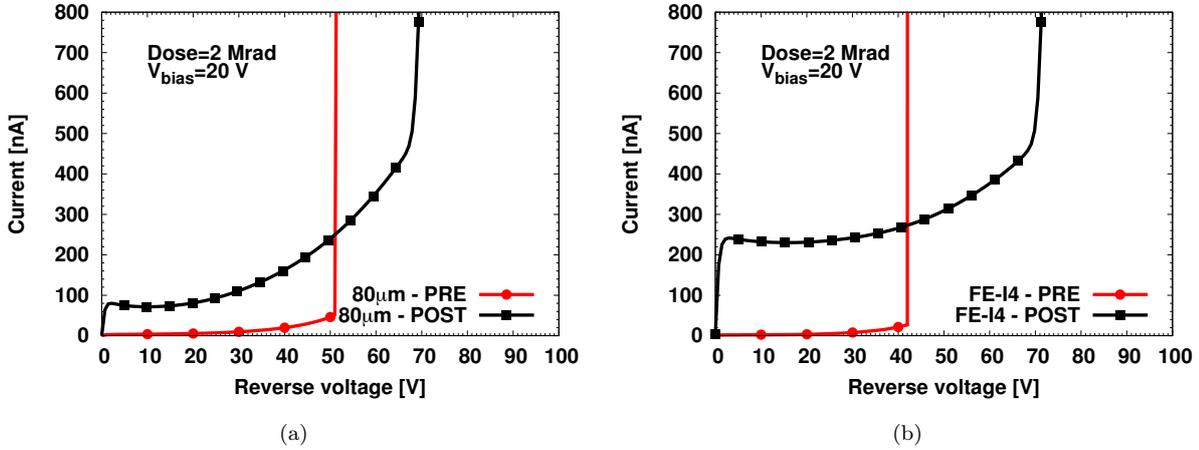


Figure 4.50: I-V measurements performed on two types of 3D diodes after X-ray surface irradiation with 20 V of applied bias: 80 μm pitch diode (a) and FE-I4 diode (b).

In addition, devices irradiated under bias show a larger current value at low biases. This is to be ascribed to the increased surface recombination velocity caused by the radiation damage, which is also increased when the irradiation occurs under bias (see Fig.2.17).

4.5.2 Proton irradiated 3D-diodes

In order to also evaluate the effects of the bulk damage on device operation, an irradiation with 800 MeV protons was performed at the Los Alamos Irradiation facility, on a large amount of 3D diodes with different geometrical implementation. The requested fluences spanned from very low values ($5 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$) up to vary larger values ($1 \times 10^{16} \text{ n}_{eq}/\text{cm}^2$). The irradiation dose was chosen considering the different geometrical implementations of the devices: sensors with larger inter-electrode distance were set to receive lower fluences in order to be sure to still be able to operate them after irradiation (e.g. the CMS diodes in 1E configuration having an inter-electrode distance of $\sim 90 \mu\text{m}$, were irradiated only up to $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$).

Because of some difficulties during the irradiation, only half of the requested dose could be delivered. A total summary of irradiated devices and requested/received fluences is reported in Tab.4.14.

The irradiation was performed without bias. The total number of irradiated devices was larger but some were damaged during irradiation and others were sent to University of New Mexico that volunteered to help with the testing. The number of measured devices is anyhow sufficient to obtain good statistics.

After irradiation, devices were kept frozen while waiting for their activity to decrease

Table 4.14: Summary of the devices irradiated at Los Alamos with 800 MeV protons. Devices type, wafer and batch of origin are also reported together with the requested and received fluences.

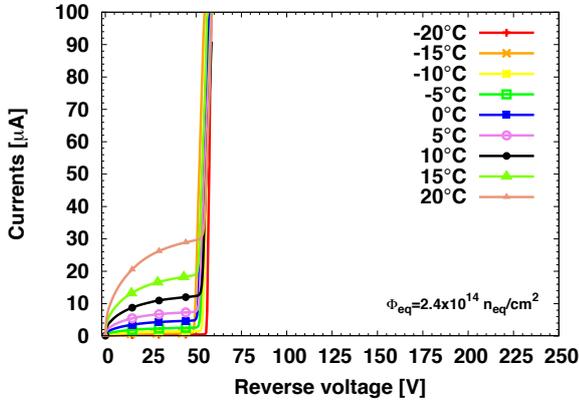
Batch	Wafer #	Device type	Device #	Requested fluence [n _{eq} /cm ²]	Received fluence [n _{eq} /cm ²]
ATLAS10	W14	CMS	D1	5 × 10 ¹⁴	2.4 × 10 ¹⁴
ATLAS10	W14	CMS	D2		
ATLAS10	W12	CMS	D3	1 × 10 ¹⁵	5.2 × 10 ¹⁴
ATLAS10	W12	CMS	D4		
ATLAS10	W14	CMS	D5		
ATLAS10	W14	CMS	D6		
ATLAS10	W14	80 μm	D10		
ATLAS10	W14	80 μm	D11		
ATLAS10	W14	80 μm	D12		
ATLAS10	W12	FE-I4	D1		
ATLAS10	W12	FE-I4-FP	D2		
ATLAS10	W12	FE-I4-FP	D8		
ATLAS10	W12	FE-I4-FP	D9		
ATLAS10	W12	FE-I4	D10		
ATLAS10	W14	80 μm	D7		
ATLAS10	W14	80 μm	D8		
ATLAS10	W14	80 μm	D9		
ATLAS10	W14	80 μm	D4	1 × 10 ¹⁶	4.2 × 10 ¹⁵

within safety levels. The devices were then glued and wire bonded to some home-made PCBs designed to ease the testing. In order to avoid annealing effects, the wire bonding was performed at room temperature.

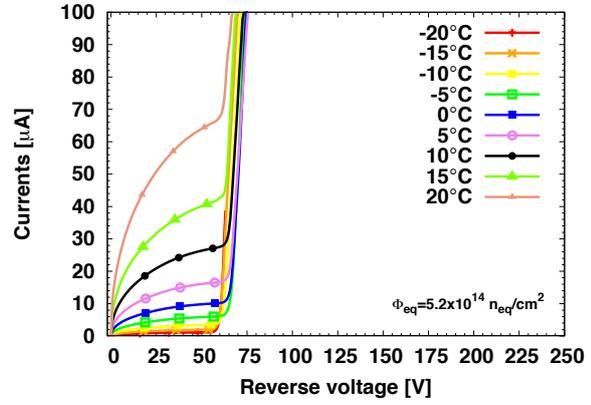
The testing procedure is very similar to the one described in the previous sections for un-irradiated devices: an HP4145 semiconductor parameter analyzer is used together with a climatic chamber.

Due to the large number of available devices only a subset of results are here shown and discussed. The only device irradiated at 4.2×10^{15} n_{eq}/cm² (W14 80 μm D4) stopped working after the very first measurement so not enough data are available to draw reliable conclusions. Preliminary data extracted from the only available measurement taken at -20 °C will be discussed anyway.

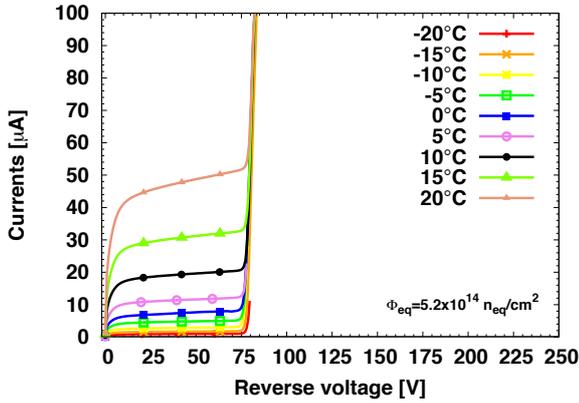
Fig.4.51 reports all the I-V measurements performed at different temperatures for at least one device irradiated at each available fluence: the top row (Fig.4.51(a) and Fig.4.51(b)) refers to CMS diodes, the middle row (Fig.4.51(c) and Fig.4.51(d)) refers to 80 μm pitch diodes and the bottom row (Fig.4.51(e)) refers to an FE-I4 diode. Notice



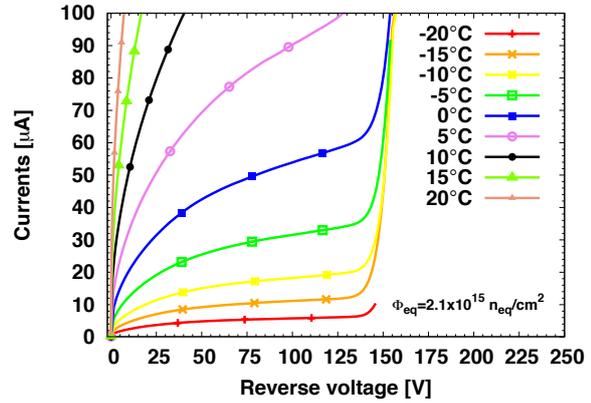
(a) W14 CMS D2 - $\Phi_{eq} = 2.4 \times 10^{14} \text{ neq/cm}^2$



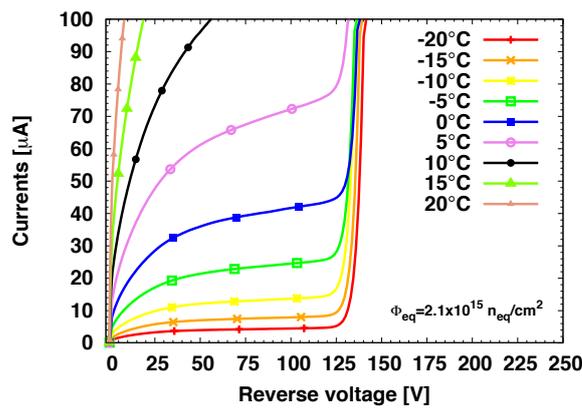
(b) W14 CMS D6 - $\Phi_{eq} = 5.2 \times 10^{14} \text{ neq/cm}^2$



(c) W14 80 μm D10 - $\Phi_{eq} = 5.2 \times 10^{14} \text{ neq/cm}^2$



(d) W14 80 μm D8 - $\Phi_{eq} = 2.1 \times 10^{15} \text{ neq/cm}^2$



(e) W12 FE-I4-FP D9 - $\Phi_{eq} = 2.1 \times 10^{15} \text{ neq/cm}^2$

Figure 4.51: Summary of the I-V measurements performed on a subset of 3D diodes irradiated with 800 MeV protons at different fluences. Device type and irradiation fluence are reported under each image for better clarity

Table 4.15: Summary of the most important electrical parameters measured on irradiated devices. Device type and received fluence are report along with: intrinsic breakdown voltage estimated from pre-irradiation measurements and simulations (V_{BD-PRE}), measured breakdown voltage after irradiation ($V_{BD-POST}$) at -20°C , reverse current density after irradiation for a common voltage of -55 V at a temperature of -20°C and calculated damage constants (α).

Device	Φ_{eq} [n_{eq}/cm^2]	V_{BD-PRE} [V]	$V_{BD-POST}$ [V]	$I(-55\text{V}, @-20^\circ\text{C})$ [$\mu\text{A}/\text{cm}^2$]	α [A cm]
W14 CMS D2	2.4×10^{14}	40.6	56.44	6.29	5.07×10^{-17}
W14 CMS D6	5.2×10^{14}	40.6	63.17	14.15	5.27×10^{-17}
W14 $80\mu\text{m}$ D10	5.2×10^{14}	52.3	77.56	10.02	3.73×10^{-17}
W12 FE-I4-FP D9	2.1×10^{15}	46.5	130.75	43.55	4.01×10^{-17}
W14 $80\mu\text{m}$ D8	2.1×10^{15}	52.3	145.9	51.18	4.72×10^{-17}
W14 $80\mu\text{m}$ D6	4.2×10^{15}	52.3	>200	54.42	2.53×10^{-17}

that device name and fluence are reported under each plot for the sake of clarity. To completely follow the discussion, the most important parameters recalled in the text are summarized in Tab.4.15 and are: the device type and name, the received fluence, the intrinsic breakdown voltage estimated from pre-irradiation measurements and simulations, the measured breakdown voltage after irradiation at -20°C , the reverse current density after irradiation for the highest possible reverse voltage of -55 V common to all devices at a temperature of -20°C , and the calculated damage constants.

A clear trend is observable for currents and breakdown voltages with respect to the received fluence, both between same type devices and even across sensors of different types. Unfortunately, since only one fluence was available for the FE-I4 type devices, the fluence dependence could not be completely studied.

Starting the analysis from CMS devices (Fig.4.51(a) and Fig.4.51(b)), only two rather low fluences were available and in fact, the increase in breakdown voltage was rather small with respect to the intrinsic breakdown voltage pre-irradiation of 40.6 V . For the device irradiated at $2.4 \times 10^{14} n_{eq}/\text{cm}^2$ the breakdown occurred at 56.44 V while for the one irradiated at $5.2 \times 10^{14} n_{eq}/\text{cm}^2$ the reverse discharge happened at 63.17 V . This low increase is caused by the small accumulated oxide charge due the low fluence. The damage related leakage current increase is coherent with the received fluence, and the calculated damage constants of about $5 \times 10^{-17} \text{ A cm}$, are in agreement with the expected values. The current trend with temperature is comparable with what observed pre-irradiation and, before the manifestation of breakdown phenomena, it shows a purely SRH behavior.

3D diodes with $80\mu\text{m}$ pitch between column of the same doping type, were irradiated at two different fluences as well: 5.2×10^{14} (Fig.4.51(c)) and $2.1 \times 10^{15} n_{eq}/\text{cm}^2$ (Fig.4.51(d)).

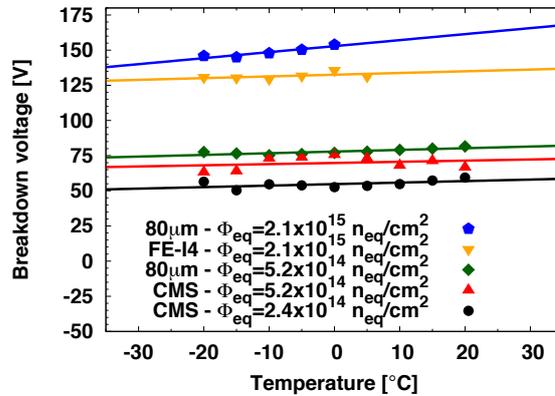


Figure 4.52: Summary of the measured breakdown voltages for each considered device at each fluence as function of the temperature.

The larger increase in breakdown voltage is evident: the device irradiated at the lower fluence reaches a maximum operating voltage of roughly 80 V, while the one at the larger fluence exceeds 150 V. The current saturation is reached relatively easily for both devices at -20°C , showing that the breakdown voltage is sufficiently high to operate the sensors at the optimal bias even after irradiation. The current trend with temperature is consistent with the expected SRH behavior and the calculated damage constants still fall within the expected value range. It is important to notice that, comparing the CMS and $80 \mu\text{m}$ devices irradiated at the same fluence of $5.2 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$ the difference in breakdown voltages (roughly 10 V larger for the $80 \mu\text{m}$ diode) is consistent with what observed in pre-irradiation and described in the previous section. The difference in current density is not very large and it might be caused by a uncertainties in the final delivered dose.

Only one fluence is available for the FE-I4-FP type diodes, $2.1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ (Fig.4.51(e)). The behavior of the device is fully coherent with what just described for the other two types. The only difference can be extracted by comparing the measurements in Fig.4.51(e) with those coming from the $80 \mu\text{m}$ diode irradiated at the same fluence and reported in Fig.4.51(d): the absolute value of the current is very similar but the breakdown voltage is about 15 V larger for the $80 \mu\text{m}$ device. This can again be ascribed to the different device layout and is in complete agreement with what observed pre-irradiation, the differences are amplified by the radiation damage.

The only measurement available for the $80 \mu\text{m}$ diode irradiated at the highest fluence of $4.2 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ did not show any breakdown before 200 V and the current density value was rather low. The damage constant is not far from the expected values.

In order to better visualize the breakdown voltages as a function of temperature and received fluence for each device, the results are plotted in Fig.4.52. The expected

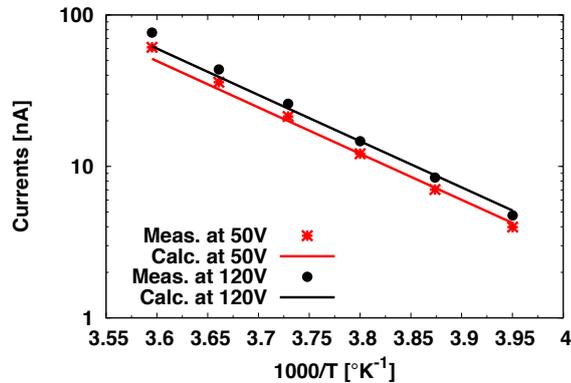


Figure 4.53: Comparison between measured (symbols) and calculated (solid lines) values of leakage current at two different bias voltages (50 V) and (120 V) for the FE-I4 diode irradiated at $2.1 \times 10^{15} n_{eq}/\text{cm}^2$.

trend, both in terms of fluence and temperature, is respected. Some uncertainties in the measurements are caused by a difficult temperature control in the climatic chamber, which requires very long times to stabilize.

The current behavior with respect to the temperature was studied for each device in the same way as for un-irradiated sensors in the previous section. For the sake of conciseness only one result is here reported in Fig.4.53 for the FE-I4-FP device irradiated at $2.1 \times 10^{15} n_{eq}/\text{cm}^2$, and it is fully representative of what found for all other devices. The current trend with temperature follows the expected SRH behavior even for large voltages. This is the confirmation that no anticipated breakdown effects are present.

The described characterization gave important informations and is fully representative of what it should be expected to see on strip and pixel devices. Numerical simulations are underway in order to try to understand the full meaning of the measurements. The main difficulty about simulations is the proper modeling of surface effects (oxide charge and interface states) for which a comprehensive model is not available yet for p-spray isolated n-in-p sensors. A basic model was put together by collecting different values found in literature but it is still very "primitive" and is not fully verified yet.

In addition, a large set of 3D diodes was irradiated with reactor neutrons at the Jozef Stefan Institute, Ljubljana, Slovenia. Devices are currently kept frozen waiting for the activity to decrease enough to allow for their assembly.

4.5.3 Proton irradiated FE-I4 pixel detectors

A very basic electrical characterization was performed on some of the FBK pixel detectors bump-bonded to the FE-I4 readout chip and irradiated at different fluences [113, 135]. As an example, the I-V measurements on a pixel assembly irradiated with 25 MeV protons at

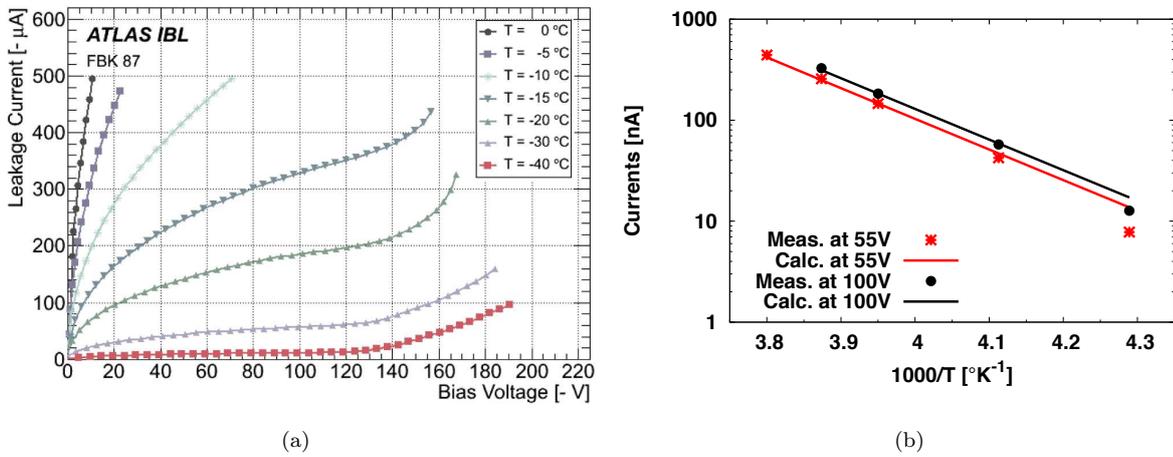


Figure 4.54: Reverse current as a function of the applied bias and the temperature [113] (a) and comparison between measured and calculated current values for two different bias voltages as function of the temperature (b).

the Karlsruhe Institute of Technology (KIT) at a fluence of $5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$, are reported in Fig.4.54(a). The assembly was placed inside a climatic chamber and the temperature was varied from 0 to -40°C . The acquisition of the reverse current was performed through the USBpix system. The breakdown voltage after irradiation reached values between 160 and 180 V depending on the temperature. Comparing this value with what found on 3D diodes, it is roughly 30 V larger than for the diode irradiated at a fluence of $2.1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$, consistently with the higher received fluence. The reverse current has a very similar trend to what found on 3D diodes, and Fig.4.54(b) shows the measured (symbols) versus the calculated (lines) values of leakage current for the considered device biased at two different voltages. This plot suggests that, also in this case, the current behavior is purely SRH. The sensor leakage current was also found to be stable with time.

In addition, a summary of the currents and power dissipation for many of the 3D pixel detectors irradiated with 25 MeV protons is reported in Fig.4.55 as a function of fluence and temperature. The reported values are well within IBL specifications, and in particular, since 3D detectors can be operated at relatively low voltages ($\sim 160\text{V}$) even after heavy irradiation, the measured power dissipation is about a factor of 10 lower than the imposed maximum limit.

As will be explained later, all the breakdown voltages found in this analysis, both for 3D diodes and for pixel detectors, are sufficiently high to assure an efficient charge collection, while the reverse currents do not affect the noise too much.

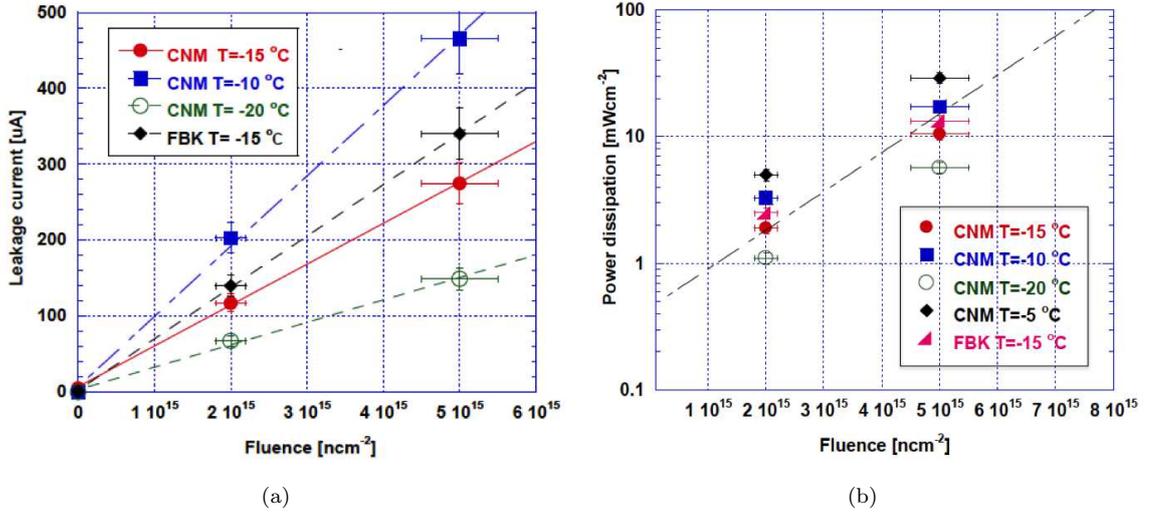


Figure 4.55: Leakage current (a) and power dissipation (b) as a function of irradiation fluence and temperature for 3D pixel detectors irradiated with 25 MeV protons. CNM devices are also reported for comparison [135].

4.6 Functional characterization of FBK devices

The functional characterization of 3D sensors fabricated at FBK was performed in different laboratories and facilities around the world and will be described in this section starting from simple 3D diodes, moving to strip detectors and finally discussing the results obtained with both ATLAS FE-I4 and CMS PSI46V2 pixel assemblies.

4.6.1 3D-diodes

The functional characterization of 3D diodes was mostly focused on the slim-edge and was performed at University of Trento by means of laser scans of the edge area. The laser scan setup is mainly composed by Thorlabs equipment: (i) two Z712B motors, (ii) two TDC001 servo motor controllers, (iii) a translational stage and (iv) a KT112 to couple the laser diode to an optical fiber. The laser is focused onto the device by means of a snap on focuser from Optics For Research (OFR, FFC-8/5-λ) and the minimum achievable spot diameter is roughly 11 μm. An home made driver provides pulses in the hundreds of picoseconds range. The readout is composed by a Cremat CR-111 Charge Sensitive Amplifier (CSA) and by an home made gaussian shaper with a peaking time of 20 ns. Data are acquired by means of a Tektronix TDS3052B oscilloscope and a Matlab software that also controls the automatic positioning of the motors. The positioning precision is in the order of 1 μm and different laser wavelengths are available. Pictures of the entire setup are shown in Fig.4.56 highlighting each component of the setup.

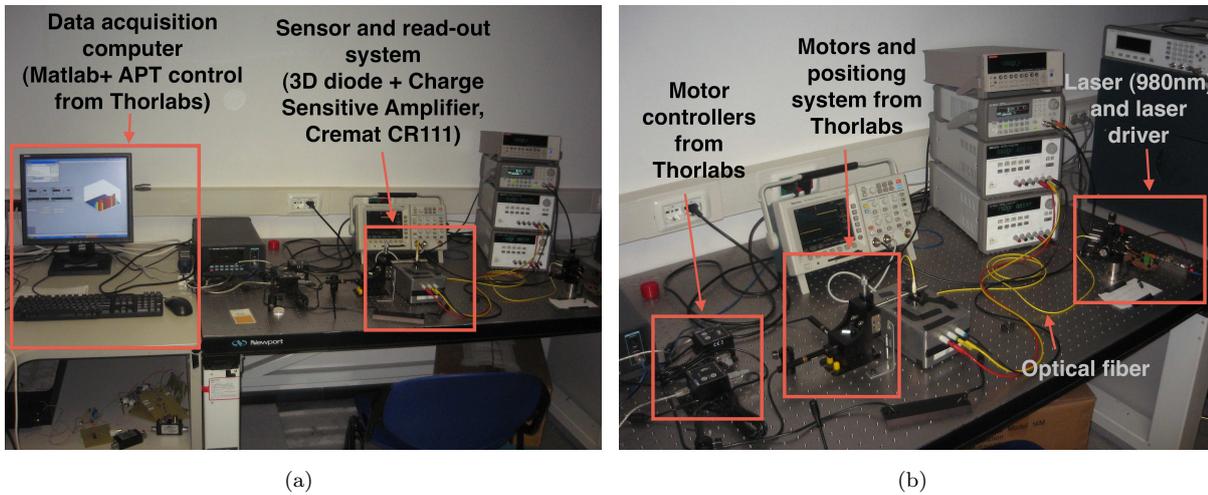


Figure 4.56: Laser scan setup available at University of Trento, each component is highlighted in the pictures.

The schematic of the readout system is reported in Fig.4.57. The bias is provided to the detector after a proper filtering (low-pass composed by R1, C1 and R2). Positive voltage is applied to the n-side while keeping the p-side grounded. In order to be sure that the bias voltage is not directly applied to the input node of the CSA, the sensor is AC coupled through C2. This also prevents the leakage current to flow into R_f causing DC offset on the output node. The CSA is a CR-111 from Cremat, the integrating element C_f is discharge by means of the resistor R_f with a time constant $\tau=R_f C_f$. Like in every CSA the output voltage is proportional to the input charge following the relationship $\Delta V_{out}=\Delta Q_{in}/C_f$. The shaping amplifier takes the CSA output and gives it a gaussian shape with a 20 ns peaking time, without affecting the proportionality of the signal amplitude to the input charge.

The possibility of precisely control the laser position allows to study the sensor response in many different positions finally obtaining a 2D signal efficiency map of the scanned area. This setup was mainly used with 3D diodes to investigate how much of the slim-edge area is active, in order to understand if a reduction of its extension was possible. In addition some preliminary tests were performed on different 3D diodes to estimate the effects of the bias voltage on the signal efficiency.

The slim-edge was thoroughly investigated with numerical simulations but was never functionally tested. In order to have an idea of what to expect on pixel sensors, a laser scan of the edge region of a FE-I4 3D diode was performed. The results reported in Fig.4.58 were obtained with a bias voltage of 15 V and a step of 10 μm in the x and y directions. The laser wavelength was 1060 nm, sufficient to generate charge along the entire bulk

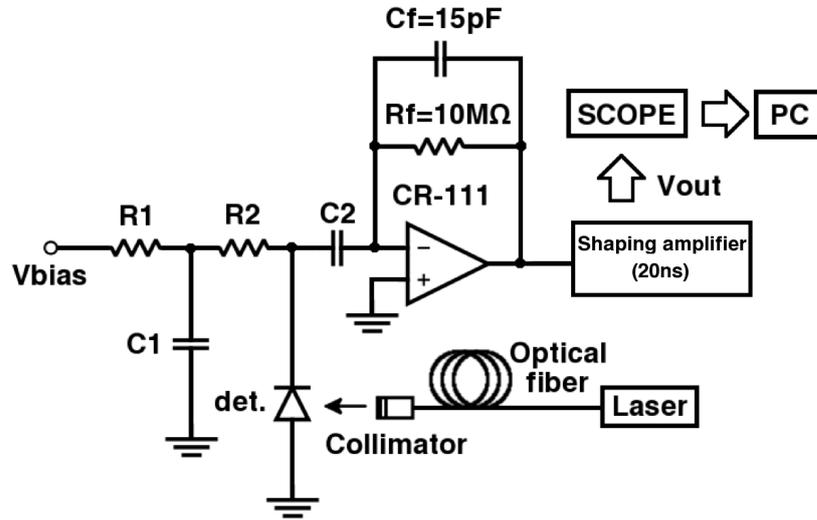
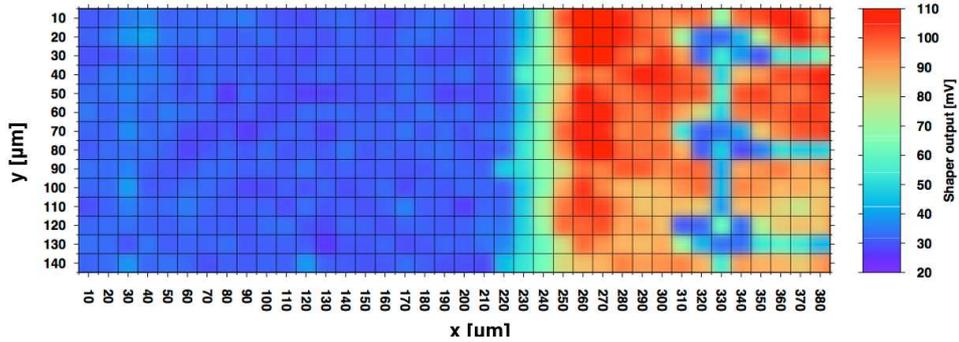


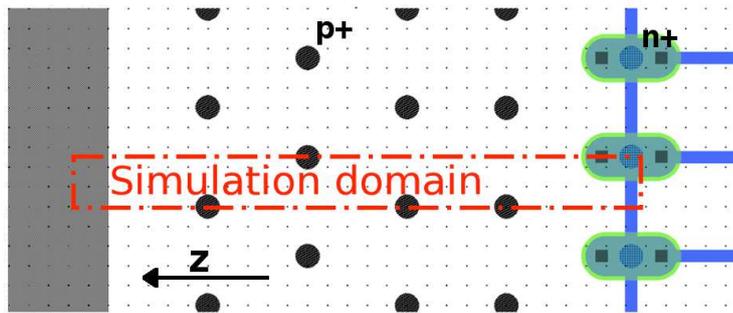
Figure 4.57: Schematic of the readout system available in the laser scan setup at University of Trento.

thickness. The scanned area is $380 \times 140 \mu\text{m}^2$, the long pixel side is oriented to be parallel to the x axis, which also correspond to what would be the z direction inside ATLAS. In the laser scan result in Fig.4.58(a) the metal pattern in the active-area is clearly visible (the laser is reflected), and the extension of the active sensor region is recognizable. A little blurring of the image is present because of the rather large spot size and a not perfect alignment with the laser beam. The applied bias voltage is well above the full depletion of the sensor. By using a 20 ns peaking time it is possible to consider only those carriers that are generated inside the depleted region and reach the readout electrodes in a sufficiently fast time. This result suggested that a good portion of the sensor slim-edge is also active, corresponding to roughly $50 \mu\text{m}$ outside the last ohmic column of the active area. This is also confirmed by the simulation reported in Fig.4.58(c) where it is possible to see the extension of the depleted region inside the sensor. The agreement with measurements is remarkably good. This result is very interesting because it confirms that the slim-edge extension in the z direction could be further reduced to roughly $100 \mu\text{m}$, with respect to the current $200 \mu\text{m}$, as previously observed in the electrical characterization (see Fig.4.36 in subsection 4.4.2).

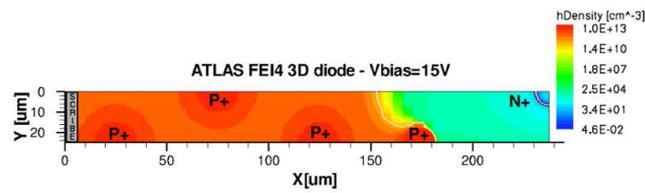
The same laser scan was also performed on an $80 \mu\text{m}$ pitch 3D diode and the results are shown in Fig.4.59 [128]. The size of the scanned region was $370 \times 170 \mu\text{m}$ and the scan step was $10 \mu\text{m}$. The applied bias voltage was again 15 V. The metal pattern is clearly visible in the 2D map (Fig.4.59(b)) and by comparing the result with the layout in Fig.4.59(c), it is again confirmed that the depletion region is stopped by the second row of ohmic columns of the slim-edge. Two 1D cuts of the signal distribution are extracted



(a)

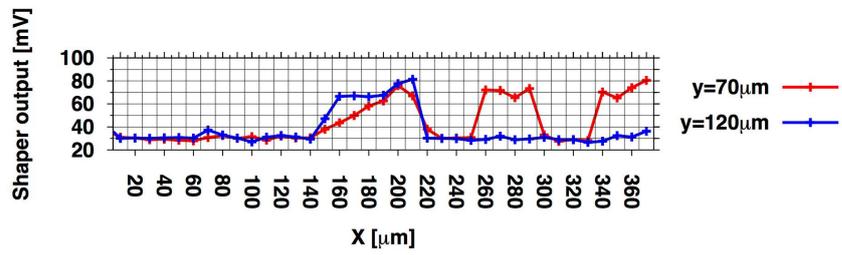


(b)

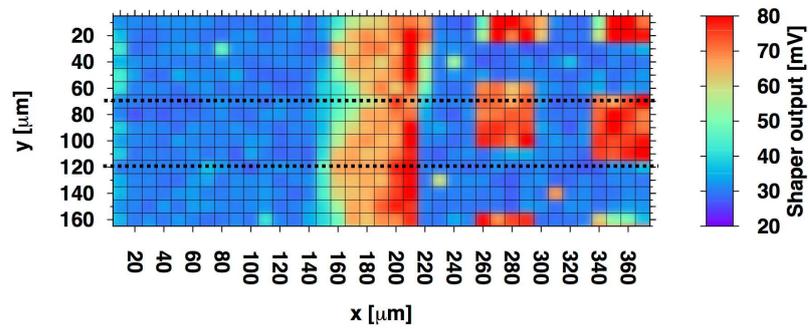


(c)

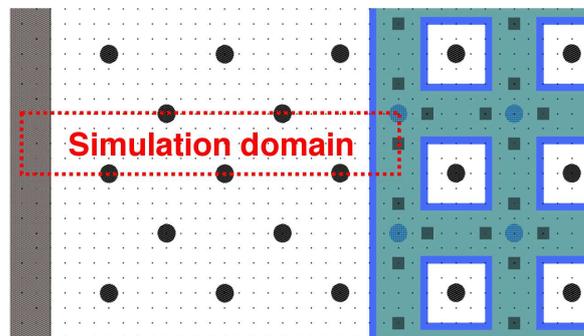
Figure 4.58: Laser scan of the edge region of an FE-I4 3D diode using a 1060 nm laser, for an applied bias of 15V. The scan result (a) is compared with the layout of the scanned area (b) and the simulated hole density for the considered bias voltage (c) [125].



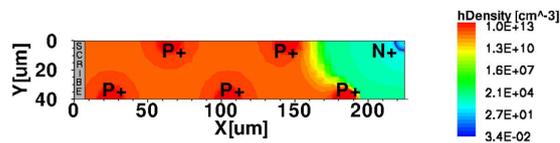
(a)



(b)



(c)



(d)

Figure 4.59: Position resolved laser scans ($\lambda=1060$ nm) on the edge region of an $80 \mu\text{m}$ 3D diode for a bias voltage of 15 V compared with numerical simulations: 1D signal cuts at $y=70$ and $y=120 \mu\text{m}$ (a), 2D signal map (b), layout of the scanned area (c) and simulated hole density along a plane perpendicular to the columnar electrodes showing the extension of the depletion region [128].

for $y=70$ and $y=120$ μm (Fig.4.59(a)), the latter position not showing any signal inside the active area because of the metal reflection. The simulated hole density reported in Fig.4.59(d) is again in very good agreement with the measured signal, stopping at the second row of ohmic columns.

Additional laser tests were also performed inside the active area of several 3D diodes covering an area the size of a single pixel in order to investigate the uniformity of the response for different bias voltages. The results reported in Fig.4.60 show the laser scan performed on a CMS 3D diode in 1E configuration coming from the ATLAS07 batch. Two different bias voltages were considered, 2.5 and 5 V. It was not possible to further increase the applied voltage due to early breakdown of the sensor. The diode layout is also reported for comparison. The effect of the bias voltage on the 2D map uniformity is clearly visible, with the signal distribution being much more uniform for a bias of 5 V. It is important to notice that, at this voltage, full depletion is not reached yet thus some lower efficiency regions are still present. These less efficient regions are located between two electrodes of the same doping type, and, in particular, the collection efficiency is much lower between p^+ columns, in good agreement with the expectations. Although the laser alignment is not perfect and the spot size rather large, it is possible to see that the left part of the pixels appears to be more efficient. This is caused by a misalignment of the metal with respect to the columnar electrodes which was caused by the very large wafer bowing measured in the ATLAS07 batch.

Additional laser tests are planned on irradiated 3D diodes and the setup is currently being adapted to add temperature control capabilities. This will require some time because the positioning system cannot be fit inside the climatic chamber thus the possibility of using Peltier modules for cooling is under study.

Meanwhile, radioactive source measurements will be performed on 3D diodes thanks to the newly acquired ^{90}Sr source. The beta particle system is compatible with the size of the climatic chamber, thus allowing to also measure irradiated devices.

4.6.2 Strip detectors

The functional characterization of 3D strip detectors previously described in subsection 4.4.3, was performed at the University of Freiburg by means of radioactive source and laser scans [132]. Both measurement setups are based on the ALIBAVA system, featuring a 25 ns shaping time [133]. The β -particle setup makes use of a 37 MBq $^{90}\text{Sr}/\text{Y}$ radioactive source to investigate the sensor response to MIP particles. The triggering is performed with two scintillators in coincidence placed behind the device under test, in order to only readout MIP-like events relative to ^{90}Y decays (maximum energy of 2.28 MeV). The laser scan setup uses a position resolved infrared pulsed laser ($\lambda=974$ nm) with pulses shorter

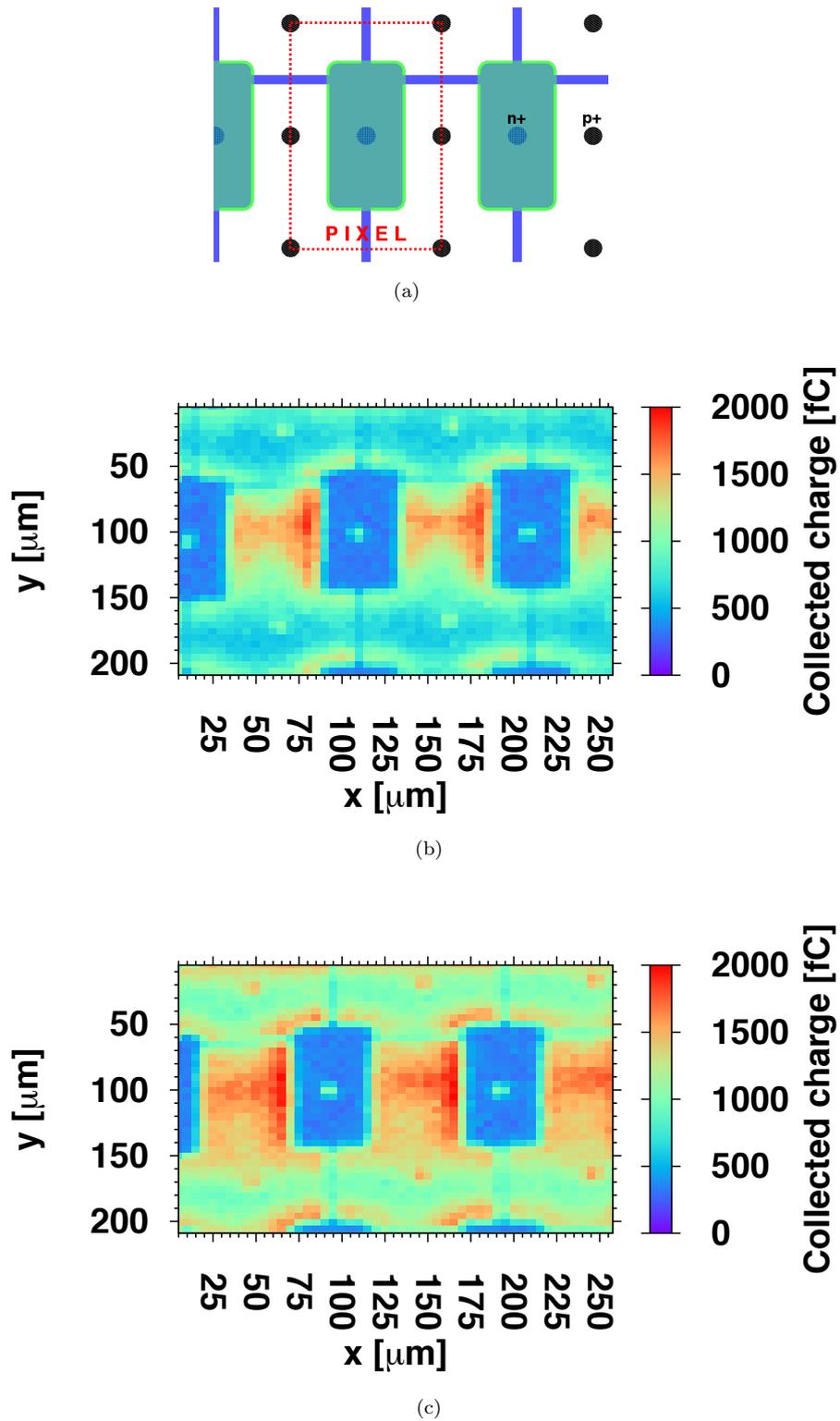


Figure 4.60: Position resolved laser measurements ($\lambda=1060$ nm) performed on a CMS 3D diode in 1E configuration coming from the ATLAS07 batch. The diode layout is also reported (a) and the two scan results refer to bias voltages of 2.5 V (b) and 5 V (c).

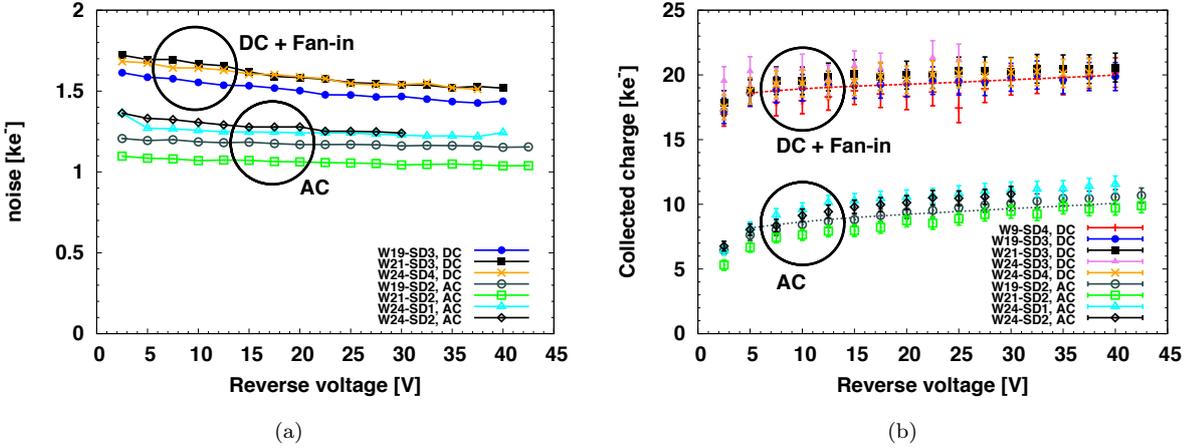


Figure 4.61: Noise figure as a function of the bias voltage for the investigated sensor (a) and relative collected charge in response to β particles as a function of the applied bias (b) [132].

than 1 ns, to investigate the detector signal efficiency on the scanned area. The laser is fed through an optical microscope (Leica Polyvar SC) by means of a 1 m long optical fiber, and is focused on the front side of the sensor. The trigger for the laser is provided from the ALIBAVA system. The laser profile has a gaussian spatial distribution with a diameter of about $4 \mu\text{m}$. The sensor is mounted on a cooling structure that can be moved in both x and y directions, with a precision of approximately $1 \mu\text{m}$ by motorized stages remotely controlled via software.

Because of the concerns raised by the value of the coupling capacitor during the electrical characterization (see subsection 4.4.3), it was suggested to connect the detectors in two different configurations: (i) using the integrated AC coupling capacitors and (ii) using the DC pads in combination with external RC fan-ins. This was done to assure that, even if predictions about the low signal transmission efficiency of AC coupled devices were going to be confirmed, significant results could also be acquired with the other assembly configuration. The value of the components in the RC fan-ins are: $R=1 \text{ M}\Omega$ and $C=275 \text{ pF}$.

As previously mentioned, the investigated strip sensors come from the IBL production batch ATLAS10, and more specifically wafers 9, 19, 21 and 24. Sensors will, from now on, be referred to with a unique identifier composed by the wafer number followed by the sensor number on the wafer.

Once the sensor assembly was completed, a noise scan was performed on all available strips sensors. The noise of the system was measured as a function of the bias voltage and was found to be ranging between 1 and 2 ke^- for most of the devices. Out of a total of 9 sensors, only two showed high noise values (in the order of 5-6 ke^- for W9-SD4 and

W24-SD3), caused by premature breakdown effects. As will be shown later, high noise values did not affect the sensor performance. Fig.4.61(a) reports the noise scan results for all the sensors with low noise values. Devices assembled using DC pads showed a slightly larger noise figure than sensors assembled using the AC pads. This effect is explained by the fact that, when strips are biased using the punch-through mechanism (i.e. using AC pads), a contribution to the noise of the system is given by the punch-through current flowing toward the bias line, which is equal to the noise contribution of the leakage current and, being the two processes independent, it adds quadratically to it (with a current noise spectral density of $2qI_{strip}$) [134]. When DC pads are used in combination with an external fan-in, a parallel noise term is added by the external $1\text{ M}\Omega$ resistor, contributing to the overall noise with a current noise spectral density of $4kT/R$. Being the latter contribution larger, it results in a larger noise figure for this configuration. A further decrease in the noise figure of devices using the AC pads comes from the low value of the integrated capacitor, which causes the noise (as well as the signal) to redistribute over the parasitic capacitances. The overall noise for both configurations decreases slightly with respect to the bias voltage but it is almost flat, consistent with the shape of the C-V measurement showed in Fig.4.42(a) and confirming that full depletion occurs at very low biases.

Charge collection results obtained in response to β -particles are reported in Fig.4.61(b). The expected collected charge in a $230\text{ }\mu\text{m}$ thick silicon sensor in response to a MIP, is equal to roughly 18.4 ke^- . Two distinct families of curves are identifiable. Devices assembled using DC pads and external fan-ins, exhibit charge saturation before 10 V of bias and a maximum collected charge slightly larger than expected ($\sim 20\text{ ke}^-$). This can be attributed to uncertainties on the wafer thickness ($\pm 20\text{ }\mu\text{m}$) and to particles impinging the device with angles different from 90° , thus traveling longer distance in the bulk and generating more charge inside the device. As previously mentioned, also noisy sensors (W9-SD4 and W24-SD3) exhibit full charge collection.

As forecasted, assemblies using the integrated coupling capacitor did not show the same performances. The collected charge corresponds to roughly half of the charge collected by other sensors. The investigation of this phenomena was performed by means of Spice simulations including all the measured electrical parameters, also implementing the AC coupling capacitor and the readout input capacitance. The simulated schematic modeling the first stage of the readout system is reported in Fig.4.62(a). The strip is modeled with a pulsed current generator with the strip to back capacitance in parallel. The charge collected by the DC coupled sensors was injected into the circuit by means of short current pulses ($Q_{in}=di/dt$). The readout is modeled with a simple integrator (CSA) consisting of an ideal operational amplifier with an RC feedback. The sensor assemblies using the RC fan-ins were simulated by including the proper fan-in values into the circuit.

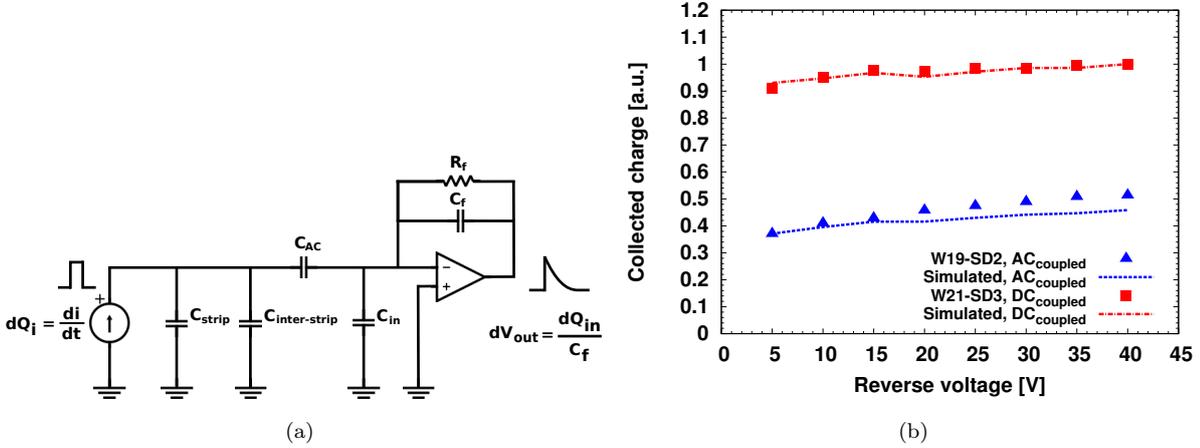


Figure 4.62: Spice simulation schematic (a) used to estimate the effect of the AC coupling capacitor on charge collection for AC coupled strip sensors and corresponding results (b).

Simulation results are reported in Fig.4.62(b) together with measured data and show very good agreement. Being the coupling capacitor almost comparable with the parasitic capacitances, the signal charge is not efficiently transferred to the readout circuit and part of it is lost. This confirms that, in the case of 3D detectors, the AC coupling through an integrated capacitor is rather difficult and other assembly methods like RC fan-ins should be considered.

An extracted Landau fit and cluster size distribution for an applied bias voltage of 15 V, are reported in Fig.4.63, and are fully comparable to those found on FE-I4 pixel detectors coming from the same batch, as will be shown in the next subsection. This confirms that charge sharing in 3D detectors is lower than in standard planar devices because of their intrinsic self shielding between different elementary cells.

Laser scans for different sensors and different biases were also performed. In particular, two laser scans for a DC coupled sensors using RC fan-ins and for two different biases, 2 V and 30 V, are reported in Fig.4.64(a) and Fig.4.64(b) respectively. The scanned area corresponds to a region of $100 \times 100 \mu\text{m}$, one junction electrode per corner is present and an ohmic electrode (etched from the backside) is visible in the middle. Due to the metal reflectivity, no charge could be generated under the strips, therefore they appear as inefficient regions in both scans. Being the columnar electrodes empty, they also appear as low efficiency regions. As already mentioned in the previous chapter, the column inefficiency can be fully recovered by tilting the devices with respect to the impinging radiation. As expected for un-irradiated 3D sensors, the scan at 30 V of bias appears very uniform and, at a first glance, does not show any particular problems. More informations can be extracted for the scan performed at 2 V, for which the sensor is not fully depleted.

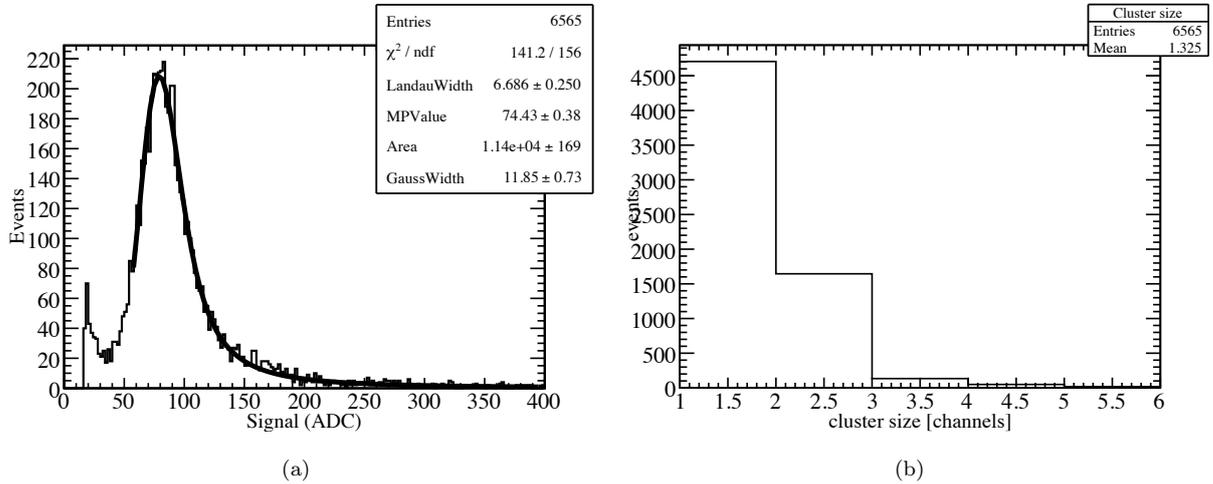


Figure 4.63: Fitted Landau distribution (a) and cluster size measurement (b) obtained from β particle measurements for an applied bias voltage of 15 V [132].

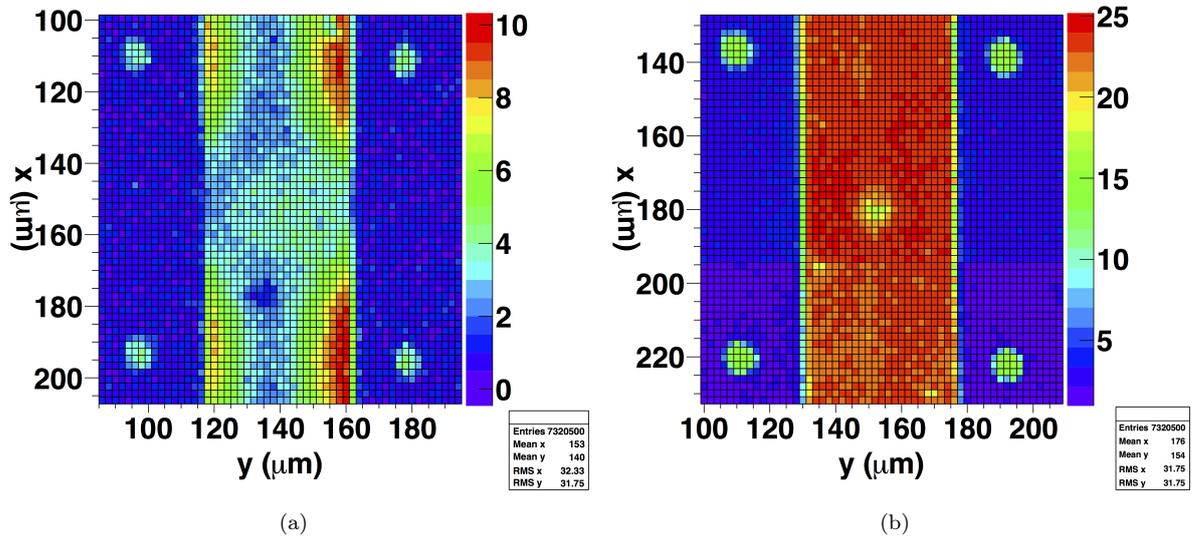


Figure 4.64: Laser scan results for a DC coupled strip detector assembled using DC pads and external fan-ins for two different bias voltages, 2 V (a) and 30 V (b) [132].

Table 4.16: Summary of all the available FBK sensors bump-bonded to the FE-I4 readout chip. Both irradiated and un-irradiated assemblies are reported together with received fluence and the type of performed tests [113].

Sample ID	Irradiation Facility	Dose [n_{eq}/cm^2]	Performed tests
FBK13	-	un-irrad	Source scan
FBK87	KIT(p)	5×10^{15}	Source scan, test beam
FBK90	KIT(p)	2×10^{15}	Test beam
FBK104	-	un-irrad	-
FBK111	-	un-irrad	-
FBK112	-	un-irrad	-

In Fig.4.64(a) two important effects can be noticed: (i) the right part of the scan appears to be more efficient than the left, and (ii) the depletion region proceeds from the n^+ columns (in the four corners) toward the p^+ column in the middle of the scanned area. Closely observing the metal strip pattern, it is possible to understand that the metal is actually slightly misaligned with respect to the columnar electrodes. This is known to be caused by the wafer bowing and, if the misalignment is contained, it will not degrade the sensor performance. The fact that the depletion region extends from the n^+ electrodes was expected because the considered sensors are n-in-p.

This entire characterization will be repeated after the irradiation planned for the beginning of 2013 at Karlsruhe Institute of Technology, as already mentioned.

4.6.3 ATLAS FE-I4 Pixel detectors

The functional characterization of FE-I4 pixel detectors was performed by means of radioactive source scans in laboratories and with pions and positrons beams at CERN and DESY. Several sensors from both FBK and CNM were bump-bonded to the readout chip and, some of them, were irradiated up to the maximum IBL fluence of $5 \times 10^{15} n_{eq}/cm^2$ with both protons and neutrons. This section will report on the functional characterization of FBK pixel detectors but a few results from CNM devices are also reported for comparison, showing that the two technologies are equivalent in most cases. A summary of the bump-bonded FBK pixel sensors is reported in Tab.4.16, also reporting the received irradiation fluence. It should be stressed that, assemblies irradiated with protons at Karlsruhe Institute of Technology (KIT), received an estimated Total Ionizing Dose (TID) of roughly 750 Mrad, much higher of the IBL requirement of 250 Mrad for which the FE-I4 chip was designed.

Bump-bonded assemblies (both pre and after irradiation) were wire bonded to the single chip cards cards of the USBpix system (see Fig.4.66(b)) in order to be tested both in

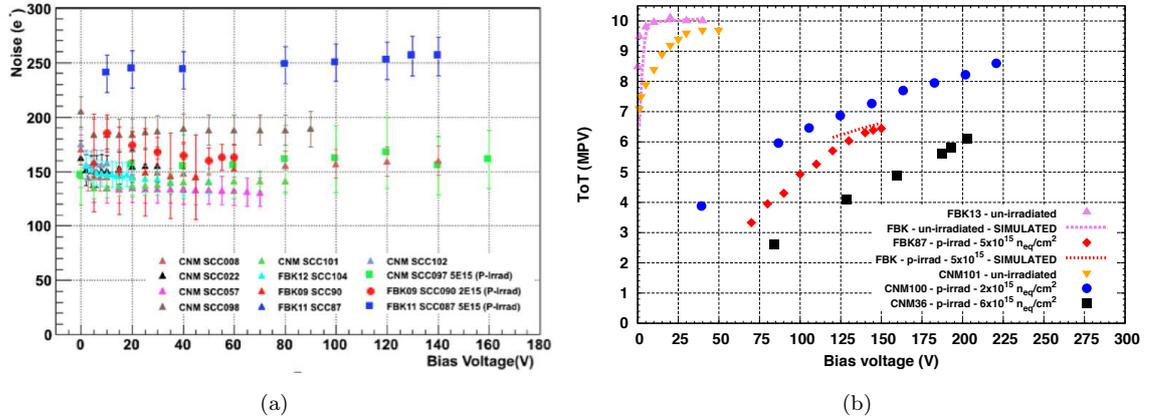


Figure 4.65: Noise as a function of the bias voltage (a) and charge collected in response to a ^{90}Sr radioactive source (b) for different 3D assemblies [113, 135].

the Lab and in test beams. Laboratory tests were performed by means of a ^{90}Sr radioactive source at CERN. Prior to measurement the system is tuned, in order to fix the threshold and the charge to ToT relation. The basic calibration is normally performed by fixing the threshold to $3200 e^-$ and $20 ke^-$ at 10 ToT. The threshold can normally be lowered down to roughly half of this value thanks to the very good performance of the readout chip. When the system is calibrated, it is possible to perform a noise characterization by injecting a fixed amount of charge in each pixel several times and by measuring the number of charge pulses detected versus the number of charge pulses injected. A summary of the noise values as a function of bias voltages for both FBK and CNM devices is reported in Fig.4.65(a) in both pre and post irradiation conditions [135]. Un-irradiated assemblies all exhibit the slowly descending noise trend that was also observed in the previous subsection for strip detectors, and tend to saturate to values in the order of $150 e^-$. The noise trend for irradiated samples is not clearly descending with bias, but the absolute values are not far from those of un-irradiated assemblies. This confirms that the increase in current caused by radiation damage, can be properly compensated by the chip without problems. Only one assembly (FBK87, blue square) irradiated at $5 \times 10^{15} n_{eq}/cm^2$, shows a larger noise figure. The cause of this is attributed to the presence of some "hot pixels" as a consequence of the high TID received, that ultimately drive the noise of the entire assembly. Noisy pixels can anyhow be later masked so that they don't affect the performance of the entire assembly.

The charge collection efficiency of the assemblies is studied by means of a collimated radioactive source placed on top of the sensor. The collimation is needed in order to limit the maximum impinging angle. The readout is triggered by a scintillator coupled to a Photo-Multiplier Tube (PMT) placed behind the assembly, so that only the most energetic

particles will trigger data acquisition. Fig.4.65(b) shows the MPV of the collected charge for several assemblies in both pre and post-irradiation conditions [135]. Unfortunately, a precise ToT to charge conversion is not available yet and it is therefore difficult to directly compare measurements performed on different sensors. The calibration was performed to have 10 ToT at 20 ke^- on each considered assembly. Numerical simulations were also performed in order to confirm the observed behavior and they are reported with dashed lines. Two un-irradiated devices were measured in pre-irradiation conditions, showing full charge collection at very low voltages, as expected from 3D detectors. The FBK sensor features a lower full depletion voltage ($<10 \text{ V}$) than the CNM device ($<25 \text{ V}$) due to the fact that columns are fully passing through the silicon bulk. Numerical simulations confirmed the observed behavior.

Data collected with the FBK87 assembly irradiated with protons up to $5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$, are also reported in the same plot and compared both with simulations and with two CNM devices irradiated at two different fluences, 2 and $6 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$. The collected charge is considerably lower than in the pre-irradiation case, due to radiation induced charge trapping. A reduction in the collected charge in the order of 20% was found for the sensor irradiated at $2 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ and in the order of 40% for the device irradiated at $5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$. This reduction is in good agreement with the analytical predictions based on inter-electrode spacing and on the effective drift lengths caused by trapping [123]. Numerical simulations of irradiated devices were performed with the "Perugia" model for p-type substrates [91] modified as described in [136]. The agreement with measurements is good, considering the uncertainties in system calibration, irradiation fluence and annealing conditions. Both simulations and measurements seem to indicate a full charge saturation just above a bias of 150-155V but, due to excess noise, measurements in the lab could not be performed at larger voltages. CNM devices require slightly larger biases to have a charge collection comparable to the FBK devices (notice that the fluence of $6 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ received by CNM36 is not much different from the fluence of $5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ received by FBK87 once the uncertainty on the delivered dose is taken into account).

Several IBL prototype modules have also been characterized using 4 GeV positrons at DESY and 120 GeV pions at the CERN SPS H6 and H8 beam lines during 2011 and 2012. Tests were performed using the EUDET telescope [100], consisting of six planes instrumented with Mimosas26 Monolithic Active Pixel Sensors having a pixel pitch of $18.4 \mu\text{m}$. Each plane consists of 1152×576 pixels covering an active area of $21.2 \times 10.6 \text{ mm}^2$. The triggering was performed by means of four scintillators in coincidence (two upstream and two downstream) resulting in an effective sensitive area of $20 \times 10 \text{ mm}^2$. The track position uncertainty when interpolated to the test modules was estimated to be $\sim 2 \mu\text{m}$. A picture of the EUDET telescope is reported in Fig.4.66(a), where all six Mimosas26 planes

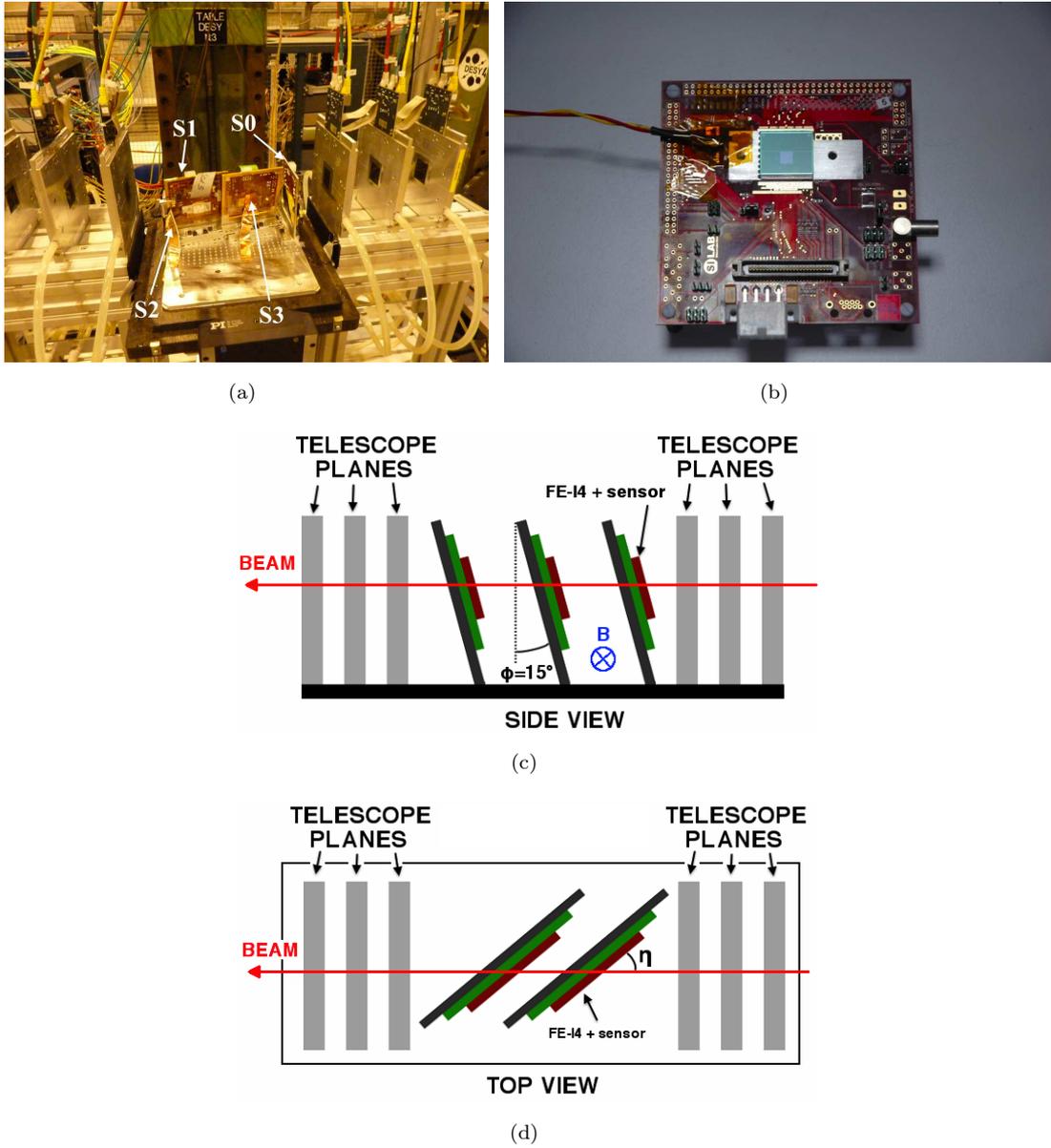


Figure 4.66: Pictures and sketches of the test beam setup: the six Mimosa26 planes of the EUDET telescope together with some DUTs mounted in a high η configuration (a), a picture of the single chip card of the USBpix system (b), the sketch of the side view of the test beam setup showing the ϕ angle and the sketch of the top view of the test beam setup showing the η angle (d) [113].

Table 4.17: Summary of all the FBK modules characterized in beam test reporting the most valuable results found together with tuning and irradiation parameters: sample ID, applied bias voltage, magnetic field on/off, tilt angle in the ϕ direction, type of particle used for the irradiation, received dose, hit efficiency, ToT to charge tuning and used threshold [113].

Sample ID	Bias	B-field	ϕ	-	Dose	Hit eff.	Tuning	Th.
-	[V]	-	[°]	-	[10^{15} n _{eq} /cm ²]	[%]	[ToT/ke ⁻]	[e ⁻]
FBK13	-20	off	0	un-irrad	-	98.8	10/20	1500
FBK90	-60	off	15	p-irr	2	99.2	8/10	3200
FBK87	-140	off	15	p-irr	5	95.6	10/20	2000
FBK87	-160	off	15	p-ire	5	98.2	10/20	1500

are visible together with the Devices Under Test (DUT) in the middle.

The tests were typically performed on three pixel modules at the time using an additional fourth as a reference plane (normally a planar detector with zero degrees tilt with respect to the beam). For a part of the run period it was possible to perform the tests inside the 1.6 T superconducting Morpurgo magnet, in order to emulate the operating conditions devices will face inside the ATLAS detector.

DUTs were wire bonded to the single chip cards and mounted on the telescope, normally with respect to the beam, using mechanical holders so that the long pixel direction (z direction in the IBL) was horizontal. Small tilt angles along the horizontal axis (also known as ϕ direction), were achieved by mounting the modules on wedges machined to simulate the desired angle (see Fig.4.66(c) reporting a sketch of the side view of the test beam setup). Rotations around the vertical axis, corresponding to different pseudo-rapidity values (η), were made using specially designed spacers allowing rotations equivalent to tracks in the pseudo-rapidity range $0.88 \leq \eta \leq 4.74$, as reported in Fig.4.66(d) showing the top view of the test beam setup.

Modules under test were mounted in a thermally insulated box, in which the temperature could be changed to test different operating conditions (the required operating temperature for the IBL is $T_{op} = -15$ °C).

The most important test beam results obtained with both un-irradiated and irradiated FBK pixel detectors are summarized in Tab.4.17 and will be here discussed in more detail. It is important to emphasize that CNM devices obtained very similar results but, since the focus of this thesis is on FBK sensors, results obtained with other sensor architectures will only be used as comparison.

FBK modules showed good charge collection, although, in some cases, due to the too low applied bias voltage, collected charge was a lower than expected. As an example, ToT distributions for an FBK and a CNM pixel sensor irradiated at 5×10^{15} n_{eq}/cm² and

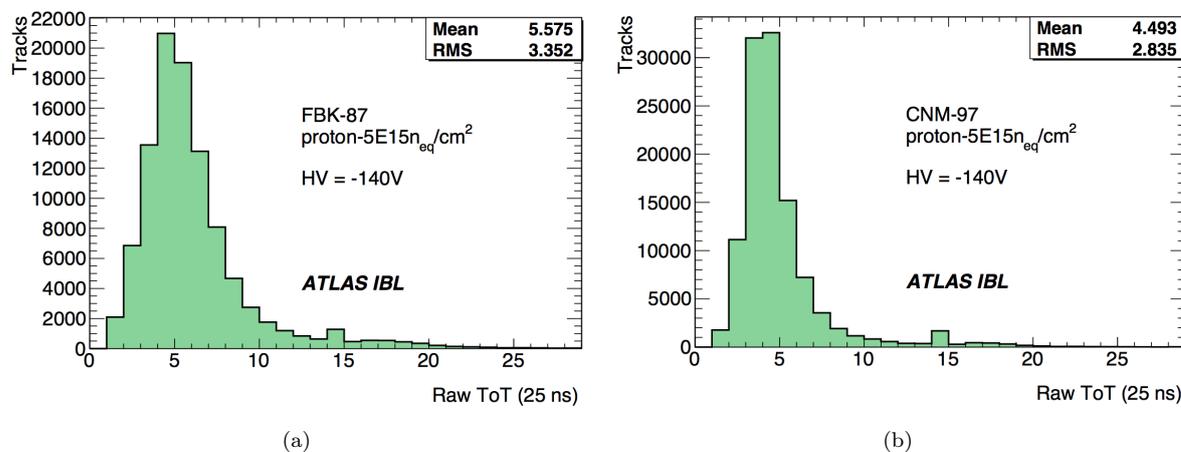


Figure 4.67: Raw ToT distribution for the FBK97 module (10 ToT @ 20 ke^- , threshold 2450 e^- ,) (a) and the CNM97 module (10 ToT @ 20 ke^- , threshold 2950 e^-) (b) for a tilt angle $\phi=15^\circ$ and no magnetic field [113].

for similar operating conditions are reported in Fig.4.67. Due to the fact that no ToT to charge calibration is available only a qualitative comparison is possible. The collected charge appears to be very similar although quite low due the non ideal bias voltage (140 V are not sufficient to operate the devices in the best conditions).

The most important parameter for the IBL operation is the hit efficiency of the pixel modules, especially after heavy irradiation. The overall hit efficiency is measured using tracks reconstructed with the telescope and interpolated to the test modules to search for a matching hit. The number of tracks with a matching hit is divided by the total number of tracks passing through the sensor. In order to get rid of fake tracks that might affect the efficiency measurement, a matching hit is required in at least one of the other modules under test. As previously stated, the large TID received by some assemblies caused the presence of some noisy/dead pixels. For this reason tracks pointing to these pixels and the surrounding ones needed to be removed from the efficiency analysis of proton irradiated assemblies. The tracking efficiency for all the measured FBK devices is reported in Tab.4.17 and the 2D maps of the hit efficiency in a single pixel are shown in Fig.4.68. As already found in previous 3D technologies (see Chapter 3 subsection 3.4.4), 3D pixel detectors cannot be 100% efficient with 0° title angles, due to the presence of the columnar electrodes that are dead region. This was also confirmed by the un-irradiated module here described (FBK13, see low efficiency regions in Fig.4.68(b)). For what concerns irradiated samples, FBK90 tested with 15° tilt and 60 V of bias, shows a very good tracking efficiency equal to more than 99%, as can be observed from the very good cell uniformity in Fig.4.68(c). This test also confirmed that 60 V of bias are sufficient to operate FBK 3D sensors irradiated

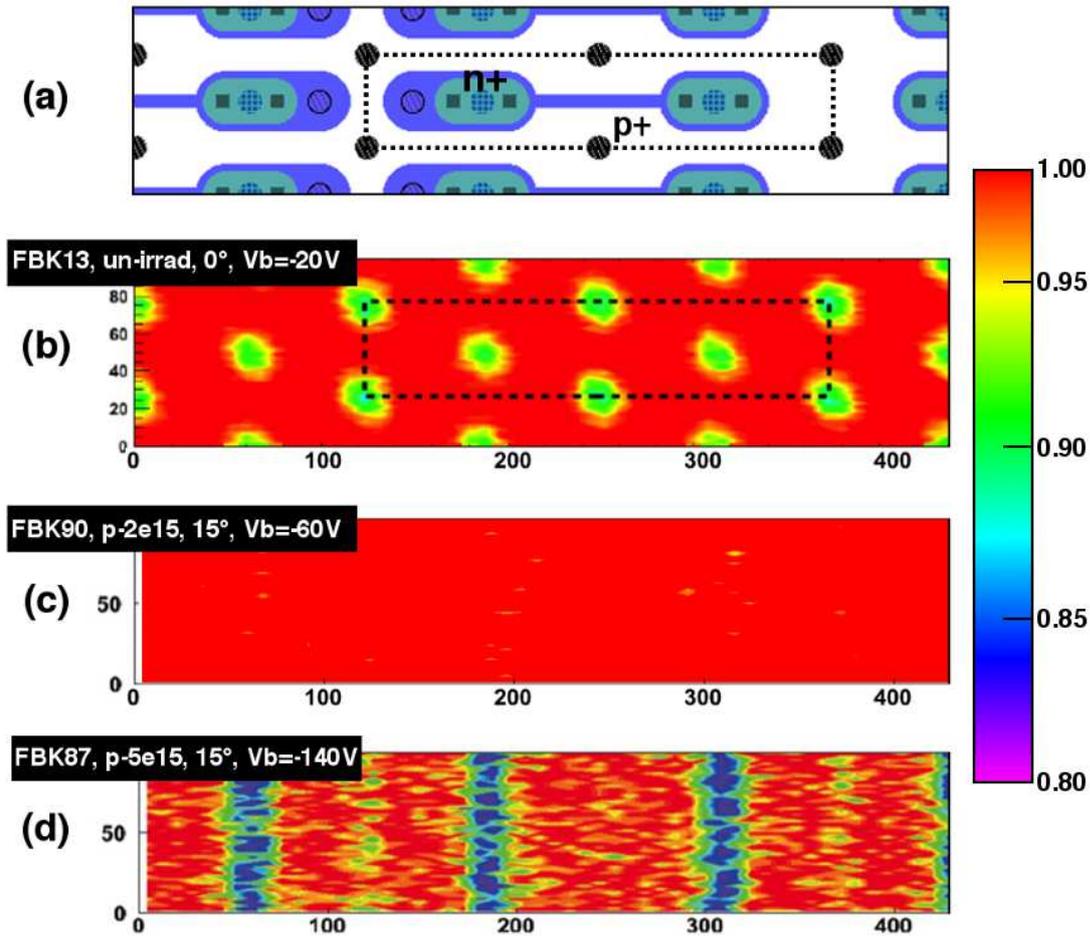


Figure 4.68: Cell efficiency maps: pixel geometry for an FBK pixel sensor (a), 2D efficiency map for the FBK13 module at 20 V of bias and without tilt along ϕ (mean efficiency 98.8%) (b), 2D efficiency for the FBK90 module at 60 V of bias and $\phi=15^\circ$ (mean efficiency 99.2%) (c) and 2D efficiency map for the FBK87 module at 140 V of bias and $\phi=15^\circ$ (mean efficiency 95.6%) (d) [113, 137].

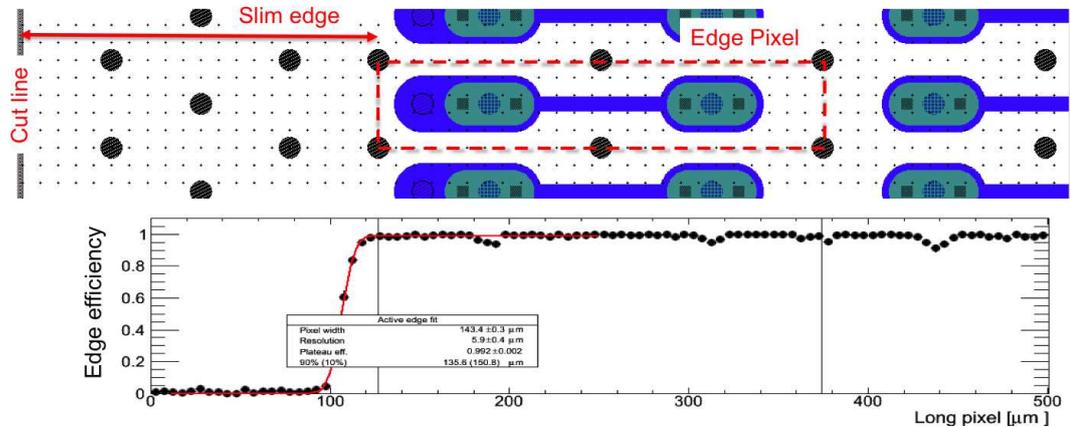


Figure 4.69: Edge pixel efficiency for the FBK90 module operated at 60 V and with a tilt of 15° in the ϕ direction [135].

at a fluence of $2 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ in the optimal conditions (the optimal operating voltage after the considered fluence was estimated to be in the order of 55-60 V using numerical simulations). The FBK87 module, instead, performed poorly in the first test beam with a hit efficiency not satisfying the IBL specifications (value highlighted in Tab.4.17). The reason for this poor results were understood after numerical simulations and radioactive source scans were performed: the applied bias of 140 V was not sufficient to fully depleted the sensor, leaving large low field regions that, combined with the trapping induced by the radiation damage and the charge sharing, led to a rather low tracking efficiency. This effect is also evident in Fig.4.68(d), where large inefficient regions can be observed. Differently from what found on CNM devices and also on older 3D technologies, the inefficient regions are placed near the junction electrodes (normally they are close to the ohmic electrodes). Although a lower hit efficiency is expected along directions connecting two electrodes of the same doping type, this effect is expected to be worse along the direction connecting ohmic electrodes, because of a slightly lower electric field and the longer distance electrons must travel to reach the collecting electrodes. The cause of this effect is not completely understood and further measurements and simulations are required. It is important to notice that, in a later beam test at DESY in March/April 2012, data were taken with FBK87 with a lower threshold and with a proper bias of 160 V, restoring the tracking efficiency to values above 98%, satisfying the IBL specifications. Unfortunately, due to the large multiple scattering of positrons used at DESY, it is not possible to reconstruct the 2D hit efficiency map, information that needs to be extracted from the data collected during the latest test beam at CERN (August/September 2012). Data are currently being reconstructed.

Another important parameter for the IBL is the extension of the inactive edge area.

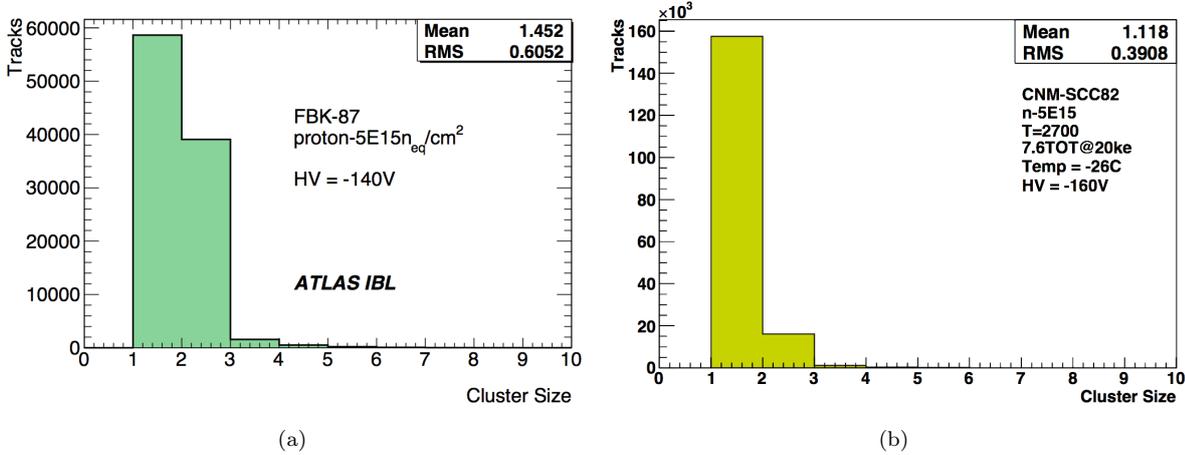


Figure 4.70: Comparison between the charge sharing of the FBK87 (10 ToT @ 20 ke⁻, threshold 2450 e⁻) and CNM97 (7.6 ToT @ 20 ke⁻, threshold 2700 e⁻) pixel assemblies for a bias voltage of 140 V and a tilt angle of 15° in the ϕ direction [113, 137].

This can be estimated by measuring the hit efficiency of the edge pixels. In Fig.4.69 the 1D edge pixel hit efficiency is compared with the sensor layout for the FBK90 module. The efficiency inside the active area is, as expected, very high. When tracks impinge the device outside the edge pixel, they can still be detected for about 20 μm (calculated by looking at the 50% hit efficiency in the profile in Fig.4.69). Considering the designed 200 μm edge region, this result returns a dead region of about 180 μm for the FBK pixel sensor (with possible residuals from the dicing of the scribe line). It is important to remember that, as found on 3D diodes, the edge area extension can be safely reduced to about 100 μm with proper sensor dicing (see subsection 4.4.2). Several studies have been performed in the past year on the improvement of the edge termination of 3D detectors by means of numerical simulations and the results will be presented in the next chapter.

The charge sharing is a fundamental parameter of every segment detector. Large charge sharing between adjacent pixels can lead to better tracking resolution, since the hit position is better reconstructed with an appropriate algorithm. However, if charge sharing occurs, the carriers generated by an event will be divided between different cells, reducing the probability of pixels passing the electronics threshold. This is a major concern especially for irradiated devices, where the total available charge is further reduced by the presence of the radiation induced charge trapping. Fig.4.70 shows the comparison between the charge sharing of the FBK87 and CNM97 modules operated in similar conditions. The devices show similar charge sharing, although the FBK is interested by a larger number of two pixels clusters, probably because of the lower threshold that allows pixels to detect a hit even with smaller charges generated inside them. These results also confirm that 3D

devices suffer from less charge sharing than planar ones.

Another key parameter for pixel detectors is the spatial resolution that, in case of multi-cluster hits, can be calculated using the information about the amount of deposited charge in each pixel (as already discussed in Chapter 2 subsection 2.2.4). The spatial resolution can be reconstructed from residuals distributions of all-hit clusters in the short pixel direction, where the track position is interpolated from the telescope and the cluster position, using simple charge weighting between cells. The measured spatial resolution for both 3D (FBK and CNM) and planar detectors is equal to about $15\ \mu\text{m}$, result that will be improved with more sophisticated clustering algorithms.

Since in the IBL the modules at the higher $\eta=2.9$ will see hits with a maximum track incident angle of $\theta=84^\circ$, tests were also performed with large tilts in this direction. Considering the sensor bulk thickness, tracks with such a large incident angle can traverse up to seven cells in the z-direction, causing the generated charge to be spread among several pixels. This could lead to charge losses when carriers are generated in low field regions and might cause some pixel to not pass the threshold. This measurement was only performed on CNM and planar devices and, as expected, the orientation of the electrodes in 3D devices resulted in a lower deterioration of the track hit accuracy in favor of 3D devices (see [113] for additional details).

During the entire IBL qualification, 3D detectors showed performances similar or better than planar devices, but for lower applied biases and, therefore, lower power dissipation. A complete analysis of the results obtained for planar detectors is reported in [113] and compared to those of 3D sensors.

4.6.4 CMS PSI46V2 Pixel detectors

In addition to ATLAS pixel detectors, both the DTC-3 and DTC-4 wafer layouts included CMS pixel sensors compatible with the PSI36V2 readout chip (Chapter 1 subsection 1.4.2), having a pixel size $150\times 100\ \mu\text{m}$ and an active matrix composed by 80 rows and 52 column for a total of 4100 pixels. The total size of the readout chip is similar to the older ATLAS FE-I3 chip and corresponds to roughly $1\ \text{cm}^2$.

Three different 3D pixel configurations were made available: (i) one junction column per pixel (1E), (ii) two junction columns per pixel (2E) and (iii) four junction columns per pixel (4E). The inter-electrode distance in the three different configurations are $90\ \mu\text{m}$, $62.5\ \mu\text{m}$ and $45\ \mu\text{m}$ for the 1E, 2E and 4E configuration respectively. The three pixel configurations are shown in Fig.4.71, also indicating the typical simulation domain. It is important to notice that, for the 1E configuration, two additional p^+ columns are present at $50\ \mu\text{m}$ from the n^+ so that, in this particular case, two different inter-electrode distances are effectively present, $90\ \mu\text{m}$ and $50\ \mu\text{m}$.

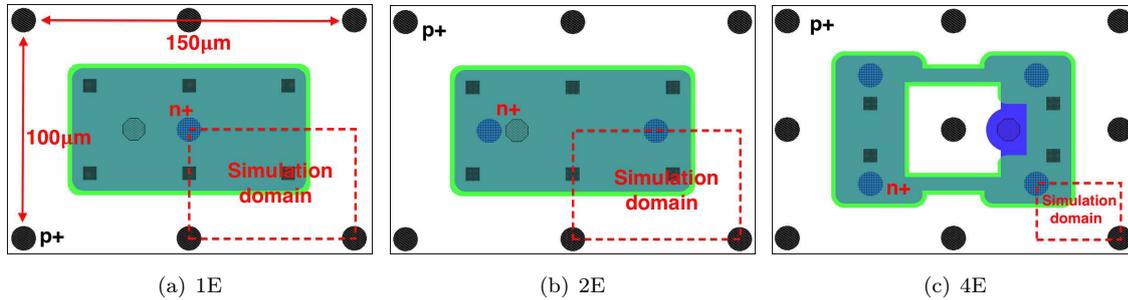


Figure 4.71: Sketches of the CMS 3D pixel configurations available.

Most of the devices here described come from the ATLAS08 batch and were fabricated on four inches, Float Zone, 200 μm thick, p-type wafers with $\langle 100 \rangle$ crystal orientation. As previously described, the ATLAS08 batch featured a very high p-spray doping concentration, resulting in a rather low breakdown voltage. A few devices from the ATLAS09 batch were also characterized and results will be shown later.

FBK pixel sensors were bump-bonded to the CMS PSI46V2 readout chip at SELEX Sistemi Integrati, Rome, Italy, with an Indium based process. Devices were assembled and tested in two different laboratories: Purdue Particle Physics Microstructure Development Laboratory (P3MD) at Purdue University, USA, and at INFN Torino, Italy.

Laboratory tests here described were performed at Purdue University [138]. Fig.4.72(a) show a sketch and a picture of the system used to perform the tests. The bump-bonded assemblies were glued and wire bonded to a Very High Density Interconnect (VHDI) circuit, which was later wire bonded to a fan-out connection board. The system assembly was completed by gluing the VHDI and the fan-out to a carbon fiber base plate. The bias voltage for the sensor is provided through a wire bond connected to its backside and to an appropriate bias pad on the fan-out board.

The laboratory characterization of CMS 3D sensors was performed by means of radioactive source (^{90}Sr) scans. The complete system consisted of a DAQ board, a 3D detector adapter and a PC. The DAQ board features a Field Programmable Gate Array (FPGA), a 12-bit analog-to-digital converter (ADC), and a 64 MB SDRAM buffer and it is connected to the PC via USB serial communication. The DAQ board and the readout chip characterization software, were developed to perform module qualification and measurements for the current CMS barrel pixel detectors [139]. The used radioactive source is a 1 mCi ^{90}Sr source emitting electrons, it has 50 μm wide opening and was placed 1 cm away from the detector. The measurements are performed using the system self-triggering capabilities.

Before proceeding with the charge collection studies a quick I-V measurements was taken for each device. This was done for essentially two reasons: (i) the temporary metal

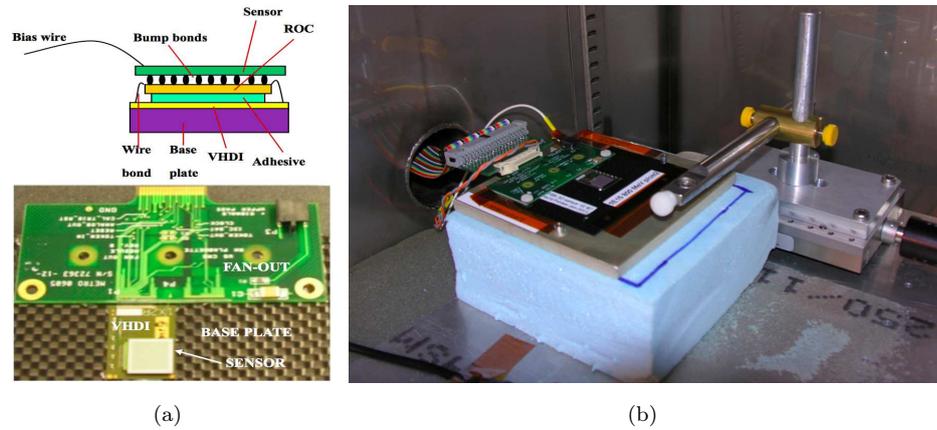


Figure 4.72: Sketch and picture of the VHCI connector wire bonded to the fan-out board (a) and picture of the source scan setup at University of Purdue [138].

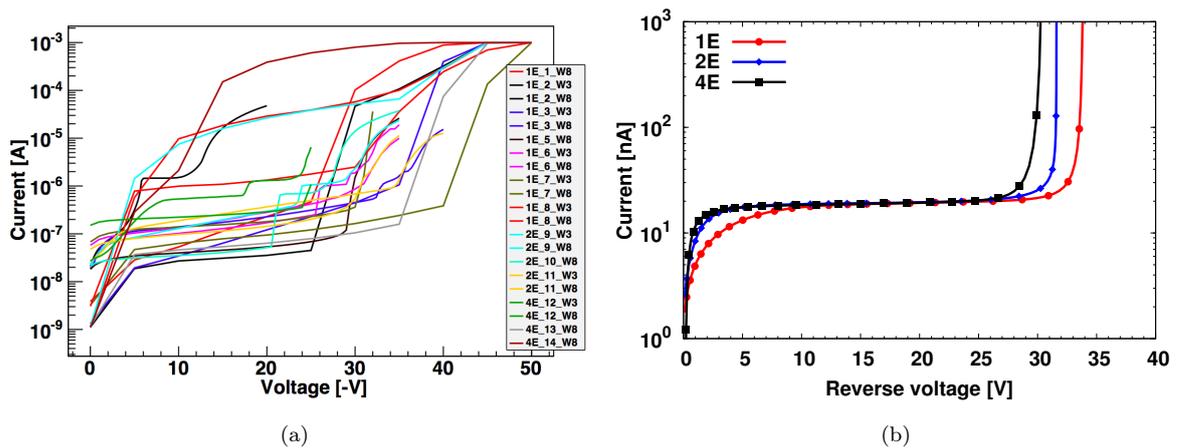


Figure 4.73: Measured (a) and simulated (b) reverse currents for the different pixel configurations [138].

was not available in the ATLAS08 batch (DTC-3 wafer layout) therefore no on-wafer selection was possible and all sensors were "blindly" bump bonded and (ii) to have a first idea of what to expect in terms of operating conditions. The performed I-V measurements are shown in Fig.4.73(a) and are compared with the simulated currents for the three available pixel configurations reported in Fig.4.73(b).

Most devices show acceptable currents, but with a rather large span, between 50 nA and 200 nA. The numerical simulations performed taking into account all the process parameters suggested that, devices with "intrinsic" behavior should have currents slightly higher than 50 nA. Sensors having larger currents are probably affected by premature breakdown effects induced by defects. The measured and simulated breakdown voltages are in good agreement and, as expected from the high p-spray doping concentration, they

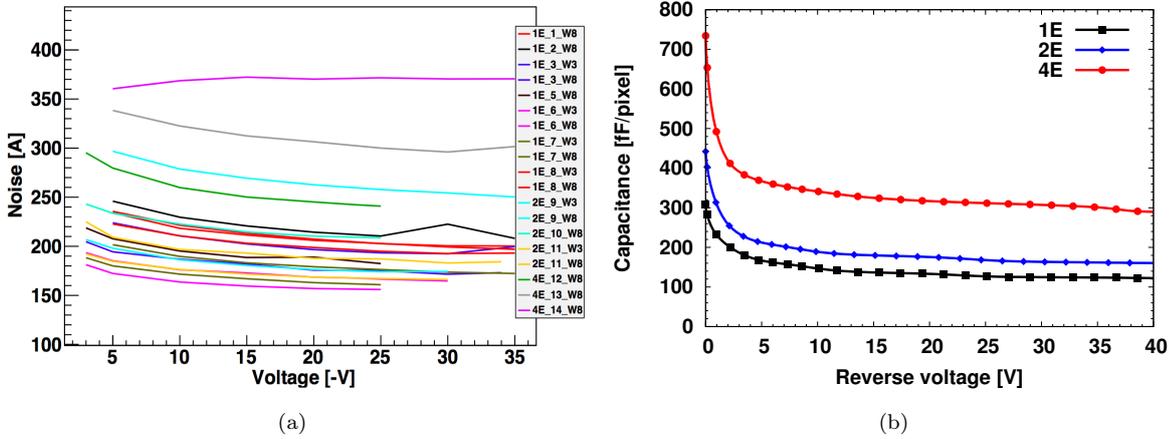


Figure 4.74: Noise figures for all the available pixel assemblies with respect to the applied bias (a) and simulated C-V curves for all the available pixel configurations [138].

are rather low, about 30 V. The knee observed in both measured and simulated currents indicated full depletion before 10 V for all the pixel configurations, so the low reverse discharge is not of major concern.

In order to understand if the increased pixel capacitance of 3D detectors would affect the noise of the system several noise scans were performed as a function of the bias voltage. Results are shown in Fig.4.74(a) and, since C-V measurements of pixel devices are not available, they are compared with the simulated C-V reported in Fig.4.74(b). The assemblies featuring the larger noise figures are those exhibiting premature discharge and very large leakage currents. Non defective devices, instead, feature ENC values between 150 and 250 electrons, roughly 50 electrons larger than planar pixel assemblies. The noise has a descending trend with respect to the applied bias because it is directly dependent on the sensor capacitance, which decreases and saturates after about 10 V. It is important to notice that it is hard to properly identify any noise differences between different pixel configurations: although for fast peaking times the noise should be dominated by the total capacitance (series noise), if the reverse current is large (parallel noise) it might be dominating over the capacitance component.

Although slightly larger than for planar pixel sensors, the noise should not affect the charge collection performances. The source scans were performed only on half of the available assemblies, the others were sent for irradiation. The results are reported in Fig.4.75(a) and are compared with the expected charge collection estimated from simulations (Fig.4.75(b)). The pixel threshold was set to 3900 electrons. The most probable collected charge in a 200 μm thick silicon sensor in response to a MIP is roughly 16 ke^- . The values measured with the studied devices are roughly 2000 electrons lower

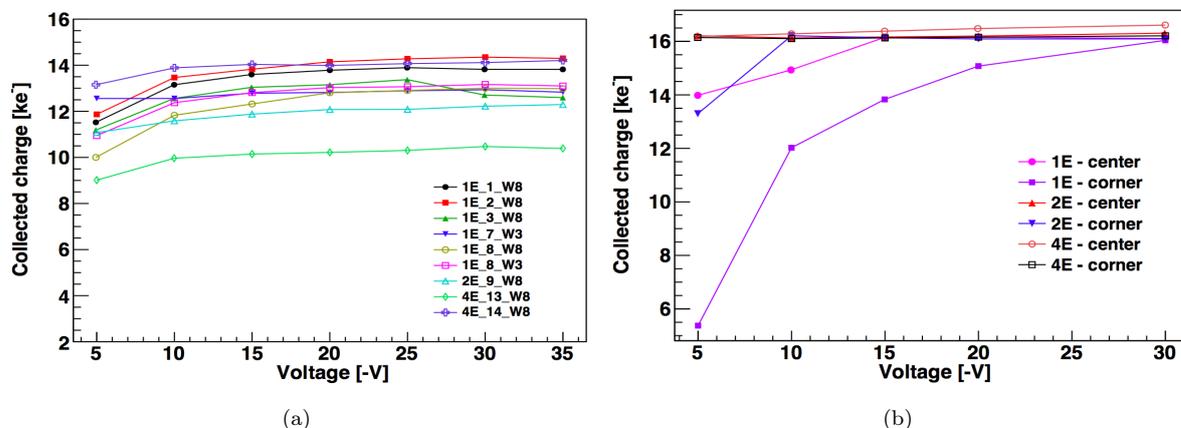


Figure 4.75: Measured (a) and simulated (b) charge collection as a function of the bias voltage in response to MIP particle. Simulations are performed for two different hit position: the center of the cell (high field region) and the corner of the cell (low field region) [138].

than the expected ones. This can be attributed mainly to two factors: charge sharing and uncertainty on the thickness of the bulk. Since the source is not collimated and was placed 1 cm away from the sensor, most particles impinge the devices with large angles (estimated to be roughly 80 degrees), increasing the charge sharing among neighboring pixels. Part of the shared charge might not be sufficient to be detected with the fixed threshold of $3900 e^-$. The other effect that might cause a decrease in total collected charge is the uncertainty on the thickness of the substrate. This quantity was estimated to be slightly lower than $200 \mu\text{m}$ from C-V measurements performed on planar test diodes. Additional information can be extracted from the simulated charge collection: as can be seen in Fig.4.75(b) if the particle impinges the devices in the center of the cell, mid-way between two electrodes of opposite doping type, charge saturation is reached at very low biases. On the contrary, if the charge is generated in low field regions (e.g. the corner of the simulation domain), it takes larger voltages to reach full saturation, up to 30 V for the 1E pixel configuration. This suggests that it is crucial to be able to apply the proper bias voltage in order to get rid of most low field region.

An example of collected Landau distribution is reported in Fig.4.76 for a 4E 3D pixel detector operated at 15 V. The MPV was estimated to be 14 ke^- from the fit shown with the dashed line.

A summary of all the most important values found in this characterization, is reported in Tab.4.18. A good agreement was found between measured and simulated leakage currents on non-defective devices. A slight difference in breakdown voltage was found, but it is within the uncertainties caused by the grid meshing, and is mainly related to how the breakdown was detected in the measurements (the voltage at which the reverse current

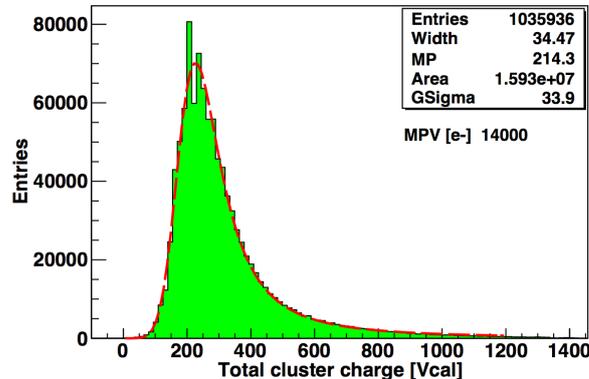


Figure 4.76: Landau distribution of a total cluster charge collected with a 4E device operated at a reverse bias of 15 V [138].

Table 4.18: Summary of the parameters extracted from the laboratory characterization and numerical simulation of CMS pixel detectors fabricated at FBK and coming from the ATLAS08 batch. Breakdown voltage (V_{BD}), leakage current (I_{LK}), signal to noise ratio and the corresponding simulated values are here reported [138].

Pixel conf.	V_{BD} [V]	I_{LK} [nA]	S/N -	Sim. V_{BD} [V]	Sim. Leakage @20 V [nA]	Sim. Capacitance @20 V [fF/pixel]
1E	40	31-193	66	30	42	133.36
2E	38	41-264	46	31	44	175.84
4E	35	53-248	36	30	52	316.32

reached the set instrument compliance). As far as signal to noise ratios are concerned, due to the lower capacitance the 1E configuration would be the best one but, because of the larger inter-electrode distances, it will require higher operating voltages. For this reason the only configuration that provides both low operating voltages and reasonable signal to noise ratios, is the 2E configuration which, with an inter-electrode distance of $62.5 \mu\text{m}$ is fully representative of what was previously found to be the best configuration also for the ATLAS FE-I4 pixel devices (inter-electrode distance of roughly $67 \mu\text{m}$).

In addition to laboratory tests, a beam test was also performed and results are reported in [140]. The beam test was performed with 120 GeV/c protons at the Fermi Meson Test Facility, Batavia, USA. The track reconstruction was performed using a telescope made of 8 planes of planar CMS pixel sensors, able to achieve a spatial resolution of $6 \mu\text{m}$ in both directions. The tracking efficiency was found to saturate at a value of about 97.5% for a bias voltage of 20 V and a tilt angle of 0° . As for the ATLAS 3D pixel detectors, inefficiencies in this test configuration are mainly related to the empty columnar electrodes, resulting as dead regions in the detector. When the devices are titled

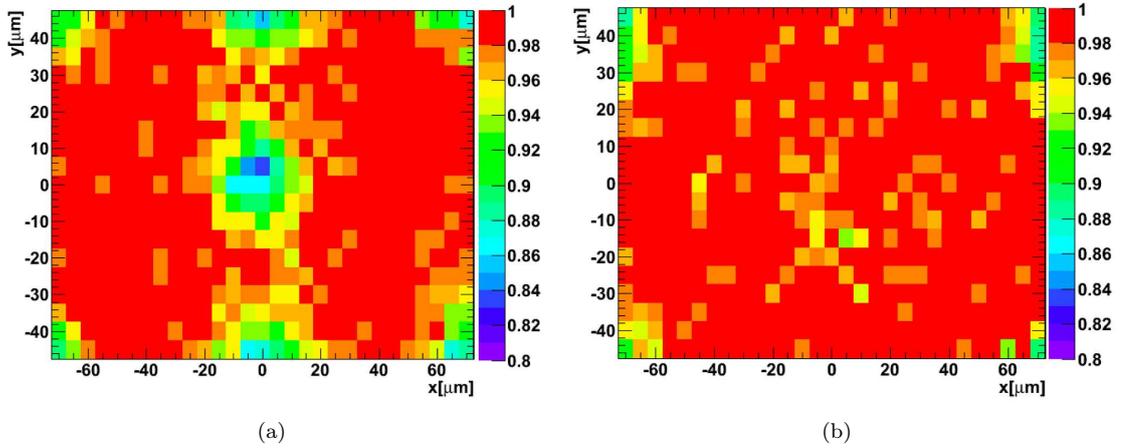


Figure 4.77: 2D efficiency maps for a 1E pixel detector coming from the ATLAS09 batch biased at 20 V for a 0° angle (a) and for a 20° angle (b) [140].

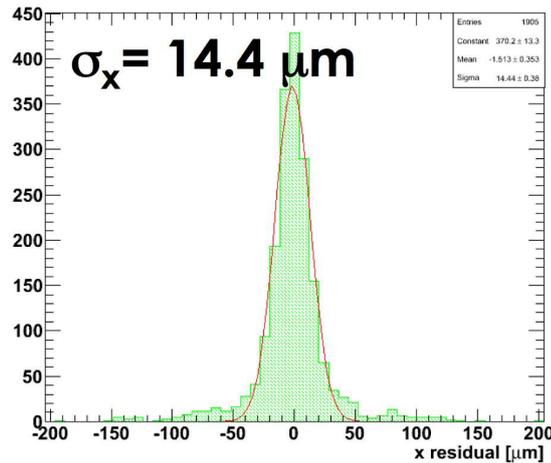


Figure 4.78: Measured spatial resolution for a 1E 3D pixel sensor in the x coordinate [141].

by 20° with respect to the beam, the efficiency is increased up to roughly 98.5% with the same bias voltage. The 2D efficiency maps for the two described cases are reported in Fig.4.77. The inefficient electrode regions are visible for the 0° case (Fig.4.77(a)) while more uniformity is obtained by tilting the devices by 20° (Fig.4.77(b)).

In addition, the measured spatial resolution, extracted from the track residuals for the 20° case, was found to be roughly $14 \mu\text{m}$ in both the x and y directions, compatible with what previously found on ATLAS FE-I4 pixel sensors.

Many of the available pixel assemblies were irradiated with protons up to large fluences and the characterization is being repeated. The data analysis is being performed, the preliminary results are encouraging and will be published shortly.

Chapter 5

Improving 3D technology at FBK

As demonstrated in the previous chapter, the ATLAS IBL has proved to be an incredible driving force for 3D technology. By creating the 3D sensor collaboration and by focusing the efforts of all the people involved, it was possible to exit the R&D phase and enter the technology industrialization successfully, completing the very first medium volume production of 3D pixel detectors. This remarkable achievement is very important because it was reached in a relative short time and very stringent requirements were satisfied. Moreover, all the performed tests and numerical simulations helped in completing the knowledge of 3D from many points of view. In fact both the electrical and functional characteristics of 3D detectors are now much better understood.

During the qualification of the 3D pixel detectors for the IBL it was understood that, especially for FBK technology, some aspects could be improved in order to deliver more reliable detectors. Building on the obtained results, it was decided to produce an additional R&D batch at FBK, in order to further improve the available 3D technology. At the beginning of 2012 a new wafer layout was designed with the help of numerical simulations [142]. This new wafer layout is internally known as DTC-5 and it contains pixel detectors in different configurations, strip detectors and a very large amount of 3D test structures needed to test different geometrical modifications. A new type of edge termination was also designed in order to further reduce the already small dead area at the edges.

This chapter will include the most relevant results obtained during the numerical simulation phase also discussing many of the implemented layout modifications. Preliminary results from the electrical characterization will also be reported.

5.1 Possible improvements to FBK technology

The functional characterization of FE-I4 pixel detectors both before and after heavy irradiation highlighted some important considerations about the optimal operating conditions of 3D detectors. As previously described in Chapter 4 subsection 4.6.3, it is crucial to operate devices at the correct bias voltage in order to obtain the desired tracking efficiency, especially after heavy irradiation, when charge trapping becomes more important. In order to do so, it was understood that it is of paramount importance to assure the highest possible breakdown voltage in pre irradiation conditions, in order to obtain the needed increase after irradiation. From this point of view, the large campaign of electrical tests and numerical simulations performed on 3D diodes with different layouts, allowed to understand that two critical regions are present in the current design of FBK 3D detectors. These critical regions are located on both sensor surfaces, where the highly doped p-spray isolation layer touches a grounded n^+ region. Being the p-spray biased at the same potential applied to the back side, large electric field peaks are present on both surfaces, reaching the critical value for relatively low voltages. This is normally not a concern before irradiation, because the full depletion voltage is lower than 10 V, but can be an issue after irradiation. The radiation induced oxide charge normally reaches large values, partially compensating the p-spray doping concentration and leading to larger operating voltages. It is important to stress that this is often not the case for devices showing defects before irradiation: if the breakdown voltage is lower than the intrinsic value, the increase after irradiation is usually much lower, causing the impossibility of reaching the optimal operating condition. This is also the reason for the stringent requirement set on breakdown voltage for IBL prototypes.

The IBL sensor qualification also returned other important results: being FBK and CNM technologies slightly different, with CNM electrodes not passing through the silicon bulk, it was finally demonstrated that, if the distance between the column tips and the opposite surface is in the order of 25 μm or less, it is not crucial to have fully passing through columns. In fact, additional advantages can be obtained by having partial columns: particles crossing the columnar electrodes perpendicularly can generate charge in the bulk under the tips, resulting in lower tracking inefficiencies.

All these considerations were taken into account when designing the new DTC-5 wafer layout. The main objectives of the new technology were to enhance the voltage handling capabilities of all sensors, while reducing the fabrication complexity in order to obtain a faster sensor production. The most important geometrical modifications implemented in the new wafer layout are essentially two: (i) a modification of the n^+ implantations on the front surface, in order to decrease the absolute value of the front side electric field peaks

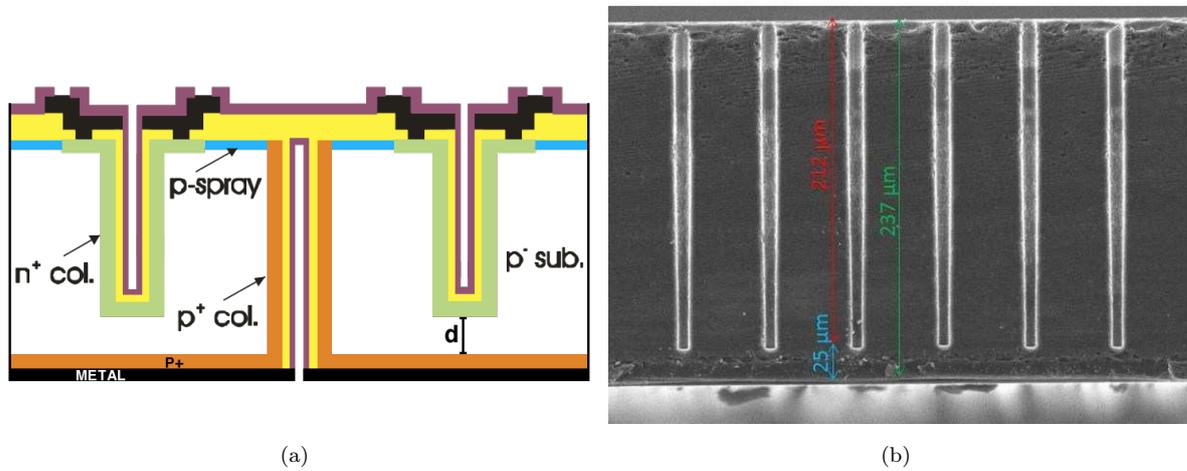


Figure 5.1: Proposed cross-section for the new batch of 3D detector to be fabricated at FBK (a) and calibration of the DRIE step to achieve the desired junction column depth (b) [142].

and (ii) the reduction of all the n^+ column depths by roughly $25 \mu\text{m}$, in order to eliminate the high field regions on the back side. The latter modification also greatly reduces the fabrication complexity because it eliminates the need for patterning the backside. It is important to remember that the ohmic columns need to remain fully passing through, in order to limit the extension of the low field regions and, more importantly, to assure the correct operation of the slim-edge fence. Both layout modifications were thoroughly investigated with the aid of numerical simulations and results will be here discussed.

A possible cross-section for the new sensor technology is reported in Fig.5.1(a). Since the distance between the n^+ column tip and the opposite surface (d) is crucial both in terms of charge collection and breakdown voltage, it is important to be able to perfectly control the DRIE process to obtain the desired column depth. To this purpose, several tests were performed at FBK in order to calibrate the parameters of the column etching step. The result of one of these tests is reported in Fig.5.1(b) where the gap between the column tip and the opposite wafer surface was measured to be $\sim 25 \mu\text{m}$ on a total wafer thickness of roughly $237 \mu\text{m}$. The etching depth also appears to be very uniform.

Since the ohmic columns will remain passing through, they will still bring the bias voltage applied to the back side directly to the p-spray layer on the front-side. By removing the high field region on the back side of the devices, the field-plate on the front side should now be able to better cope with this situation. In addition a further front side layout modification was conceived that should help redistributing the electric field in a more efficient way. This geometrical configuration implements a floating n^+ ring around the main grounded n^+ junction on the front side, the main objective being interrupting the outer p-spray electrostatic potential (equal to the backside bias) in order to obtain a

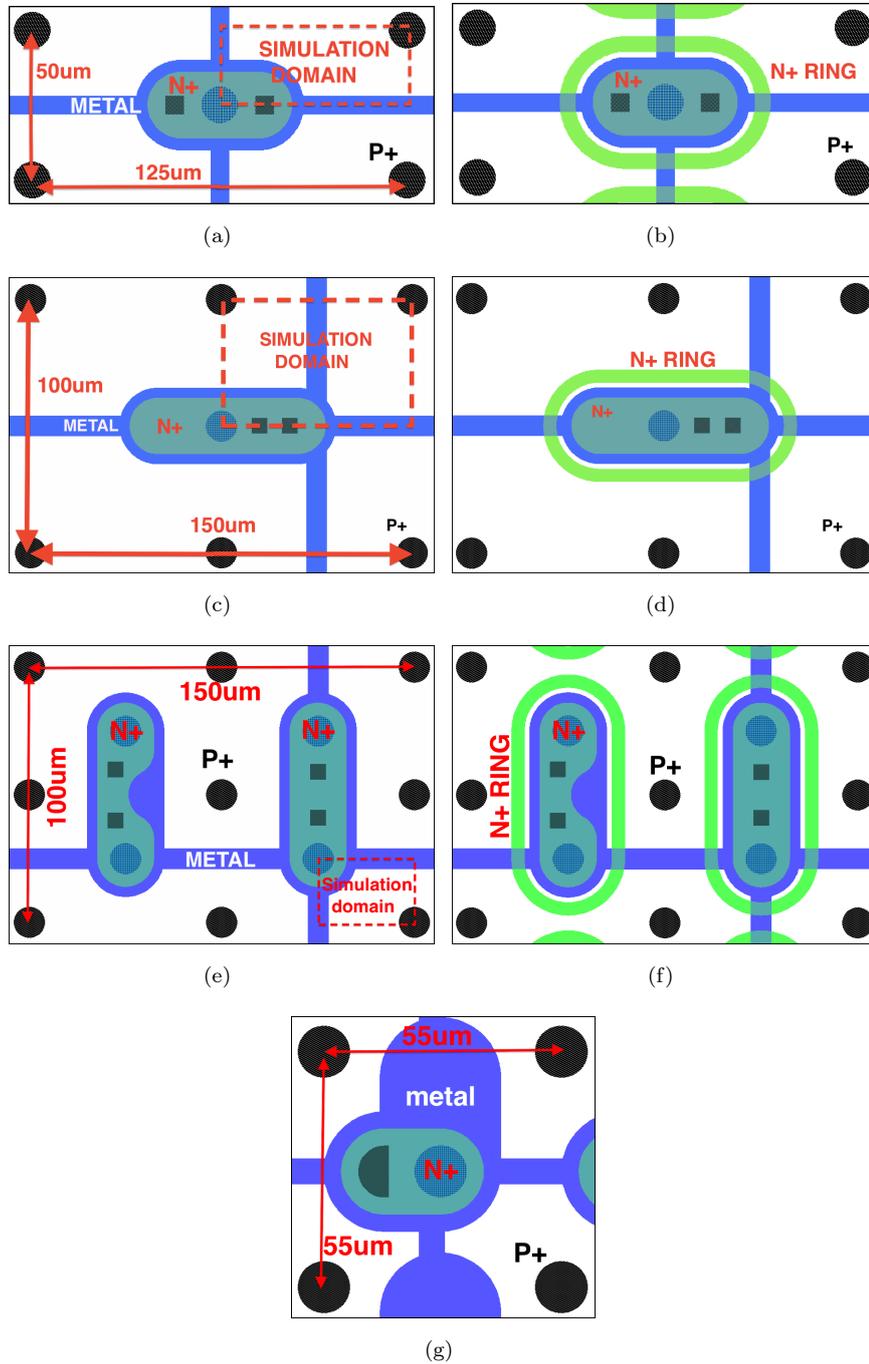


Figure 5.2: Layout of the front side of some of the most relevant 3D diodes available in the DTC-5 layout: FE-I4 (a), CMS 1E (c), CMS 4E (e) without floating n^+ ring and same diodes with n^+ floating ring (b), (d), and (f) respectively and MedipixII diode (g).

lower polarization of the inner p-spray. By lowering the electrostatic potential difference between the grounded junction and the p-spray, it should be possible to increase the voltage handling capabilities of the device. An example of the latter layout modification is shown in Fig.5.2 for different detector types.

Because of the growing interest in testing CMS-like 3D detectors [138], several implementation of these devices were included in the DTC-5 layout, in addition to FE-I4 pixel detectors, MedipixII pixel detectors and 80 μm pitch strip detectors. A total of 12 different sensor implementations were designed, each accompanied by its relative 3D test diode:

- 2 different FE-I4 diode configurations (with and without n^+ floating ring);
- 4 CMS diode configurations without n^+ floating ring (1E, 2E, 3E and 4E);
- 4 CMS diode configurations with n^+ floating ring (1E, 2E, 3E and 4E);
- an 80 μm pitch diode (recalling the strip detector geometry);
- 1 MedipixII diode.

Numerical simulations performed on the described structures are reported in the following section while a summary of the modifications to the fabrication process is given in section 5.4.

5.2 Numerical simulations

The discussed layout modifications were first tested performing numerical simulations on a quarter of an elementary cell for each investigated device type. Simulations were performed with the aid of the Synopsys TCAD tools. As previously explained, because of the peculiar electrode orientation, simulations of 3D detectors must be performed in three dimensions, in order to take into account the correct distribution of all the electrical quantities of interest. As an example, the structure used to simulate the FE-I4 diode with n^+ floating ring is shown in Fig.5.3(a) together with the 2D cross-section extracted from the diagonal connecting the two columnar electrodes. The n^+ island used to connect the columnar n^+ electrode was slightly reduced in size with respect to previous technologies in order to fit the floating ring in the space remaining between two adjacent pixels. The ring is 5 μm away from the island. The surface isolation is made of the usual uniform p-spray implantation on the front side. The backside is made of a uniform p^+ implantation. The n^+ electrode is not passing through and, in order to consider a worst case situation in which the DRIE process proceeds deeper than expected, the gap from the opposite wafer surface is set to 20 μm . The p^+ column is fully passing through. In order to see all the layout details, the silicon oxide layers on both wafer sides were hidden. The metal contact is shaped exactly following the desired layout: the field-plate is implemented on the front

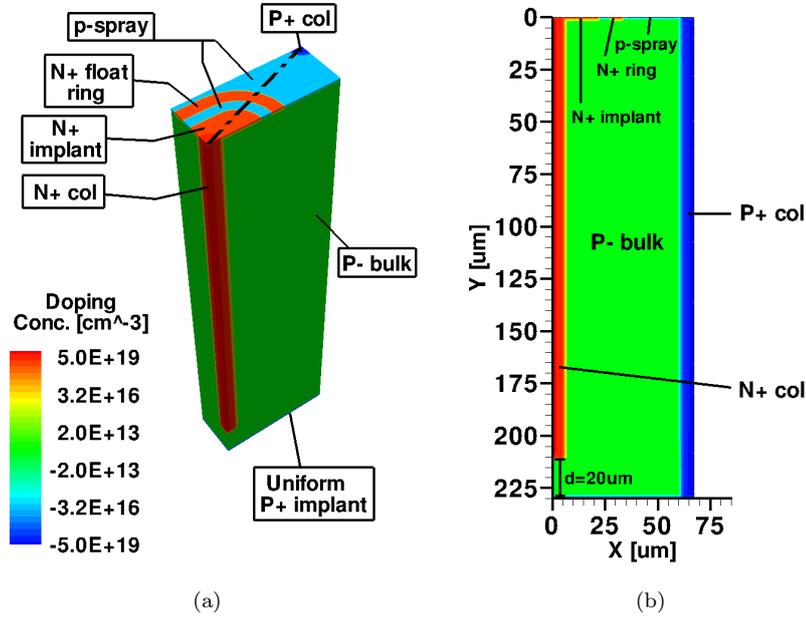


Figure 5.3: Structure used to simulate the FE-I4 diode with floating ring.

side while the contact is fully uniform on the back side. All the doping profiles for the surface implantations (e.g. n^+ on the front side, p-spray on the front side and p^+ on the backside) are representative of FBK technology and were obtained from Secondary Ion Mass Spectrometry (SIMS) measurements performed on a sample from one of the IBL production batches. The other process parameters such as carrier lifetimes, oxide charge concentration and surface recombination were also representative of the IBL production batches.

The structure is realized using a scripting language compatible with the program *Sentaurus Structure Editor* (sde) and is then meshed with *Sentaurus Mesh* (snmesh). The structure is quite complex and, since the main interest of these simulations was to correctly predict the electrical behavior, a proper meshing of the most critical regions is required (e.g. the front side geometries), leading to a total number of mesh points spanning from roughly 100 k for the less complex ($80 \mu\text{m}$ pitch diode) to more than 200 k for the most complex (CMS 1E with floating ring). Due to the asymmetry of the MedipixII structure it was not possible to only simulate a quarter of the elementary cell and the number of points diverged leading to the impossibility of obtaining reliable results.

The files generated from the meshing engine are fed to simulator, *Sentaurus Device* (sdevice), that, after receiving a command file proceeds to solve all the required differential equation. In the particular case of this study, Poisson's equation and the continuity

Table 5.1: Summary of the physical models used in the performed simulations.

Physical quantity	Numerical models
Effective intrinsic density	OldSlotboom
Mobility	Doping Dependence High Field Saturation Enormal
Recombination	Doping dependent SRH High Field Saturation Electric field driven Avalanche
Surface recombination	SRH

equations are solved before proceeding with a bias ramp on the back side p^+ while grounding the front side n^+ . The floating ring, when present, is set to have a null current in order to emulate the actual floating operation.

The simulator allows to chose between a large number of physical models, and the proper ones must be selected each time, depending on the performed analysis. In the specific case of the design of a new structure, it is crucial to enable, besides the standard models, also the avalanche breakdown one. In addition, material specific and interface specific (e.g. interface between silicon and silicon oxide) models can be enabled. Very important is the insertion of the positive charge trapped in the oxide and the surface recombination, because it can affect the breakdown voltage quite strongly. A summary of the used models is reported in Tab.5.1.

The simulator performs all the required calculations for each cell with specifically designed numerical solvers and returns the distribution of the required electrical quantities in several files that can be analyzed with specific software tools.

In order to understand if the modification applied to the newly designed structures had the desired result, the first performed analysis was focused on the reverse current as a function of the bias voltage for each of the simulated diodes and is reported in Fig.5.4. In agreement with the expectations, all devices showed an increase in breakdown voltage of at least ~ 15 V with respect to the best case reverse discharge obtain in the IBL production batches of roughly 50 V. The device showing a larger increase in performance seems to be the 80 μm pitch diode, featuring a reverse discharge at about 160 V. The other diode types, in the configuration without the floating ring, show a lower increase in breakdown voltages, but the reverse discharge still occurs between ~ 100 and ~ 120 V. The unexpected result was the small increase in voltage handling delivered by the presence of the floating ring. In fact, all the devices featuring this layout detail, reach breakdown at around 70 V.

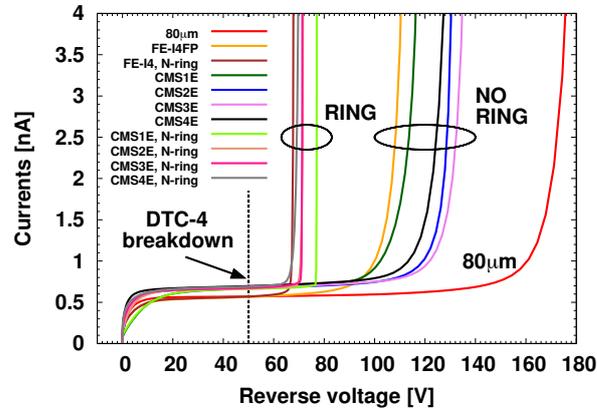


Figure 5.4: Simulated reverse currents for all the newly designed detector geometries included in the DTC-5 batch.

In order to understand the reason for this unexpected behavior, the distribution of the electrostatic potential and the electric field close to the front sensor surface, was extracted from the simulation results for a bias voltage of 65 V and is reported in Fig.5.5 comparing the two FE-I4 devices without (left) and with (right) the floating ring. In addition, the 1D distribution of the same quantities along the diagonal of the extracted 2D map is shown. As expected, the p-spray on the front surface is biased at 65 V, because the p^+ electrodes are bringing the bias applied to the backside directly to it. The electrostatic potential of the p-spray inside the floating ring (Fig.5.5(a) right) is considerably lower than the one on the outside, leading to a much lower potential difference at the main grounded junction. This is easily understood also observing the electrostatic potential profiles reported with dashed lines in Fig.5.5(c). For a coordinate of $25 \mu\text{m}$, the potential is much lower for the structure without floating ring. This shows that the expected effects of the n^+ ring were properly forecasted, but it does not explain why a lower breakdown voltage was obtained. This information can be extracted from the electric field distribution shown for the same structures in Fig.5.5(b). The case without ring (left) features the expected high field region at the curvature of the n^+ region, where the p-spray is in contact with it. The spreading of the electric field on a region of roughly $5 \mu\text{m}$ is the direct consequence of the presence of the field-plate, that helps in redistributing the field allowing for higher operating voltages. On the other hand, the devices featuring the floating ring (Fig.5.5(b) right) shows a low electric field in the region inside the ring (as expected) but a rather large field peak on the outside of the ring, where the biased p-spray is in contact with it, ultimately causing the breakdown to occur earlier than for the other structure. This is easily observed in Fig.5.5(c): the electric field peaks on the main n^+ region are considerably lower for the floating ring case, and the effect of the field-plate is visible for both structures. The electric

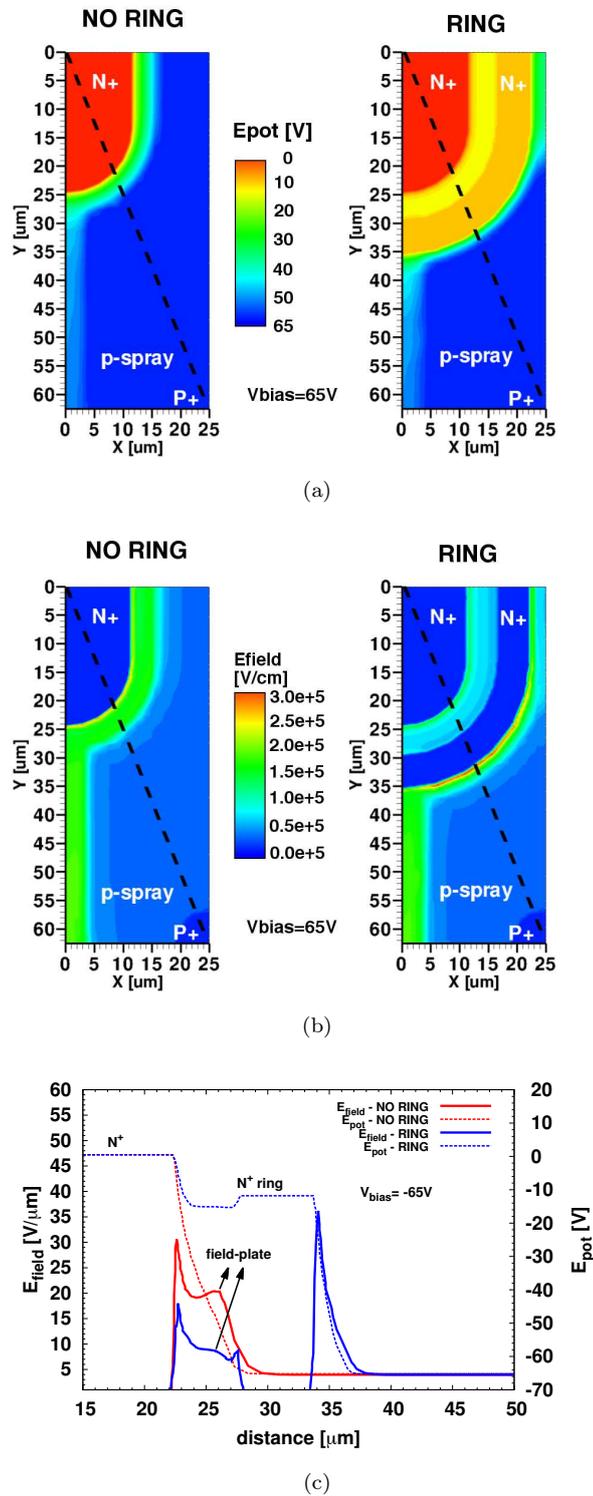


Figure 5.5: Bi-dimensional simulated distributions of the electrostatic potential (a) and of the electric field (b) near the front surface of two FE-I4 3D diodes without (left) and with (right) the floating n^+ ring. The 1D distribution of the same quantities extracted from the diagonal connecting two electrodes of opposite doping types is also reported (c) [142].

field peak on the outer p-spray for the structure featuring the n^+ ring, can be observed at a coordinate of about $34 \mu\text{m}$. This peak is larger than the others and it is already very close to the critical value of $40 \text{ V}/\mu\text{m}$, finally causing the structure to discharge earlier than expected. This effect was feared but, due to space constraints caused by the very short pixel pitch of the ATLAS devices ($50 \mu\text{m}$ in the lateral direction), the ring could not be placed differently and, due to the limitations in feature size related to the standard lithography processes, its dimension could not be further reduced. In order to obtain the optimal performance of this layout feature, a larger ring to n^+ island distance would be needed, leading to a more homogeneous electric field redistribution. The only device which could have allowed for a different ring placement was the CMS 1E type structure but, in order to have consistency between the different layouts, it was decided to leave it unchanged. Although it was not possible to fully exploit the improvements brought by the floating ring, it is important to stress that this layout detail could play an important role in increasing the pixel shielding from surface currents and defects, especially after heavy irradiation.

In addition to the layout modifications just described, some new slim-edge implementations were also tested with the aim of further reducing the dead area along the edges (see next section). The layout of the DTC-5 batch was finalized in May 2012 and the fabrication started immediately after. A large number of devices were implemented and in particular: (i) 4 FE-I4 pixel detectors in two different configurations, (ii) 26 CMS pixel detectors in 8 different configurations, (iii) 8 DC coupled, $80 \mu\text{m}$ pitch, strip detectors, (iv) 2 MedipixII pixel detectors and (v) several planar and 3D test structures. A few modifications were introduced in the fabrication process as well, in order to achieve faster sensor delivery. These modifications will be very briefly described in section 5.4.

5.3 New slim-edge implementation

As it was proven during the previous studies reported in Chapter 4 subsections 4.4.2 and 4.6.1, the design of the slim-edge implemented in the IBL production batches could be optimized to further reduce the edge extension to roughly $100 \mu\text{m}$, without compromising the correct operation of the sensors. For this reason it was decided to reduce the slim-edge extension in the z direction by $50 \mu\text{m}$ leading to a total dead area of $150 \mu\text{m}$. This was a conservative choice made in order to avoid problems coming from uncertainties in the diamond edge cutting procedure. A comparison between the old slim-edge (DTC-4) and the new one (DTC-5) implemented in FE-I4 pixel sensors can be observed in Fig.5.6. Additionally to the $50 \mu\text{m}$ reduction in the extension of the slim-edge, the first column outside the active area was moved to a position in which it will be directly in front of

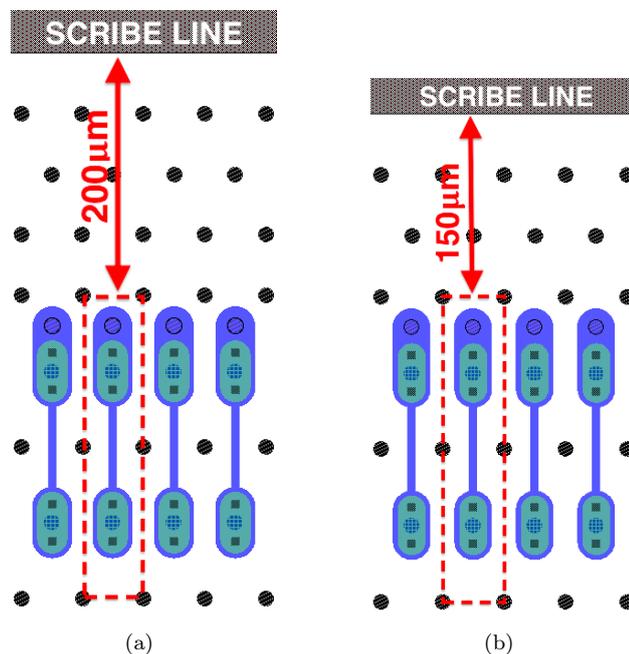


Figure 5.6: Comparison between the slim-edge implementation in the z direction in the DTC-4 layout (a) and in the DTC-5 layout (b).

the junction column of the edge pixel, in order to provide a better containment of the depletion region.

Apart from the described reduction in edge extension applied on pixel detectors (and also on 3D diodes), several different edge termination solutions were studied with numerical simulations [143]. Since the previously studied and implemented fence of ohmic columns proved to be very effective in stopping the depletion region to laterally grow toward the cut region, a different version of the same concept was implemented. The main idea was to replace the slim-edge p^+ columns with a series of equally spaced short and narrow p^+ trenches that should be more efficient in delivering the same result, without requiring the use of a support wafer. A possible implementation of this idea is shown in Fig.5.7 and 5.8, the only difference being that in one case a single row of trenches is used while in the other a double row of trenches is realized. In both cases the edge region is reduced to a remarkable $50 \mu\text{m}$. The structures here reported were simulated for an $80 \mu\text{m}$ pitch diode because of its well understood behavior and more regular layout, but could be adjusted to fit almost any device geometry.

The numerical simulation is performed in the same way as it was for the previous version of the slim-edge because the obtained results were confirmed to be extremely accurate. The cut region is modeled with the usual low lifetime region ($<1 \text{ ns}$) and the p^+ structures are swept from zero to very large biases, while grounding the n^+ electrodes.

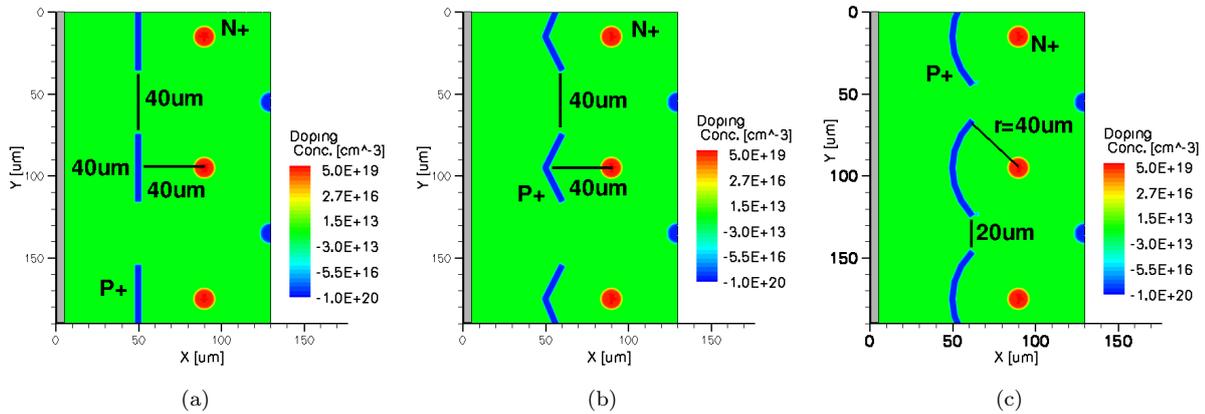


Figure 5.7: Simulated structures for the new slime-edge implementation featuring a *single row* of p^+ trenches instead of a fence of ohmic columns. Different trench shapes where implemented: rectangular (a), triangular (b) and round (c) [143].

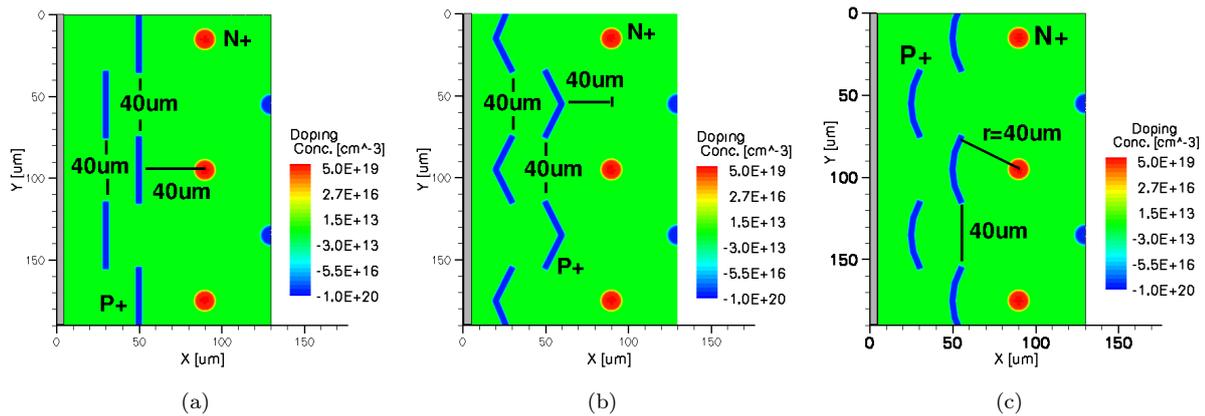


Figure 5.8: Simulated structures for the new slime-edge implementation featuring a *double row* of p^+ trenches instead of a fence of ohmic columns. Different trench shapes where implemented: rectangular (a), triangular (b) and round (c) [143].

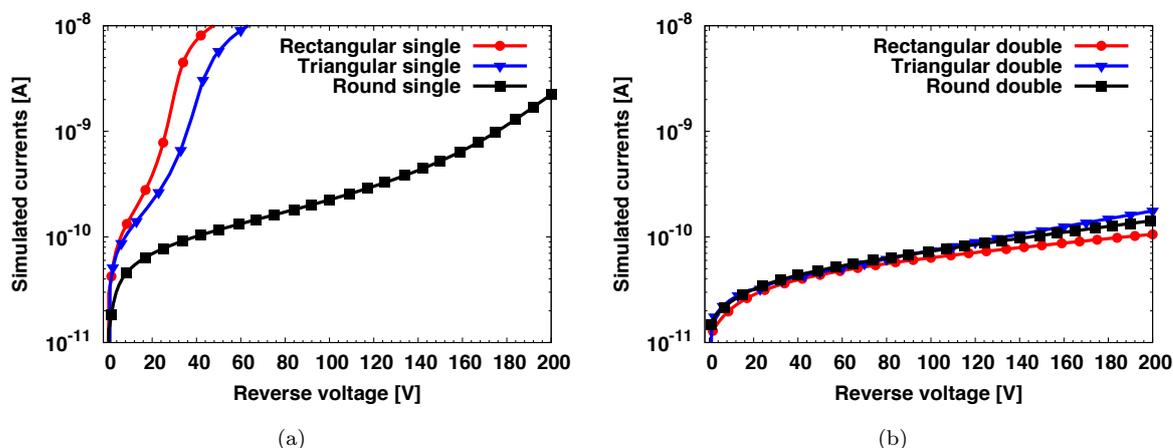


Figure 5.9: Simulated reverse currents for all the different new implementations of the slim-edge: results for both the single row of trenches (a) and the double row of trenches (b) are both reported [143].

The avalanche models are disabled to avoid interference with the studied phenomena. The simulated reverse currents for all the investigated structures are reported in Fig.5.9. As can easily be observed in Fig.5.9(a), in the case of a single row of trenches none of the implemented layouts seems to operate properly, showing premature current increases that prevent the devices to be properly operated. Only in the round trenches case, this effect seems to be less important. The reason for this result can be understood by looking at the hole density distribution reported in Fig.5.10 for a bias voltage of 50 V. The depletion region, indicated as the region where the amount of holes is lower, can easily reach the cut region in both the rectangular (Fig.5.10(a)) and in the triangular (Fig.5.10(b)) cases. This does not happen as quickly for the round case (Fig.5.10(c)), but it will happen as the bias voltage increases. The breakdown voltage in the newly designed devices is expected to be considerably higher than before, so it is not sufficient to assure the correct operation of the slim-edge up to low voltages, therefore the single trench configuration was discarded. On the other hand, by observing Fig.5.9(b), none of the implemented configurations seem to suffer from edge related current injections up to very large voltages. The reason for this is well understood examining the hole density distributions in Fig.5.11 ($V_{bias}=50$ V). It appears that, by properly fixing the distance between the two rows of trenches, it is possible to achieve a sort of "pinch-off" effect of the depletion region, allowing to assure the slim-edge operation up to very large voltages. Having proved that the "double trench" structures should be effective, they were implemented on a set 3D diodes with $80 \mu\text{m}$ pitch, in order to repeat the electrical and functional tests described in the previous chapter.

The only concern about the realization of these structures was that, in order to maintain the fabrication complexity low, they will have to be fabricated together with

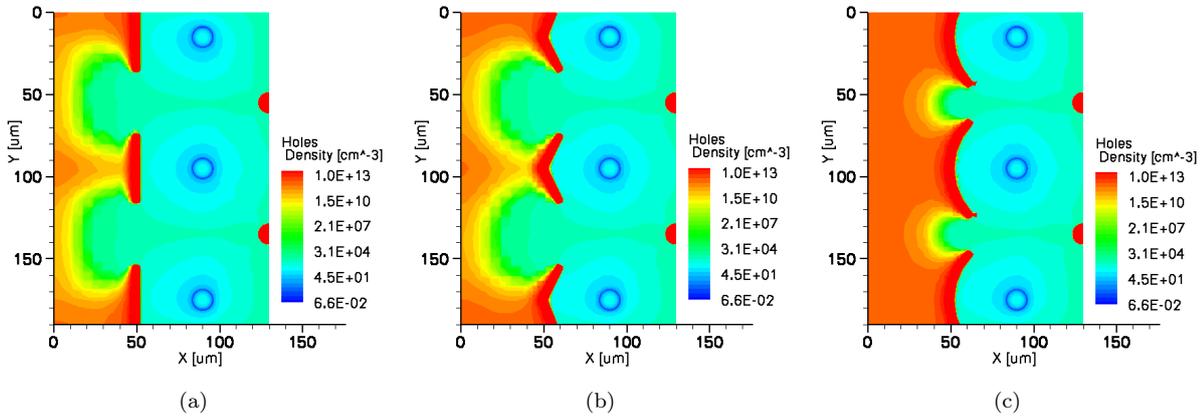


Figure 5.10: Simulated hole density distribution for the new slime-edge implementation featuring a *single row* of p^+ trenches instead of a fence of ohmic columns for a bias voltage of 50 V: rectangular trenches (a), triangular trenches (b) and round trenches (c) [143].

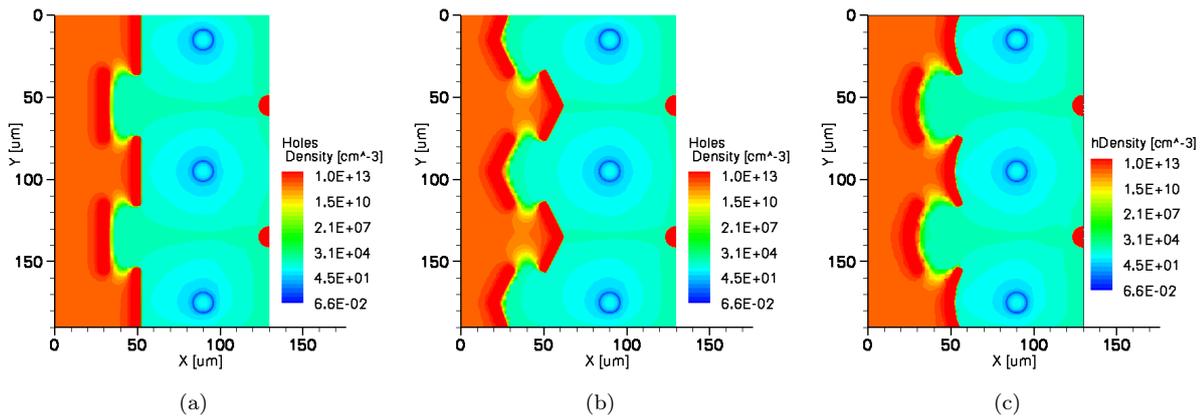


Figure 5.11: Simulated hole density distribution for the new slime-edge implementation featuring a *double row* of p^+ trenches instead of a fence of ohmic columns for a bias voltage of 50 V: rectangular trenches (a), triangular trenches (b) and round trenches (c) [143].

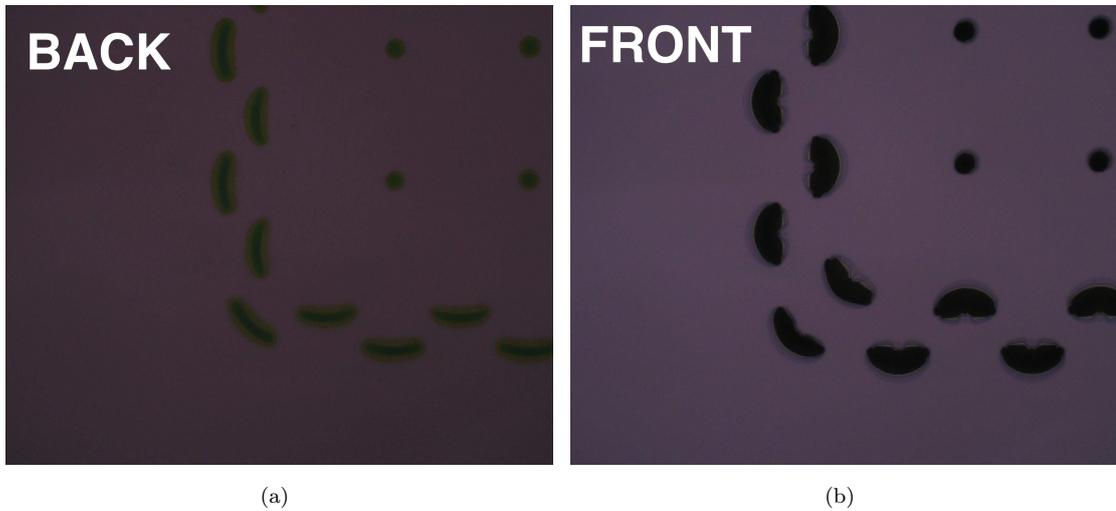


Figure 5.12: Round double row trenches etched during the fabrication process. The structure definition on the backside is very good (a) and it is roughly maintained also after the etching reaches the front side (b). Columnar electrodes are successfully etched at the same time.

the p^+ columnar electrodes (e.g. same etching step and same doping step). As already stated, when etching structures featuring rather different geometries, the etching times can be considerably different. Luckily, designing the trench width sufficiently narrow with respect to the radius of the columns, proved to be an efficient strategy to obtain comparable etching times. This concept was tested before the fabrication of the new batch and the etching results were also optically investigated very carefully during the process. In particular, two pictures of the etched trenches are reported in Fig.5.12, showing that it is possible to maintain the trench conformity both on the front and on the back surfaces and, at same time, etch fully passing through columnar electrodes. These results were also achieved by slightly modifying the DRIE process parameters toward the end of the etching, thus assuring similar etching times for both structure types. An example of this is reported in Fig.5.13, where the final part of a passing through p^+ column is visible: the region where the DRIE parameters were modified is clearly marked by the increased "scaloping" effect.

5.4 Process modifications and device fabrication

The modifications discussed in the previous section should result, not only in large voltage handling capabilities of the devices, but also in a considerable complexity reduction from the point of view of the fabrication process.

The modification that definitely helps in reducing the process complexity is the

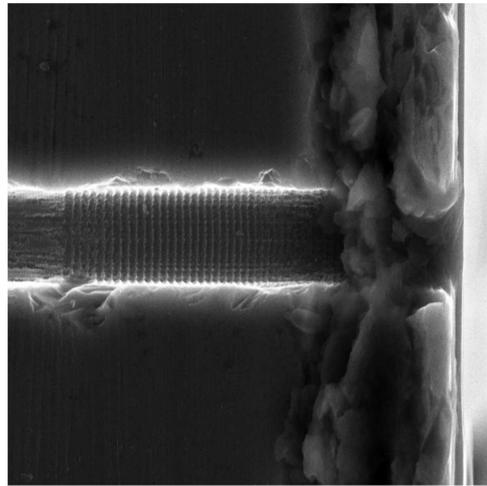


Figure 5.13: Detail of the final region of a p^+ columnar electrode obtained with the modified DRIE process developed to assure similar etching times between columns and small trenches. The "scalping" effect, more visible on the right, is the result of the modified process parameters.

shortening of the junction columns. As already explained, this removes the critical region on the backside of the sensor but also has other advantages: (i) it removes the need for the patterning of the backside and (ii) makes the p-spray implantation on the backside of the wafer not necessary anymore. Making the backside uniform has several advantages both in terms of fabrication speed and cost: several lithographic steps, such as the definition of the p^+ geometries and contact openings on the back side, can be avoided and the relative masks are not necessary (thus also partially reducing the overall cost). Additional easing would come from making the back side metal uniform as well, but this is not possible because of the need for bump bonding alignment markers.

An additional modification to the process was implemented in order to speed up sensor production. In the IBL batches the doping of the surface n^+ regions was made by implanting phosphorus Ions with a dedicated step. An additional phosphorus implantation was performed inside the front side contact holes, to increase the surface doping concentration and produce better contacts with metal. This last step was a direct consequence of the lowering of the peak doping concentration due to the several thermal processes the wafers went through before reaching the end. In the new batch, the process was designed to perform the doping of the surface junctions together with the doping of the n^+ columnar electrodes using thermal diffusion from a phosphorus solid source. By doing so, it was possible to remove two process steps (lithography and doping of the surface n^+ regions). This particular doping modality should also result in a higher surface doping concentration making the additional implant inside the contacts not strictly necessary (as a security measure the implant was performed only on some wafers).

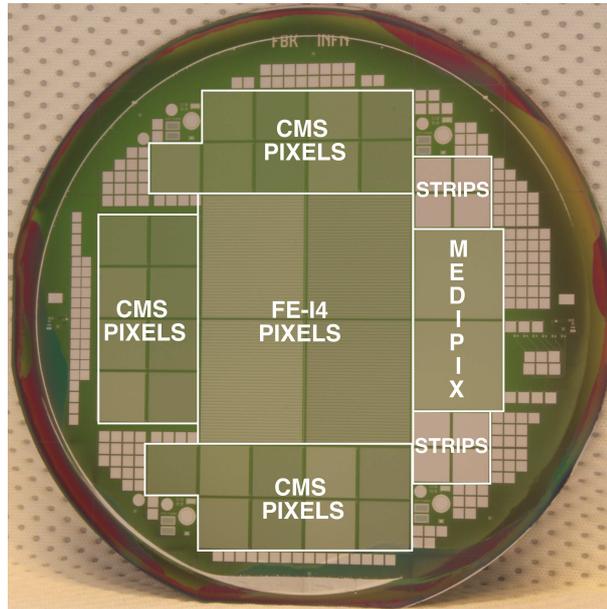


Figure 5.14: Picture of one of the fabricated wafers from the latest 3D batch at FBK with the DTC-5 wafer layout [142].

The fabrication started in June 2012 and was completed in a little more than four months, with completed wafers delivered in mid October 2012. The picture of one of the fabricated wafers is reported in Fig.5.14 also showing the placement of the most important devices. All around them it is possible to see the very large number of implemented 3D diodes in many different configurations in order to test all the implemented layout modifications.

Unfortunately, an unforeseen complication manifested itself during the fabrication: a wafer bowing as high as $500\ \mu\text{m}$ (with respect to a wafer thickness of $230\ \mu\text{m}$) was measured. This actually caused a lot of complication in completing the batch and also resulted in a rather poor electrical yield, as will be explained in the next section. The used edge protection was proven to be effective in preventing the bowing in the previous batches but, in this case, it is believed to have failed because of the asymmetry between the front and back sides (the back side is not patterned anymore).

5.5 Electrical characterization of new devices

As expected, the large wafer bowing resulted in quite large current densities due to the stress and modifications induced on the silicon lattice. Current densities in the order of $0.5\ \mu\text{A}/\text{cm}^2$ and breakdown voltages of roughly $100\ \text{V}$ were measured on planar test diodes. This was not very promising and, in fact, the electrical yield on pixel detectors

was very low. The electrical characterization of pixels and 3D diodes was performed using the temporary metal (as in IBL batches) at the automatic probe station. Measurements on 3D diodes were also automatically performed after temporary metal removal, but no great modifications were observed. Nevertheless, a sufficient number of 3D diodes showed acceptable performances and an extensive campaign of I-V measurements of good devices is being performed and data are being analyzed. As an example Fig.5.15 shows the measured IV curves of some 3D diodes in different FE-I4 configurations. Luckily, the numerical simulation predictions were correct and devices actually show breakdown voltages larger than 70 V with a few of them apparently reaching 125 V. A few devices manage to reach 200 V by they are believed to show soft breakdown around 80 V were a "kink" in the curve can actually be observed. In order to understand if a trend with different layout implementations is observable, all the I-V measurements from good devices need to be collected and plotted, in order to have sufficient statistics. This is a rather slow process and will require some time. In addition to these devices, some of those with the modified slim-edge show good characteristics and will be used for electrical and functional characterization of the new termination, as soon as the wafers will be available for cutting.

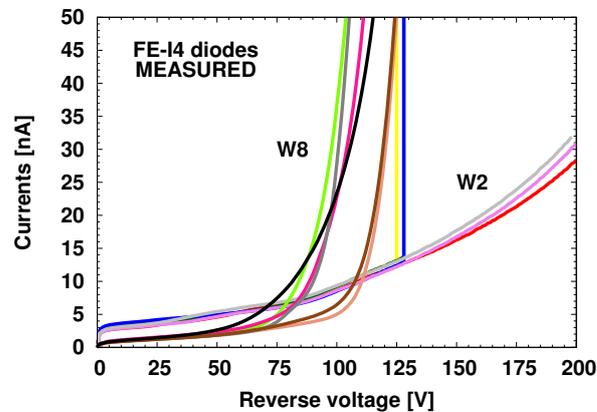


Figure 5.15: Preliminary I-V measurements performed on FE-I4 3D diodes from two wafers (W2 and W8) of the newly fabricated sensor batch [142].

In conclusion, this new sensor batch was unfortunately not fully successful, but the cause for the poor yield was identified. The immediate repetition of the fabrication with the adequate corrections is not possible because the clean room at FBK is now closed in the process of upgrading it to process 6" wafers. The operation will restart in early 2013 but the 3D process will need to be re-calibrated on larger wafers, operation that might require a few months.

Chapter 6

Additional applications of 3D technology

The activities focused at the design, production and characterization of 3D pixel detectors for the ATLAS IBL, not only helped in making the technology grow to its maturity, but also opened the doors to other applications in particle physics and in other fields as well. The DRIE process is now well controlled and integrated in the fabrication process and allows to also realize structures different from columnar electrodes.

This chapter will briefly describe some additional application of 3D technology at FBK, discussing how the technology can be adapted to produce different devices. Some preliminary results for each discussed application will also be shown.

6.1 The ATLAS Forward Physics

In addition to the installation of the IBL, the ATLAS collaboration is planning to install additional tracking stations both upstream and downstream the experiment, with the intent of identifying and record events with leading intact protons emerging from diffractive collisions [144].

The ATLAS Forward Proton (AFP) detectors, both upstream and downstream, will be placed at about 210 m from the ATLAS interaction point, divided into two different detector boxes, one at 206 m and the other at 214 m, as shown in the sketch in Fig.6.1. In the first station (AFP1) it is planned to install a small pocket containing 6 layers of silicon tracking detectors, to reconstruct the trajectory of the scattered protons. In the second station (AFP2), another pocket containing silicon detectors is planned and, in addition, one containing a timing detector.

For this specific application, the proximity to the beam is crucial, so the plan is to remove a section of the current beam pipe and replace it with a Movable BeamPipe (MBP)

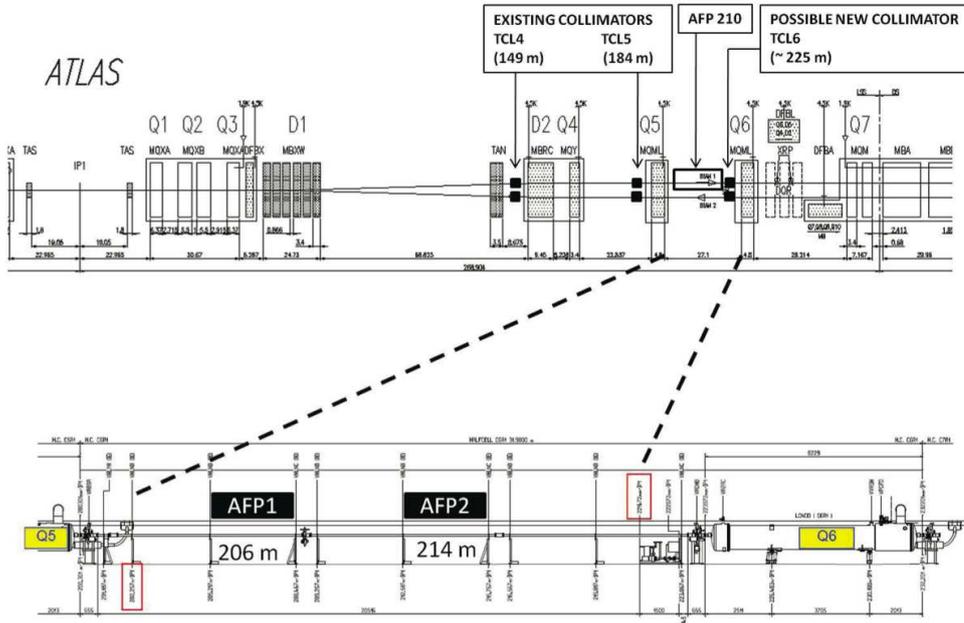


Figure 6.1: Sketch of the LHC beamline region where the installation of one arm of the AFP detector is planned [144].

also known as Hamburg BeamPipe (HBP). Based on a design successfully deployed at DESY in 1995 [145], the movable beam pipe should allow to keep the AFPs away from the beam during the injection and bring them very close when the beams are declared stable. A possible layout of the MBP is reported in Fig.6.2, where the two crucial regions are highlighted: the window and the floor. To assure the proper operation of the AFP stations, it is crucial to deliver the lowest possible thickness for both the window and the floor of the beam pipe, the former to avoid additional proton scattering and the latter to minimize the detector distance from the beam. The proposed thicknesses for the window and the floor are currently 250 and 300 μm respectively [144]. Because of the use of such thin material, electronics and sensors are planned to be installed in sealed containers integrated into the beam pipe in which secondary vacuum should be maintained, in order to prevent possible issues related to the breaking of the beam pipe vacuum.

As previously stated, silicon pixel detectors will be used to measure several points along the track of the scattered protons. This, combined with the LHC dipole and quadrupole magnets, forms a powerful momentum spectrometer. The distance between sensors and beam, will determine the minimum fractional momentum loss of detectable protons, so it is crucial to be able to minimize it. To this purpose, special requirements were set for silicon detectors:

- Spatial resolution in the x (y) direction of about 10 (30) μm per detector station.

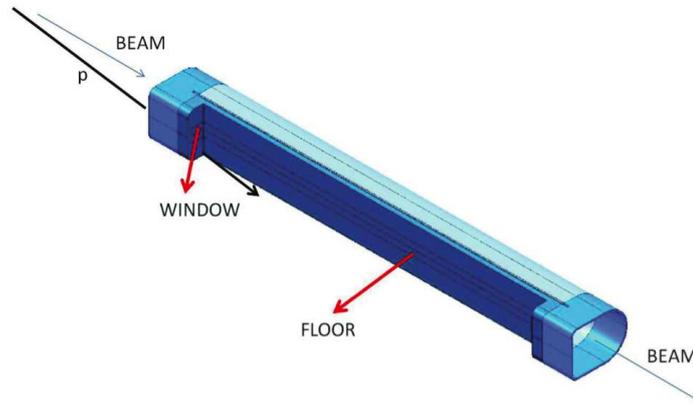


Figure 6.2: Tentative layout sketch of the AFP movable beam pipe [144].

- Angular resolution between a pair of modules equal to 1 rad.
- High efficiency on a $20 \times 20 \text{ mm}^2$ area.
- Minimum dead area extension at the edge.
- High radiation hardness.
- Able to operate at LHC luminosity.

The IBL pixel sensors satisfy all these requirements and, in particular, 3D detectors show several advantages especially in terms of the very small edge region achievable and radiation hardness (as will be shown in the next subsections). Due to their very good performance and their availability, 3D sensors are currently considered the baseline technology for the AFP installation, planned for the long shut of 2017-2018 that will bring the LHC to Phase-1. Because of the peculiar placement of the considered modules inside AFP, a main concern come from the rather un-homogeneous irradiation devices will withstand, with the region closer to the beam receiving a considerably larger dose than the rest of the device. In addition, it is necessary to find a reliable way to reduce the current edge extensions of the IBL prototypes to a minimum. Both these issues will be addressed in the following subsections.

In addition to tracking detectors, also a timing detector is planned. This should allow to measure the time difference between outgoing scattered protons and could be used to reject overlapping background, by establishing that two scattered protons did not origin from the same vertex [144]. Stringent requirements have been placed also on the timing detector:

- A timing resolution of 10 ps or better.
- Acceptance comparable to that of the silicon tracking devices.
- Sufficient granularity in order to avoid pile-up.
- It should have triggering capabilities.

The detector currently considered for the installation is the so called QUARTIC detector. It is a quartz device based on a Cerenkov detector coupled to Micro Channel Plates (MCP) and Photo Multiplier Tubes (PMT) [146].

6.1.1 3D pixel detectors in un-homogenous irradiation conditions

Because of the specific operating mode of silicon devices inside the AFP stations, one side of the devices will be closer to the beam with respect to the others, causing the sensor irradiation to be not uniform. As a consequence, the part of the sensor placed closer to the beam will require larger biases to be operated in the most efficient conditions. At the same time, the oxide charge will greatly increase in the more irradiated part of the device while it will remain almost unchanged elsewhere. As a result, the sensor maximum operating voltage might be limited by the low irradiated region that, breaking down too early, will cause the impossibility of operating the device at the proper bias.

A preliminary investigation of these operating conditions for 3D devices fabricated at CNM is reported in [148]. Two IBL 3D pixel assemblies were un-homogeneously irradiated at the IRRAD1 facility at CERN-PS, and were later electrically and functionally characterized in a beam test with 120 GeV pions at the CERN SPS H6 beam line in August 2012. The maximum fluences received by the two devices are 4 and 9.4×10^{15} n_{eq}/cm^2 . The operating conditions in the AFP are similar to those in the IBL so devices were tested at -15°C and at the maximum possible operating voltage. The device irradiated at the lower fluence showed a very good efficiency in the un-irradiated region (98.9%) and a lower efficiency in the irradiated one (92%). This low efficiency was mainly related to defective and dead pixels in the readout chip due to the high radiation dose received. By removing defective pixel in the post processing phase it was possible to increase the efficiency of the irradiated region up to 98%. The other device was very difficult to operate because of the large radiation induced leakage current. The preliminary results are interesting and further tests are being performed.

6.1.2 Reduction of the edge extension in IBL 3D pixel sensors

The IBL devices were designed to have slim-edges in the z direction and no constrain were set for the others because modules will be overlapped in $r-\phi$. In the AFP, the side closer to the beam is one of those that are not designed to be slim. In particular, as previously described in Chapter 4 subsection 4.2.2, one of the other two sides are has a 1 mm extension in order to fit the large bias tab needed to bias single sided 3D sensors.

In order to obtain AFP compatible devices, a way of reducing the large dead area at the desired edge is needed. Two approaches are currently being investigated: (i) a

laser scribing followed by manual cleaving and side wall passivation and (ii) the regular diamond saw cutting procedure. Both approaches are briefly described in the following paragraphs also citing the most relevant results.

Laser scribe, cleave and Alumina sidewall passivation

This technique is relatively recent but is showing very interesting results. It features a partial high quality laser cut (less chipping and dangling bonds), followed by a manual cleaving and a sidewall passivation performed with Alumina [147]. This technique is particularly interesting for silicon detectors realized on p-type substrate because Alumina features negative trapped charge that, by attracting positive charge at the silicon/alumina interface, will result in a complete passivation of the side wall.

This technique was tested on CNM pixel detectors compatible with the FE-I3 readout chip [148]. The edge dead area was reduced from the initial ~ 1 mm to widths in the order of 50-100 μm . Out of seven detectors, only two featured a bad behavior after cut, probably due to the cut being too close to the active area. All the other devices showed high breakdown voltages and good leakage current. In addition, charge collection tests were performed using a ^{90}Sr radioactive source. Devices showed full charge collection at ~ 10 V.

The same tests were also performed on 3D diodes fabricated at FBK with very similar results. Unfortunately full functional results are not available yet.

On a side note, although this approach is very promising, the radiation hardness of the Alumina passivation layer is yet to be assessed. In particular, the amount and the sign of the Alumina trapped charge after irradiation needs to be investigated in order to assure that the passivation is still effective also after heavy irradiation.

Diamond saw cut

The same procedure described in Chapter 4 subsection 4.4.2 was repeated also on FE-I4 pixel detector but on the edge relevant to the AFP operation. In order to ease the testing, one of the bad pixel sensors was used. Since, as previously explained, bad sensor normally present only one defective temporary metal strip, a few good strips were detected on the device prior to cutting and then the multiple cut procedure was applied. The most relevant results are reported in Fig.6.3. The performed cuts are shown in Fig.6.3(a) and the measured currents for two different strips are shown in Fig.6.3(b) and 6.3(c). These results are comparable with those obtained with the same procedure on the other sensor edge. In this case it is actually possible to cut roughly 25 μm closer to the active area, in fact the reverse current of the measured strips doesn't show any premature discharge up to the sixth cut, corresponding to an edge extension of roughly 75 μm .

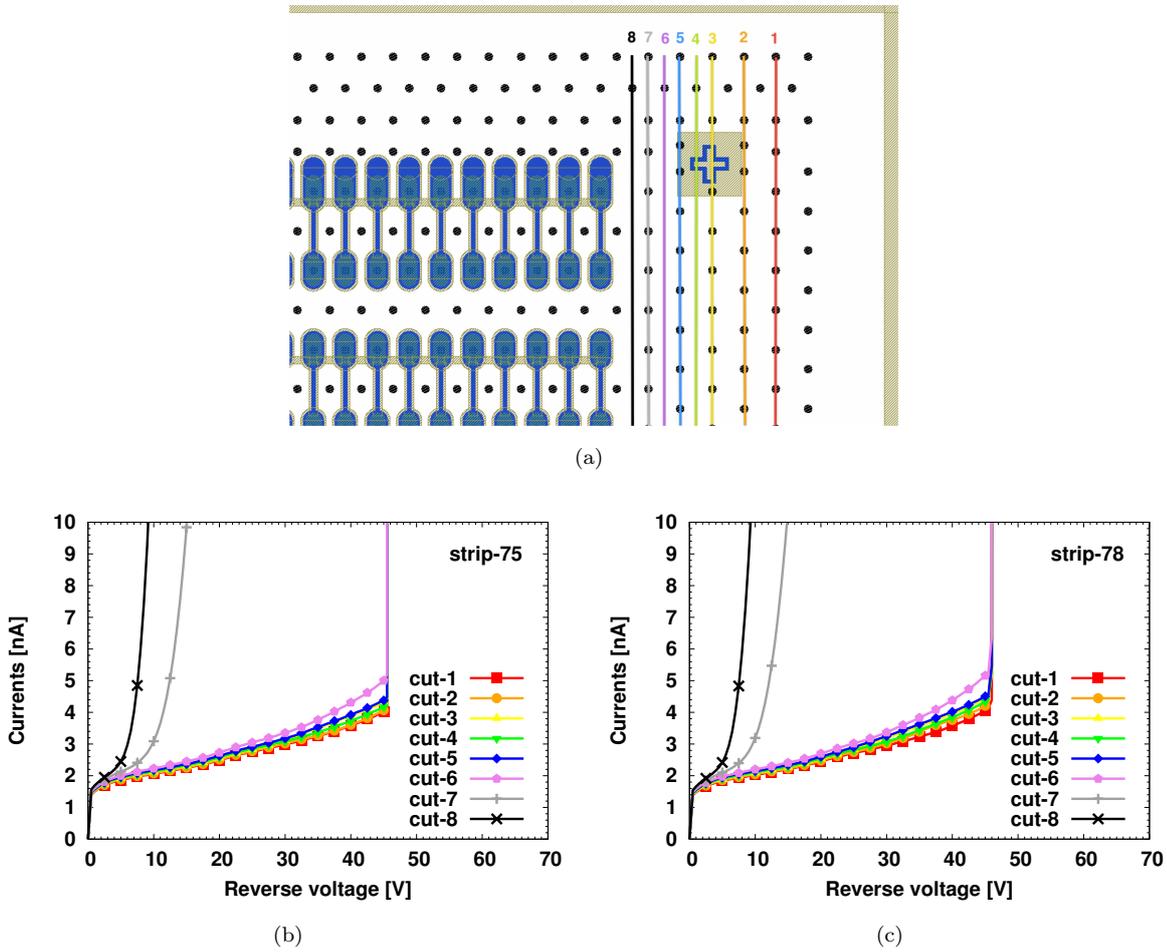


Figure 6.3: Results of the performed electrical characterization of the slim-edge region for AFP performed on FE-I4 pixel detectors fabricated at FBK. The sketch of the performed cuts are shown in (a) and the reverse currents measured on two different temporary metal strips after each performed cut are shown in (b,c).

A few pixel detectors, from both FBK and CNM, with the Under Bump Metal already deposited at IZM, were sent to FBK for dicing (on the sixth cut), and were later sent back to IZM for bump-bonding to the FE-I4 readout chip. The characterization of bump-bonded assemblies will be performed at CERN.

It is important to notice that, in the DTC-5 layout described in Chapter 5, all FE-I4 Pixel sensor were already designed with reduced slim-edges also on the side needed for AFP (a total extension of $200 \mu\text{m}$). Unfortunately the amount of good sensors is very low and does not justify the cost needed for bump-bonding. The new termination structures will be tested on 3D diodes and, in case of success, they will be implemented on a new batch when production will restart at FBK after the clean room upgrade.

The preliminary results obtained with 3D pixel detectors compatible with the FE-I4 readout chip in the AFP configuration are very encouraging. A more complete campaign of irradiation and testing also on devices featuring minimal edge extension will be performed in the next months.

6.2 Planar detectors with active-edges

The edge termination techniques so far described in this work are fairly recent. The ohmic fence slim-edge was developed specifically for IBL pixel detectors and proved to be efficient, while the Scribe-Clive-Passivate (SCP) method, is more recent and its performances have still to be proven in all the forecasted operating conditions.

The edge termination is definitely not a new topic in the field of silicon detectors. In the past years, several different approaches to this layout detail were proposed, with the specific aim of preventing the injection of spurious currents coming from the cut edge into the active sensor area. In standard planar processes, where large bias voltages are required, most of the edge terminations require to keep the junction electrodes far away from the scribe lines (0.5 to 1 mm), in order to fit multiple guard-rings allowing to gradually drop the bias voltage from the active area to the edge [149].

In the attempt of reducing this large dead area at the edge, several techniques are available and among them are laser cutting procedures resulting in cleaner and less damaged cut edges [150], and current terminating structures which prevent the edge leakage current to reach the active area [151].

A new and very effective solution to eliminate any cut related spurious currents and, at the same time, drastically reduce the extension of the dead edge area, is the *active-edge*. The active-edge is an additional feature of 3D technology (as explained in Chapter 3 section 3.1) and it consists in a deep and narrow trench etched with the DRIE process and then doped and filled with polysilicon [71]. In addition to 3D detectors, the active-edge can easily be applied to standard planar devices with only a moderate complication in the fabrication process (a support wafer is necessary to keep the pieces in place during fabrication). In fact, the ability of this method to reduce the edge region extension down to a few tens of microns, was successfully proven by means of X-ray beam scans on planar strip sensors [152, 153]. Besides the complications in the fabrication process, the active-edge presents an additional drawback: being the edge trench normally very close to the readout electrodes, the distribution of the electric field at the edge is partially distorted, possibly leading to charge collection inefficiencies especially in segmented detectors. This effect was indeed observed in planar detectors with active-edges compatible with the MedipixII readout chip and fabricated at VTT, Finland [154]. Depending on the detector

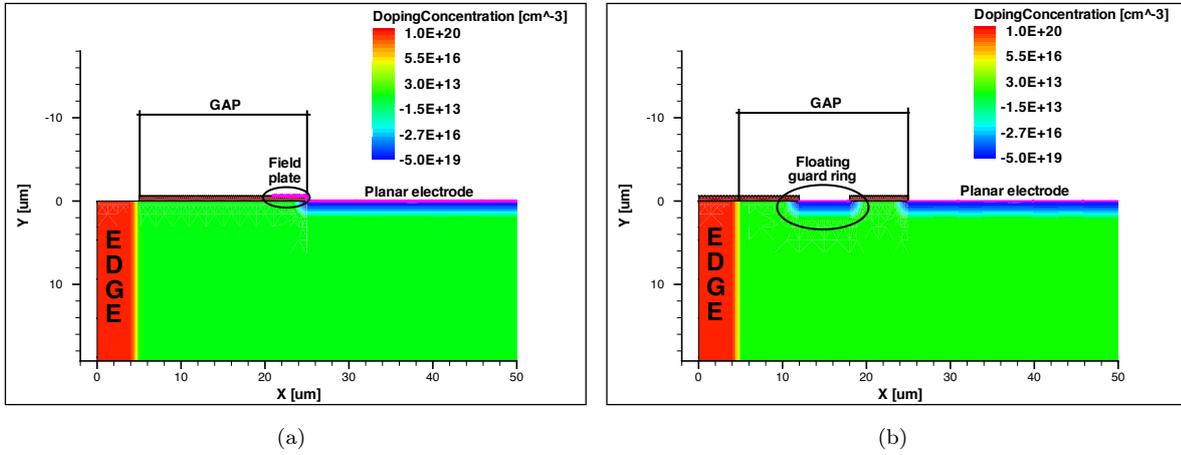


Figure 6.4: Details of the structures used in the numerical simulations: planar diode with active-edge and field-plate (a) and planar detector with active-edge and floating p^+ ring [155].

structure (e.g. n-in-p, p-in-n or n-in-n) the field distortion can either lead to enhancement or reduction of the charge collected by the edge electrodes. However, this effect can easily be quantified and corrected during data acquisition or in the post-processing phase.

In addition to the many activities performed at University of Trento and FBK in the framework of the projects related to the design and fabrication of 3D sensors, a batch of planar detectors with active-edges was also produced [155]. The design of the sensors was performed with the aid of numerical simulation tools (Synopsys TCAD tools [90]), investigating the best geometrical configuration of several layout details, aiming at maximizing the operating voltage. Devices were fabricated at FBK in 2010 and the characterization started soon after. The most important results from the design and testing points of view are here discussed.

6.2.1 Computer aided design

In the design of active-edge structures the most important parameter to keep in mind is the distance between the outer junction electrodes of the active area and the highly doped trench. If this distance is too short, it will cause a dramatic reduction in the maximum operating voltage of the devices, leading to the impossibility of reaching full depletion even after moderate radiation doses. As already discussed in Chapter 4 and 5 in relation to the design of 3D detectors, the use of field-plates and floating rings (or a combination of the two) can lead to a noticeable improvement in the voltage handling capabilities and, for this reason, the consequences of the same layout details were also studied during the design of the batch of planar detectors with active edges. Fig.6.4 shows two example structures used in the simulation process: Fig.6.4(a) represents a planar p-in-n diode with active edge and

field-plate, while Fig.6.4(b) shows the same device but without field-plate and with the addition of a planar floating p^+ ring. In both structures, the edge to main junction distance is indicated with "GAP". Simulations were performed in 2D, the considered n-type bulk thickness was $200\ \mu\text{m}$, and parameters such as the GAP, the oxide trapped charge and the field-plate length were parametrized in order to find the configuration delivering the best performances. The GAP distance was varied between 10 and $40\ \mu\text{m}$, the field-plate length between 3 and $24\ \mu\text{m}$ (where the GAP size allowed longer extensions) and the oxide charge in the range from 1 to $5 \times 10^{11}\ \text{cm}^{-2}$. In order to speed up the simulation process of all the many geometrical configurations, a simplified breakdown analysis was used, as suggested from the Synopsys manual. Using this method, the simulator calculates the ionization integral and returns a breakdown condition when it reaches a value of 1. This method is fast and less CPU consuming but it usually underestimates the breakdown voltage (it is, therefore, a conservative method).

The very first simulations were performed on a simple diode with active-edge (i.e. no field-plates or floating rings were implemented) in order to have an initial benchmark. Successively, the same structure was modified to include the floating ring and the field-plate. The breakdown voltages obtained for these two structures are reported in Fig.6.5. The trend obtained for the simple diode (Fig.6.5(a)) indicates larger operating voltages for large GAPs (as expected) and the strong influence of the oxide charge is also observable, with lower charges providing higher discharge voltages (the charge value for a standard planar process on $\langle 100 \rangle$ substrates is expected to be in the order of 1×10^{11}). The addition of the floating ring (Fig.6.5(b)) starts producing appreciable effects for GAP sizes larger than $20\ \mu\text{m}$, and for higher oxide charge concentrations: for gaps lower than $20\ \mu\text{m}$ the breakdown voltage is dominated by the very short p^+ to n^+ distance. Anyway, considering a standard GAP size of $30\ \mu\text{m}$, breakdown voltages in the order of 150-200 V can be expected, more than enough to safely operate the devices in over-depletion.

The addition of the field plate was studied on structures without floating ring and GAPs of 10, 20 and $30\ \mu\text{m}$. The same oxide charge concentrations were used. The obtained results are reported in Fig.6.6. The usual increase with the GAP size was observed, with highest voltages obtained for the $30\ \mu\text{m}$ GAP. Once again, lower oxide charges translate into higher operating voltages. The effect of the field-plate is really noticeable only for GAPs of 20 and $30\ \mu\text{m}$: on the entire range of the investigated field-plate lengths, the optimal one seems to be in the order of $6\ \mu\text{m}$, for a GAP of $30\ \mu\text{m}$, delivering maximum operating voltages exceeding 200 V and reaching, in the best case, 350 V.

After analyzing all the simulation data, it was possible to outline a set of design guidelines:

- GAPs of $30\ \mu\text{m}$ or more should be used to achieve breakdown voltages of roughly

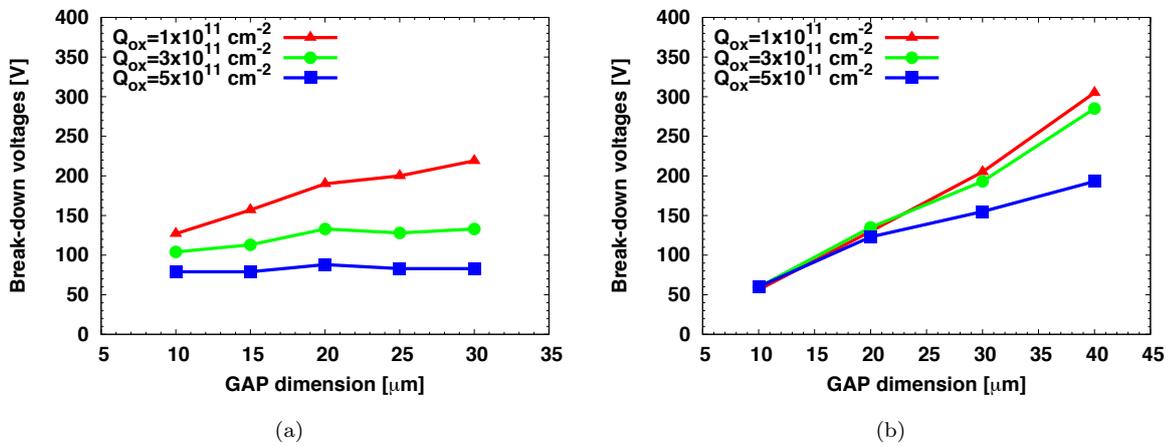


Figure 6.5: Comparison of the simulated breakdown voltage between a simple diode with active-edge (a) and the same device with the addition of a p^+ floating ring (b).

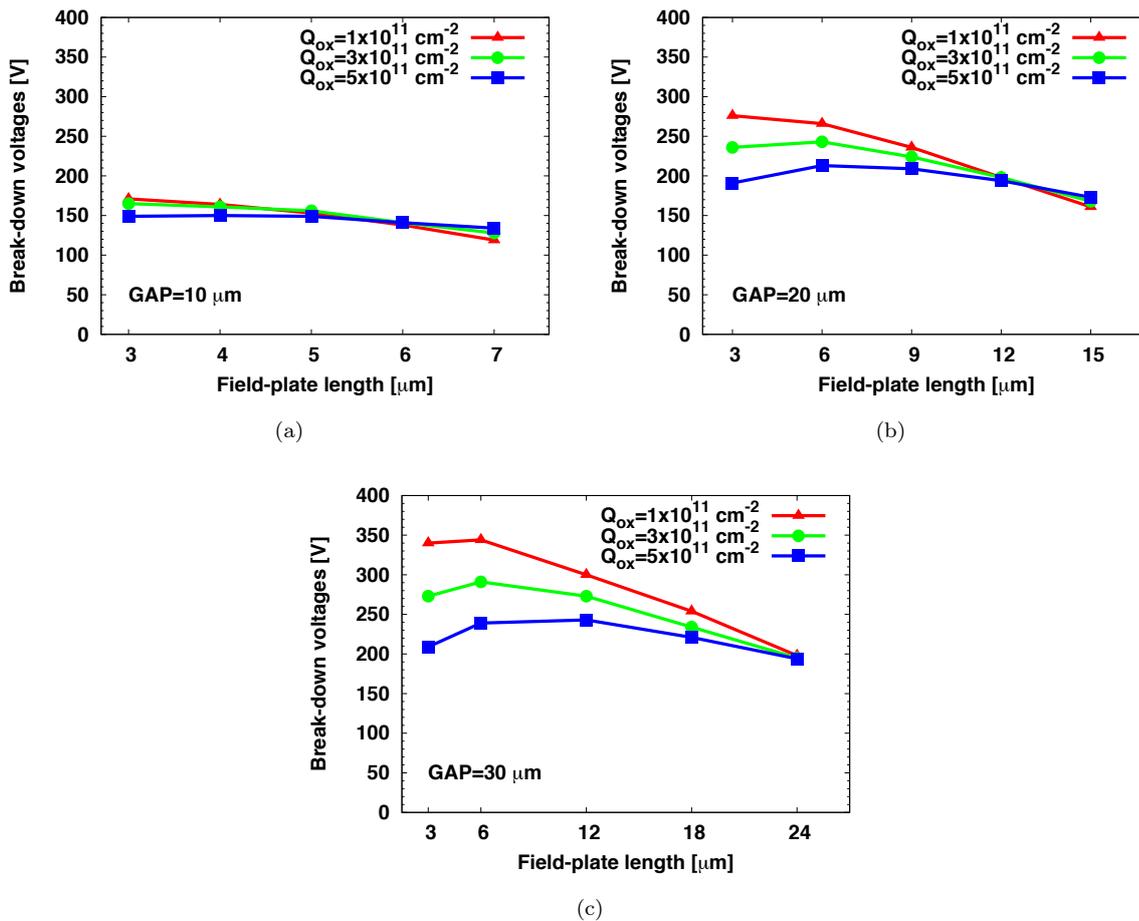


Figure 6.6: Distribution of the simulated breakdown voltages for active-edge diodes as a function of the field plate length and for three different GAP distances: 10 (a), 20 (b) and 30 μm (c).

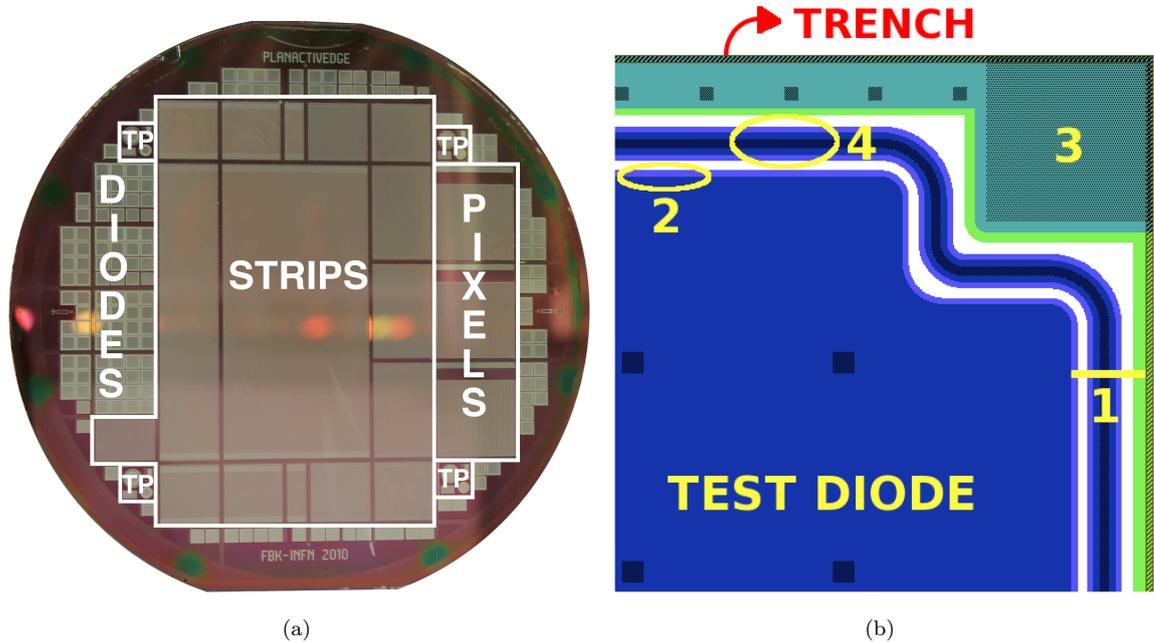


Figure 6.7: Wafer picture of one of the fabricated wafers of planar detectors with active edges (a) and details of a test diode with active-edge, field-plate and floating ring (b). The highlighted regions are: the GAP between the trench and the main electrode (1), the field-plate (2), the bulk bias pad (3) and the floating ring (4) [155].

200 V while keeping the dead area small.

- Introducing a floating p^+ ring inside the GAP region can help in delivering higher operating voltages.
- The more convenient layout designed appears to be the one including a field plate of roughly $5\text{-}6\ \mu\text{m}$.

6.2.2 Wafer layout

A picture of one of the fabricated wafers is reported in Fig.6.7(a) also highlighting the implemented devices: a total of 16 strip detectors are placed in the middle of the wafer, three pixel sensors are placed on the right side, while, all around, a large number of test diodes with different geometrical implementations are placed. As usual, also standard planar tests structures were implemented to monitor the process parameters (indicated with TP in Fig.6.7(a)).

Strip detectors are available in different sizes and with different inter-strip pitches (50 , 80 and $100\ \mu\text{m}$) and can be AC or DC coupled. Pixel detectors are compatible with the readout chips of the pixel sensors currently installed in the ALICE experiment at

LHC. For both strip and pixel detectors, the GAP was designed conservatively to be between 50 and 100 μm . Test diodes come in many different flavors matching the different combinations implemented in the simulations and more: the gap size ranges from 10 to 200 μm , they come both with and without field-plates, having lengths between 3 and 24 μm ; single or multiple floating rings are also implemented (depending on the GAP size). Because of the need for a support wafer, all detectors have a bias pad on the front side, since the back side is not accessible. All the layout details implemented in the test diodes are visible in Fig.6.7(b).

6.2.3 Fabrication process

Although easier than a full 3D process, the fabrication of planar detectors with active-edges includes some non standard steps. Because trenches are fully passing through the sensor wafer, a support wafer is needed. This also helps in increasing the mechanical strength of the processed wafers delivering an higher mechanical yield. Since the wafer bonding machine is not available in-house, this step was performed as an external service at SINTEF (Oslo, Norway).

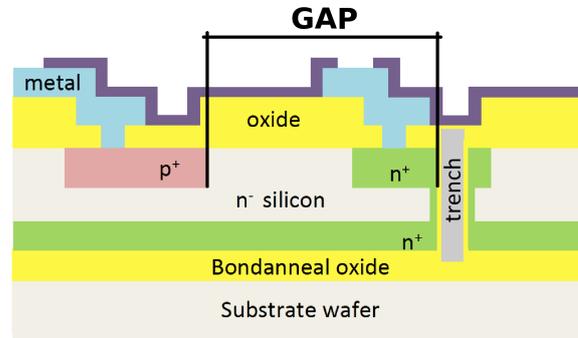


Figure 6.8: Schematic cross-section of a planar device with active-edges fabricated on n-type substrate (not to scale) [155].

Sensors are realized on high resistivity, n-type wafers, with $\langle 100 \rangle$ crystal orientation and a substrate doping concentration of $2 \times 10^{11} \text{ cm}^{-3}$. A schematic cross-section of the fabricated sensor is shown in Fig.6.8. The complete process sequence consists of six lithographic masks and the main steps can be summarized as follows:

1. After marker definition, n^+ and p^+ surface regions are defined and implanted.
2. After growing proper oxide and nitride protection layers, trenches are etched by DRIE and doped with phosphorus diffusion from a solid source (ohmic contact).
3. Trenches are filled with polysilicon to partially restore the wafer planarity and allow for the next lithographic step.

- The final steps are standard and include contact opening, metal deposition and patterning, passivation and sintering.

Because of rather different shape from columnar electrodes, the etching of the trenches turned out to be the most critical step. Etching a long trench is faster than etching a round hole and the strength of the etching mask layers becomes more critical. In the very first processed wafers, the photoresist and oxide layers used as etching masks were not fully efficient and the resulting trenches were larger than their nominal values (from 25 to 30 μm instead of the designed 5 μm , as shown in Fig.6.9(a)). In the second half of the production batch, a better combination of protection layers was adopted and so trenches could be made narrower and better defined (see Fig.6.9(b) where the total trench width is equal to roughly 11 μm).

Another critical aspect related to this sensor technology is the need to fill the etched

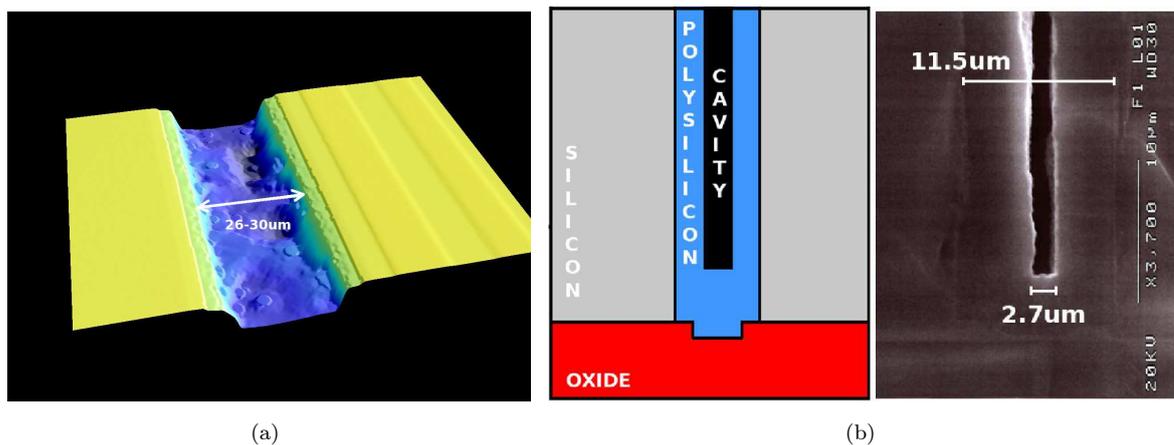


Figure 6.9: Comparison between the bad trenches obtained in the first half of the fabrication batch (a) and the much better trenches obtained after the etch masking layers were optimized (b) [155].

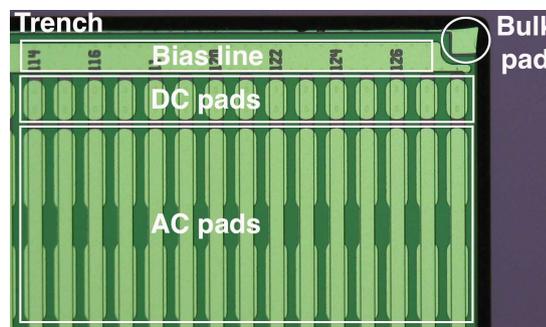


Figure 6.10: Enlargement of the corner of one of the fabricated strip detectors with active-edges. The trench is visible in black on both the top and right sides, in the corner the bulk pad is placed. The AC and DC pads are highlighted together with the bias line [155].

Table 6.1: Most important process parameters extracted from the the measurements on planar test structures: V_{FD} is the full depletion voltage, I_{LK} is leakage current density, τ_g is the bulk generation lifetime, t_{ox} is the oxide thickness, N_{ox} is the oxide charge concentration and s_0 is surface recombination velocity. The original process is the one with non optimized trench widths while the modified process is the one providing better trenches and optimized surface properties [155].

Parameter	Unit	Original process	Modified process
V_{FD}	V	5	5
I_{LK}	nA/cm ²	125-375	150-600
τ_g	μ s	85-255	50-210
t_{ox}	nm	650	600-1050
N_{ox}	10 ¹⁰ cm ⁻²	100	0.2-1
s_0	cm/s	800	10-90

trenches with polyisilicon in order to re-establish the wafer surface planarity and preventing any issues related to the spin coating of the photoresist in the following lithographic steps. After the trench optimization, the quality of the lithography was indeed pretty good as can be observed in Fig.6.10 where a picture of the corner of a strip detector is reported.

6.2.4 Electrical characterization

The electrical characterization was performed at the probe station starting, as usual, from the standard planar test structures. The extracted process parameters are reported in Tab.6.1. Due to the very low substrate concentration, the full depletion voltage was found to be in the order of 5 V. The leakage current densities are not fully satisfactory for a planar process but they are in agreement with what previously found on 3D detectors and might be affected by the problems encountered during the trench etching. Surface parameters in the first part of the process were quite bad but improved when the optimized process was finally adopted.

A subset of simulations was also repeated with the measured process parameters, delivering breakdown voltages lower than those found in the design phase (between 50 and 100 V less) but no changes were observed in the trends related to GAP distances, field-plate lengths and floating rings. A few I-V curves measured on active-edge diodes from the second part of the batch (featuring better trenches) are reported in Fig.6.11(a). As can be observed, the value of the reverse currents span between 5 and 15 nA and the breakdown voltages are distributed on a range of voltages from 100 to roughly 300 V, increasing with larger GAP sizes. The effects of the field-plate are observable in Fig.6.11(b) where the breakdown voltage distribution is plotted as a function of the GAP size for two diodes without (red squares) and with a 5 μ m field-plate (blue circles). As previously

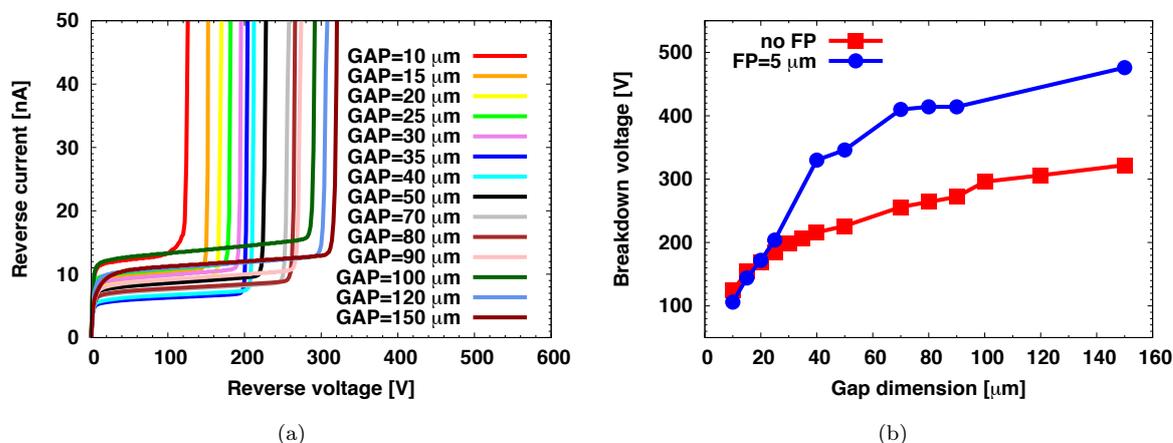


Figure 6.11: Measured leakage currents for diodes with different GAPs (a) and comparison of the measured breakdown voltages as a function of the GAP distance between an active-edge diode without field-plate (red squares) and one with a 5 μm field-plate (blue dots) (b) [143].

predicted by numerical simulations, the field plate has no effects at all for GAP distances lower than 20 μm , its effects start to be noticeable for larger GAPs, leading to an increase in breakdown voltage of roughly 100 V (maximum operating voltages of 500 V for GAPs in the order of 150 μm). It is important to notice that, for the intended GAP of roughly 30 to 40 μm for which these devices are intended, the field-plate can deliver operating voltages higher than 300 V to be compared with full depletion voltages of 5 V.

6.2.5 Functional characterization

The functional characterization of fabricated devices was performed by means of laser and X-Ray beam scans [143, 156]. The used laser scan setup is the one previously described in Chapter 4 subsection 4.6.1, while the X-Ray beam tests were performed at the B16 beam line at Diamond light source, Didcot, UK [157]. The X-ray photon energy was 15 keV and the measured beam size was 3 μm FWHM. The devices were biased using a NIM module and the variation in the current for each point of the scan was amplified and registered with a Keithley 428 current amplifier. The positioning was realized with a sub-micron platform.

The results of the laser scans performed on two different active-edge diodes are reported in Fig.6.12 and Fig.6.13 and are compared with the layout of the scanned area. The two measured devices are respectively:

- A device with GAP size of 40 μm and a field-plate of 3 μm biased at 20 V (Fig.6.12).
- A device with GAP size of 50 μm and one floating ring biased at 40 V (Fig.6.13).

In both scans the main electrode (DIODE) is visible as a low efficiency region, due

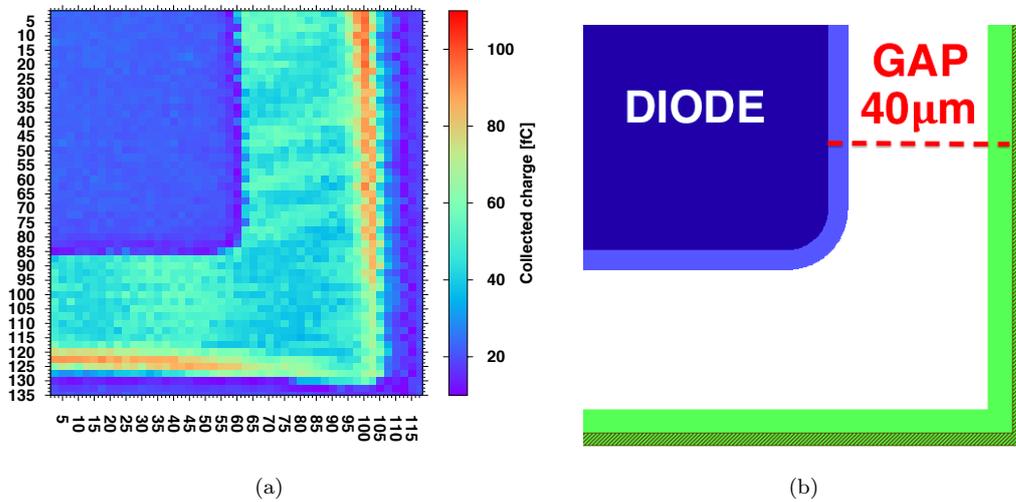


Figure 6.12: Laser scan of the corner region of a planar diode with active-edge and a 3 μm field-plate for a bias voltage of 20 V. The GAP distance is 40 μm. The scan is performed with a 1060 nm wavelength and with a scan step of 5 μm [143].

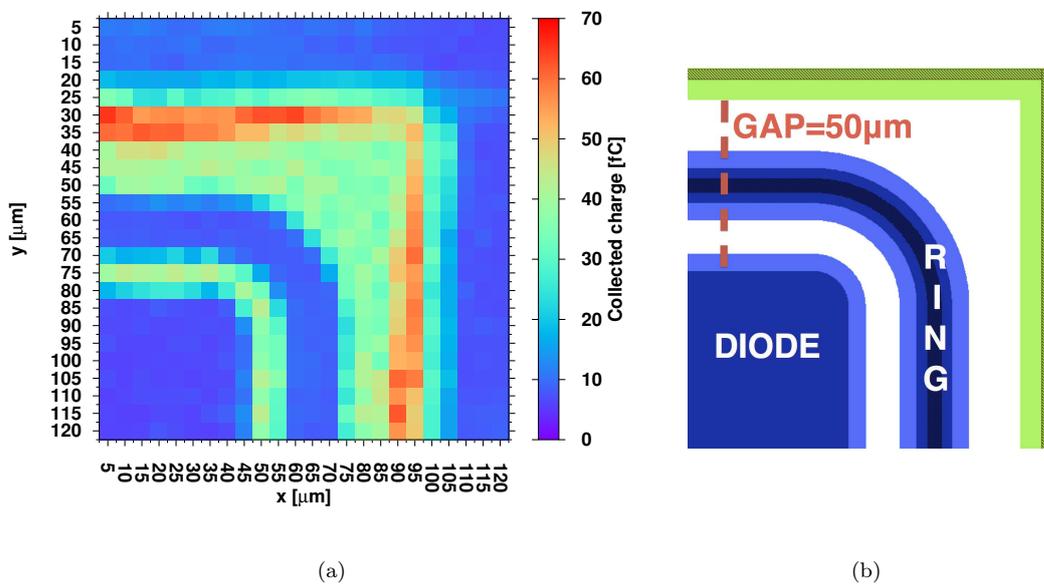


Figure 6.13: Laser scan of the corner region of a planar diode with active-edge and a floating-ring for a bias voltage of 40 V. The GAP distance is 50 μm. The scan was performed with a 1060 nm wavelength and with a scan step of 10 μm [156].

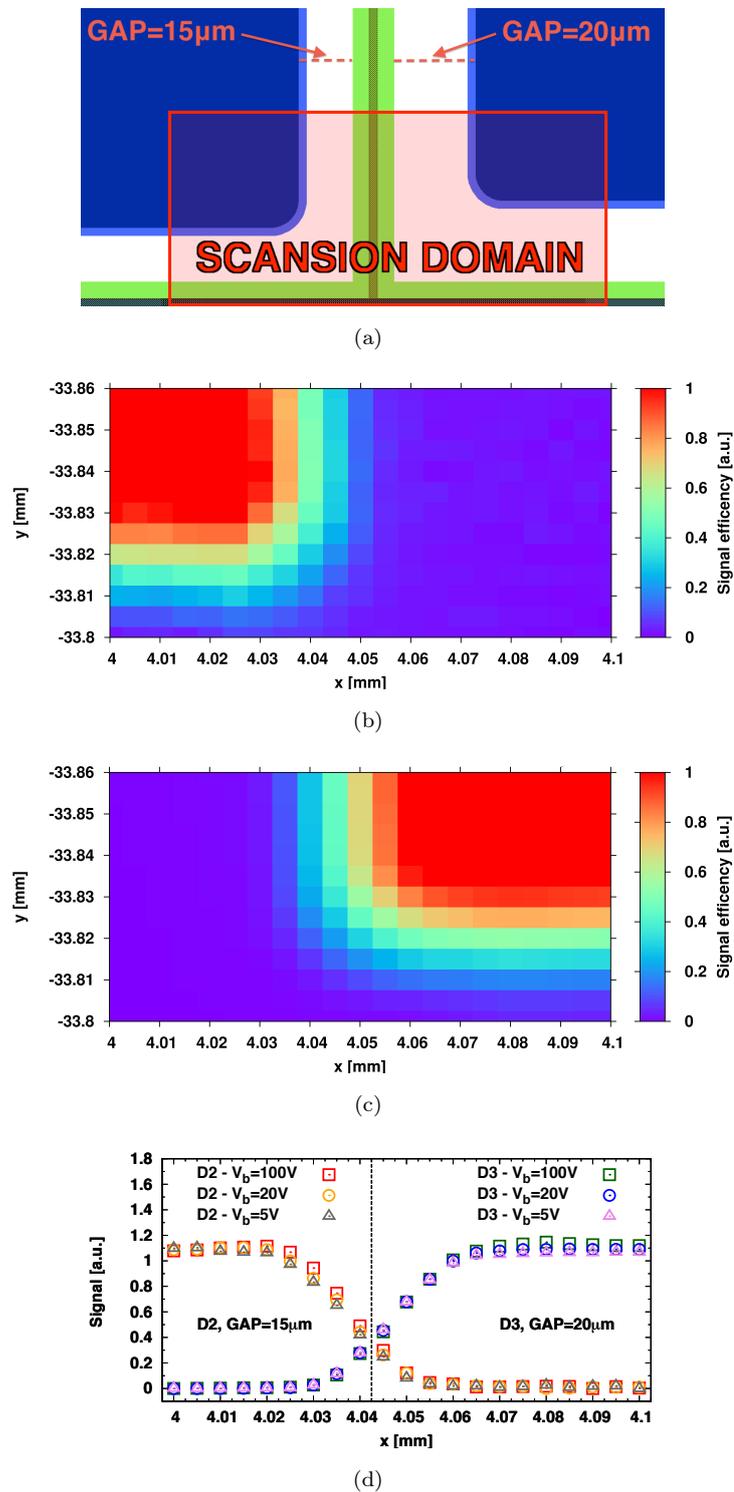


Figure 6.14: X-Ray beam scan of two adjacent diodes with active-edge for different bias voltages. The two diodes have GAPS of 15 and 20 μm respectively. The scanned region is reported in (a), the 2D signal efficiency maps are shown in (b) and (c) and the relative 1D signal efficiency profiles are reported in (d) [156].

to the fact that the metal is reflecting the laser light. The signal uniformity over the entire GAP region is very good although some higher efficiency regions are detected at the trench edge. This is believed to be caused by a thinner stack of surface layers that assure better light transmission to the silicon underneath, causing the total generated charge to be higher. In the specific case of Fig.6.13(a) the metal on top of the floating ring is visible as well.

In the case of the X-Ray beam scan reported in Fig.6.14, two adjacent diodes sharing the same trench were connected to two separate readout channels and a 2D scan was simultaneously performed on both of them with a step of 5 μm . In order to study the effects of the bias voltage on the collected charge, 5, 20 and 100 V biases were used. The layout of the scanned area is reported in Fig.6.14(a), the designed gap distances were 15 and 20 μm for the left and right diode respectively. The obtained 2D scans are reported in Fig.6.14(b) and 6.14(c) and a 1D scan extracted for a fixed y coordinate is reported in Fig.6.14(d). The active region of the device shows a very uniform charge collection with little or none influence by higher biases. These tests confirmed that full collection efficiency can be obtained in less than 20 μm from the physical edge.

These tests were very encouraging but need to be confirmed after irradiation. A neutron irradiation run is planned during the first months of 2013 at the Jozef Stefan Institute, Ljubljana, Slovenia.

Building on the knowledge gained with this first experimental batch of planar sensors with active-edge, another run was completed in October 2012. The new devices were this time realized on p-type substrates and with a layout compatible with the FE-I4 readout chip, in view of a possible use of these devices in the future ATLAS upgrades [158].

6.3 Slim 3D detectors with built-in charge multiplication

In the past decade, several R&D activities have explored new approaches to radiation tolerant particle sensors in view of the High Luminosity (HL) LHC upgrades, where the innermost layers of pixel detectors will have to withstand radiation fluences in excess of 10^{16} 1-MeV equivalent neutrons ($n_{eq} \text{ cm}^{-2}$) [159]. New materials, fabrication processes, device concepts and operating conditions have been extensively investigated with encouraging results [56, 98, 160, 161, 162].

Among the recent findings is charge multiplication in heavily irradiated silicon sensors, resulting in signal amplitudes that are considerably larger than those expected from the extrapolation of the trapping time constants extracted at lower fluences [163], and that can even exceed the pre-irradiation values. Charge multiplication has been independently observed by several research groups in planar pad and strip detectors after exposure to

large radiation fluences [163, 164, 165, 166, 167, 168, 169]. Very high bias voltages, in the order of 1000 V, have normally to be applied in order to reach the critical electric field values causing the onset of avalanche effects. In parallel with measurements of collected charge with LHC-like read-out chips, further studies (e.g., by edge Transient Current Technique [169]) aim at a deep understanding of charge multiplication phenomenon and at its modeling [170, 171]. Moreover, modified sensor designs easing the electric field control are being investigated in order for charge multiplication to be reliably exploited in future experiments [172].

Charge multiplication has also been shown to take place in double-sided 3D sensors [84, 92, 108, 109, 135, 173], in the bias voltage range from 200 to 350 V. In heavily irradiated 3D sensors ($\sim 10^{16} \text{ n}_{eq} \text{ cm}^{-2}$) the relatively small inter-electrode spacing, in the order of 50 μm , could indeed justify the onset of avalanche multiplication effects at much lower voltages than those necessary for planar sensors. Nevertheless, the observation of charge multiplication in samples irradiated at lower fluences ($\sim 10^{15} \text{ n}_{eq} \text{ cm}^{-2}$) [84, 108, 109, 173] and even in non irradiated samples [109], suggests that other mechanisms might play a major role. In particular, it should be stressed that charge multiplication was reported only for 3D sensors having non-passing-through columns, where high electric field peaks can develop at column tips, as confirmed by TCAD simulations [92, 135]. On one hand this results in a non uniform charge multiplication process, making the exploitation of this phenomenon in existing 3D sensors not straightforward. On the other hand it should be stressed that with 3D sensors of standard thickness (in the range from 200 to 300 μm) the signal amplitudes that can be obtained at relatively low voltages makes charge multiplication not essential to achieve a good tracking performance. Nevertheless, different considerations would apply in case the sensor substrate were thinner, as required for future applications of pixel sensors in vertex tracking in order to minimize the amount of multiple scattering experienced by charged particles, thus improving the momentum resolution [174]. The use of thinner substrates strongly reduces the active volume of the sensor causing, for charged particles, a much smaller signal with respect to that of thicker sensors. To achieve good signal-to-noise ratio this reduction needs to be compensated introducing a process of charge multiplication. Of course, in order to control charge multiplication both before and after irradiation, modified 3D cell topologies are necessary.

The work here described proposes a novel 3D sensor designs on thin silicon substrates allowing a moderate charge multiplication gain (lower than 10) to be obtained at reasonably low voltages (in the order of 100V) [175]. The study is based on TCAD simulations calibrated against experimental data. Analytical models are also used to provide useful predictions of gain as a function of the position within a cell and of the associated avalanche noise factor.

6.3.1 Design and technological aspects

In order for the electric field along the junction columns of a 3D sensor to be high enough for the onset of charge multiplication, two solutions can be envisioned. The first approach consists in enriching the doping of the substrate close to the junction columns, so as to reproduce the structure of a typical avalanche photodiode [176]. Although viable in principle, as confirmed by process simulations, this approach is very complicated to be pursued in practice since the doping of vertical electrodes and around them can only be performed by thermal diffusion, and proper control of doping profiles for two overlapping diffusions of opposite doping type might be very difficult to be achieved.

The second approach, here considered, is a geometrical one, i.e., it consists in reducing the inter-electrode spacing down to small values, in the order of $15\ \mu\text{m}$, that are suitable to obtain high electric field peaks at bias voltages of about 100 V, as will be shown in the following. A small pitch between electrodes brings along both advantages and disadvantages that should be carefully considered. Very high charge collection efficiency can be expected even in heavily irradiated sensors, because charge trapping effects are strongly attenuated if the inter-electrode distance is shorter than the maximum drift length of charge carriers. However, this would also result in a larger capacitance, hence a higher noise [73]. In addition, a high density of vertical electrodes would spoil the hit reconstruction efficiency in case the electrode themselves are not sensitive enough [113]. Nevertheless, it should be stressed that the disadvantages of a short inter-electrode distance would be mitigated in case of thin sensor substrates, which would also ease the fabrication process in some respects. Thinner substrates would in fact result in a lower electrode capacitance, since the latter scales with the electrode depth to a large extent. Moreover, the electrode diameter could be reduced, since the aspect ratio (depth-to-diameter) attainable with Deep Reactive Ion Etching (DRIE) can be assumed to be almost constant [177]. A narrower electrode diameter provides several advantages: i) a further reduction of the capacitance; ii) an increase of the electric field peaks at the electrodes, that is useful for charge multiplication; iii) a better sensitivity of the electrodes themselves; iv) a simpler fabrication process (in particular in the poly-Si filling and doping of the electrodes), because of the smaller thickness of poly-Si to be deposited and finally etched from the wafer surface [68].

Keeping into account the previous aspects, as will be explained in the following, we have conceived some possible 3D cell topologies, that are summarized in Fig.6.15: all of them feature a short inter-electrode distance, with a junction column (n^+) at the centre of a cell, but they differ in the ohmic (p^+) electrode configuration. Cells in Fig.6.15(a), Fig.6.15(b), and Fig.6.15(c) are based on columnar electrodes only, whereas cells in Fig.6.15(d), Fig.6.15(e), and Fig.6.15(f) are based on a junction columnar electrode and an ohmic trench electrode. Note that n^+ doping is chosen for read-out electrodes to

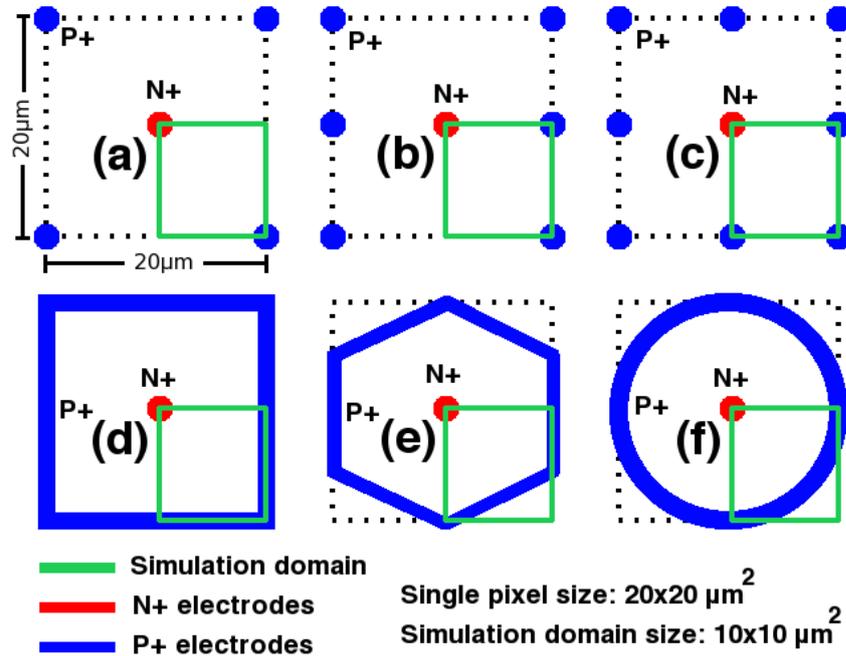


Figure 6.15: Basic cells of the proposed 3D sensors with charge multiplication by design. The corresponding simulation domains are also shown.

exploit the higher mobility and higher impact ionization coefficients of electrons compared to holes [176]. A value of $4 \mu\text{m}$ is considered for the electrode width, that is feasible for sensor thicknesses lower than $75 \mu\text{m}$: in fact, these structures were scaled by a factor of ~ 3 with respect to existing 3D sensors fabricated for the IBL, which are $230 \mu\text{m}$ thick with a $12 \mu\text{m}$ electrode diameter, i.e., with an aspect ratio of about 20:1 [124].

All these cell topologies will be shown to allow for charge multiplication, with slightly different characteristics. However, the choice of a specific structure, besides considering the expected performance, should also account for the additional constraints set by the realization of a full sensor assembly, that are briefly discussed in the following:

- sensor fabrication: 3D cells using only columnar electrodes could be fabricated either with a single-side process with support wafer, originally developed at the Stanford Nanofabrication Facility - SNF (Stanford, USA, [68]), and now available also at SINTEF (Oslo, Norway, [76]), or with a double-side process, independently developed by CNM (Barcelona, Spain [86]) and FBK (Trento, Italy [85, 129]) in slightly different versions, and already tested at CNM on very thin sensors [178]. On the contrary, 3D cells using trenches require a single-side process with support wafer [68, 76, 71], that also allows for a better mechanical robustness and for active edges.
- surface isolation between pixels: as in currently existing 3D sensors, n^+ electrodes

should be isolated at the surface. To this purpose, p-spray or p-stop implantations are normally used. In case of small cell sizes, here considered, p-stops could be difficult to accommodate, so p-spray should be preferred. The related concern, especially before irradiation, is that p-spray would cause premature surface breakdown at voltages lower than those required for charge multiplication. In this respect, it should be noted that trench p^+ electrodes would intrinsically provide isolation between n^+ electrodes, without need of p-spray, but an early breakdown risk at the surface would still be present, especially after irradiation, due to the high electric field at the corner between the p^+ trench and the electron accumulation layer induced by the positive oxide charge.

- sensor layout: although narrow electrodes are expected to yield a much better response than large ones, a high density of electrodes is certainly not beneficial. Having defined the geometrical efficiency as the ratio between the area not covered by electrodes and the total area, better values are obtained for structures based on columnar electrodes only. As an example, the geometrical efficiency is $\sim 87\%$ for the cell of Fig.6.15(c) and $\sim 67\%$ for the cell of Fig.6.15(d). Additionally, cells using trenches could result in less regular pixel shapes, or even incomplete area coverage. Note that the cylindrical cell of Fig.6.15(f), although not practical, will be included in the following analysis as a reference, since it is the only one providing a true radial symmetry, thus allowing a direct comparison with a 1D analytical model.
- interconnection to a read-out chip: a cell size of $20 \times 20 \mu\text{m}^2$, common to all structures, is pretty small, but it would be suitable for interconnection to a read-out chip in case very high spatial resolution were required [174]. To this purpose, micro-bump or micro-TSV techniques could be adopted, allowing for pitches lower than $5 \mu\text{m}$ [179]. As an alternative, these cells could be joined together by means of metal interconnections in order to obtain larger pixels.

6.3.2 TCAD simulation approach

The numerical simulations here reported were performed using the Synopsys TCAD package [90], which has already been proved to be a reliable tool for the analysis and the design of 3D sensors. In particular, it was already demonstrated in this work that numerical simulations, accounting for geometrical and technological details, can predict both the static and the charge collection properties of 3D sensors, both before and after irradiation [85, 92, 102, 125, 129, 130, 135, 142]. The general strategy for the simulation of 3D sensors is reviewed in [92]. For the sake of clarity, here we remind just a few details. A Minimum Ionizing Particle (MIP) is simulated using the Heavy Ion model, which requires, among other parameters, the amount of charge to be released per unit length (80 electron-hole

pairs per micrometer) and the lateral distribution of the charge cloud about the particle track (Gaussian with a $1 \mu\text{m}$ radius). Surface radiation damage is modeled by increasing the density of oxide fixed charge and of interface states. Bulk radiation damage is modeled using the 3-level "Perugia" trap model [91], modified as described in [136]. The latter model, along with the avalanche generation model, has already been demonstrated to accurately reproduce charge multiplication phenomena in irradiated 3D sensors [92, 135]. Similarly, simulation results relevant to avalanche breakdown mechanisms occurring at the surface of non irradiated 3D sensors have been found to be in very good agreement with experimental data [130, 142].

Different sets of simulations have been carried out: initially, the simulation parameters have been calibrated to accurately describe the electrode response, and the most critical design/technological issue, i.e., premature surface breakdown, has been addressed. Then, the charge multiplication properties of different 3D cells have been thoroughly investigated and compared by using a simplified simulation domain describing the core of the devices. Finally, results for the most promising device layout have been checked also using a full three-dimensional structure.

Electrode response calibration

It is known that electrodes filled with poly-Si are not really dead regions, but exhibit a reduced efficiency compared to the sensor bulk, due to the relatively low carrier lifetime caused by small poly-Si grain sizes. Measurements performed on 3D sensors from SNF have shown electrode efficiencies in the order of 30-40% [183, 184]. Achieving a fully efficient electrode would be quite difficult because carriers can only move by diffusion inside it due to the lack of any electric field. In addition, due to the high electrode doping concentration, the recombination probability is very high. In order to accurately model the behavior of the electrodes, we have performed a calibration of the lifetime values by comparing simulated results with experimental data. Two 2D structures reproducing the vertical plane along the diagonal connecting three columnar electrodes were defined (1 n-type and 2 p-type, and vice-versa), and a MIP was scanned from left to right impinging also inside the poly-Si filled columnar electrode. The structure geometry was representative of a SNF 3D sensor (e.g., the column radius was $7 \mu\text{m}$) and the carrier lifetimes in poly-Si were parameterized in order to find the value delivering a $\sim 30\%$ efficiency at the centre of the electrodes. Although this 2D approach is quite simplified, satisfactory results were obtained: the efficiency profiles as a function of the particle hit position for n^+ and p^+ electrodes are reported in 6.16(a) and 6.16(b), respectively. As can be seen, a lifetime of $1 \mu\text{s}$ is adequate to reproduce the experimentally observed efficiencies for both electrode types [183, 184].

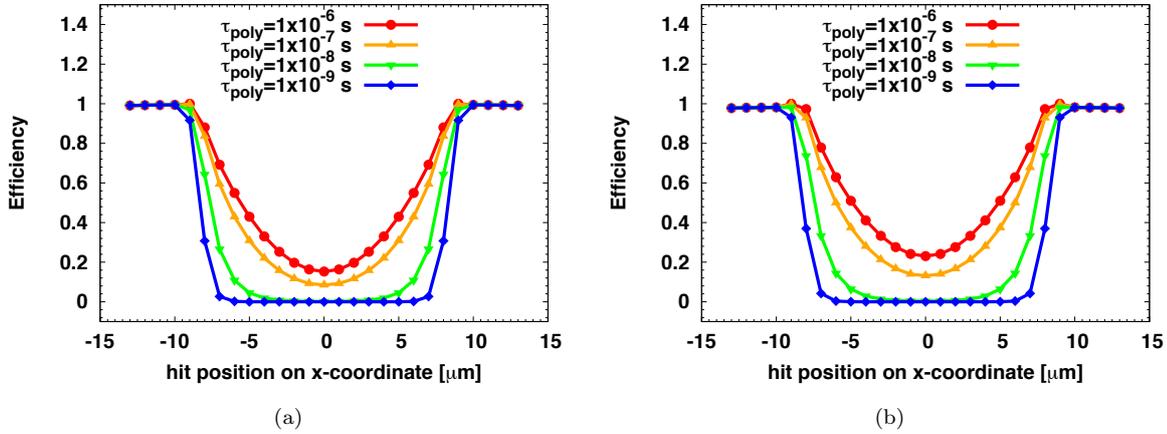


Figure 6.16: Simulated efficiency of the electrodes for a standard 3D detectors with poly-Si filled electrodes and for variable poly-Si carrier lifetimes. Results for both n^+ (a) and p^+ (b) electrodes are reported.

Better results are expected for the devices here discussed, that feature narrower electrodes than SNF ones. In order to prove this, the same 2D structures were re-simulated, keeping the lifetimes at $1 \mu\text{s}$, but shrinking the electrode radius to $2 \mu\text{m}$.

Results are reported in Fig.6.17 and show that the efficiencies are $\sim 80\%$ for n^+ electrodes and $\sim 90\%$ for p^+ electrodes. Further improvements in the electrode response might be achieved by using oxygen-free gases, such as PH_3 for phosphorus and B_2H_6 for boron, for the electrode doping in order to avoid the barrier effect due to the oxide layer that would otherwise be formed at the electrode surface [180].

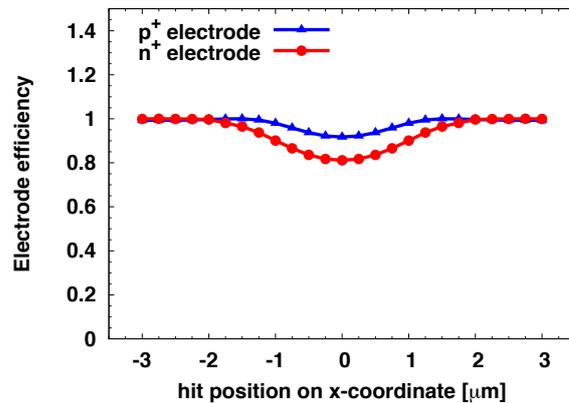


Figure 6.17: Simulated efficiency of the electrodes for a 3D detector with electrodes filled with poly-Si and having radius of $2 \mu\text{m}$. The considered poly-Si lifetimes are equal to $1 \mu\text{s}$.

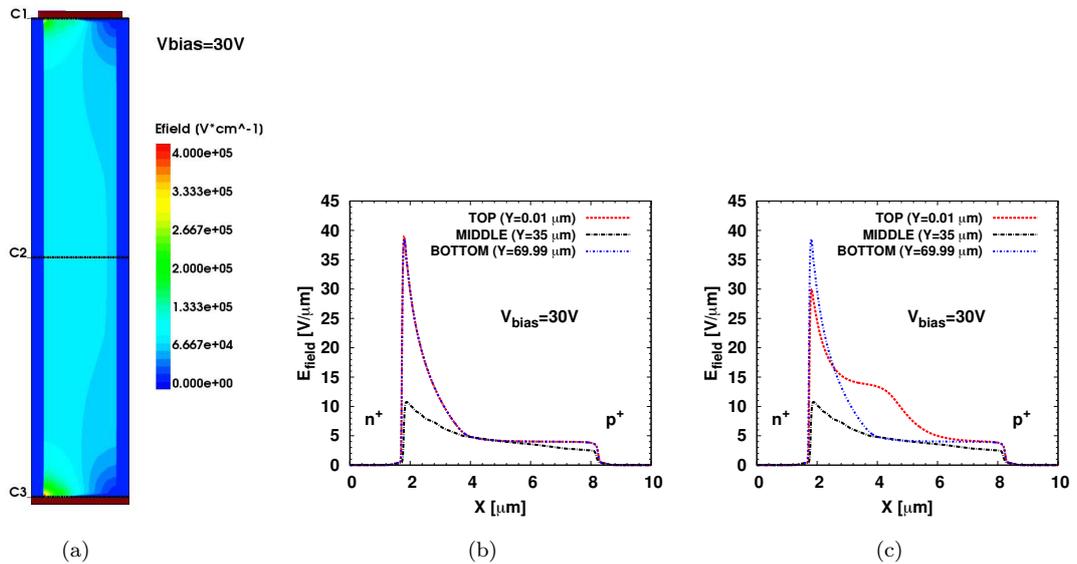


Figure 6.18: 2D Electric field distribution for the structure with field-plate (a) and comparison between the 1D electric field profiles extracted at 3 different depths of the device without (b) and with (c) field-plate.

Surface isolation

A crucial aspect of any silicon sensor, is the design of the surface isolation layers, i.e., p-spray or p-stop implantations. For the structures considered in this study, and with the intent of achieving electric fields high enough to produce charge multiplication along the electrodes, it is crucial to prevent from premature breakdown at both the upper and lower surfaces. In order to investigate these aspects, 2D simulations were performed with reference to a vertical plane along the diagonal connecting two columnar electrodes of opposite doping types, having both surfaces covered with silicon dioxide with a fixed charge concentration of $1 \times 10^{11} \text{ cm}^{-2}$, typical of pre-irradiation conditions.

Both p-spray and p-stop isolations were considered. P-stop isolation was soon discarded because, due to the geometrical constraints caused by the small cell size, it resulted in low breakdown voltages ($\sim 50\text{V}$, i.e., not sufficient to reach the multiplication regime along the vertical electrodes). The p-spray case was analyzed in greater detail, starting from a standard solution and then implementing some improvements which finally led to a suitable structure. Fig.6.18 shows the results for a structure with p-spray on both wafer surfaces (implanted dose $2 \times 10^{12} \text{ cm}^{-2}$). The maximum operating voltage was in this case only 30V. Very large electric field peaks are in fact present at both sensor surfaces at the n^+ /p-spray junctions, as shown in Fig.6.18(a). The 1D electric field profiles extracted at 3 different depths inside the device (top, middle and bottom) are reported in Fig.6.18(b). It can be seen that the peaks on both the upper and lower surface have the

same magnitude and, at the same time, the field in the middle of the structure is not high enough to cause charge multiplication. As already observed in our previous studies on 3D sensors [130, 142], the addition of a field-plate to the junction electrode can moderately increase its voltage handling capabilities. This was tested on the same structure but, since a back-side metal patterning would be very complicated for the proposed devices (or actually impossible in case of a single-side 3D technology), the field-plate could only be applied on the front side, so that the high electric field peak on the back side remained unaltered, see Fig.6.18(c).

A possible solution to the breakdown problem on the back side would be to make the n^+ column non passing through, leaving a uniform p^+ implantation on the back side, as successfully tested on the latest batch of 3D sensors at FBK [142]. However, this modification alone is not sufficient, due to the high electric field developing at the column tip, caused by its narrow diameter. Nevertheless, the DRIE process has some flexibility and, choosing an isotropic etching as a last step, it is possible to change the shape of the column tip, and particularly, to increase its radius [181]. The combination of the field-plate on the front side and of the modified column tip geometry is able to increase the breakdown voltage of the sensors to values large enough to allow for avalanche multiplication along the electrodes. The bi-dimensional distribution of the electric field obtained at the breakdown voltage is reported in Fig.6.19, together with the 1D profiles extracted from the most critical regions. As can be observed, the electric field peaks on the front side, on the column tip, and along the column are similar, allowing to reach fields high enough for charge multiplication for the whole electrode depth. This approach has indeed additional benefits on the detection efficiency: being the junction column non passing through, it is possible for impinging particles to generate charge in the silicon bulk underneath it and, since the field around the column tip is very large, charge multiplication can be exploited also in this region.

Simplified structure for charge multiplication simulations

The results described in the previous section proved that it is possible to limit the detrimental effects of the sensor surface and column tips on the breakdown voltage, so the charge multiplication can be studied on a simplified structure, representing the central region of the device. The considered structure is reported in Fig.6.20 for the case featuring four columnar electrodes of Fig.6.15(c). Due to symmetry considerations it is possible to limit the simulation domain to a quarter of the elementary cell (see also Fig.6.15, for all simulated layouts). The structure thickness can be limited to $1\ \mu\text{m}$ because the vertical field in the central part of the device is uniform. The substrate doping concentration is chosen to be $1 \times 10^{13}\ \text{cm}^{-3}$, corresponding to a resistivity of $\sim 1\text{k}\Omega\ \text{cm}$, in order to lower

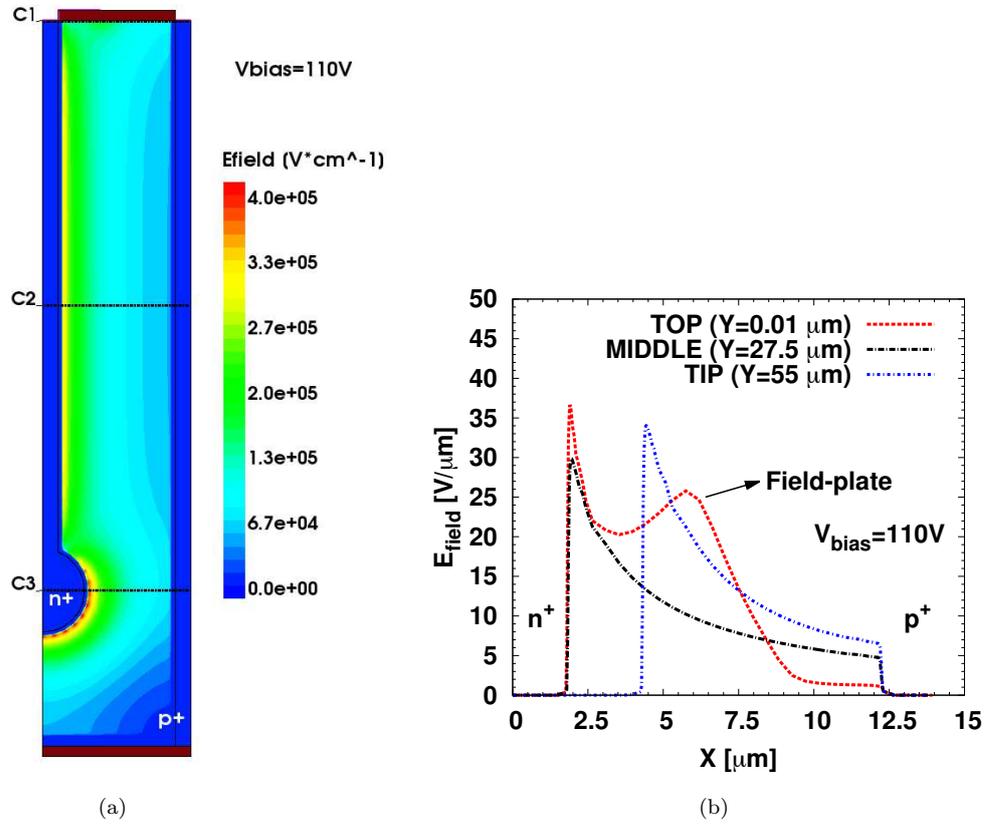


Figure 6.19: Bi-dimensional electric field distribution inside the structure with the modified tip geometry and the field-plate (a) and relative 1D profiles at different depths extracted from the simulated data (b).

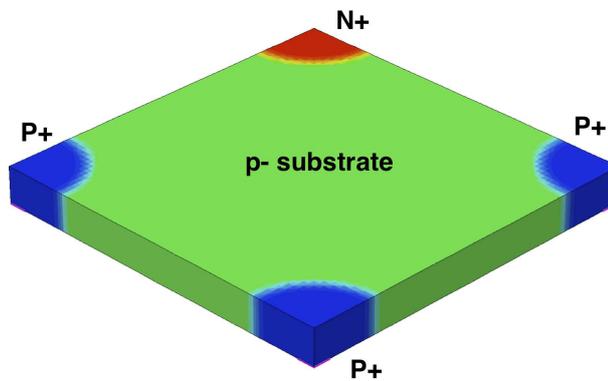


Figure 6.20: Simplified simulation domain for the 1N-3P structure.

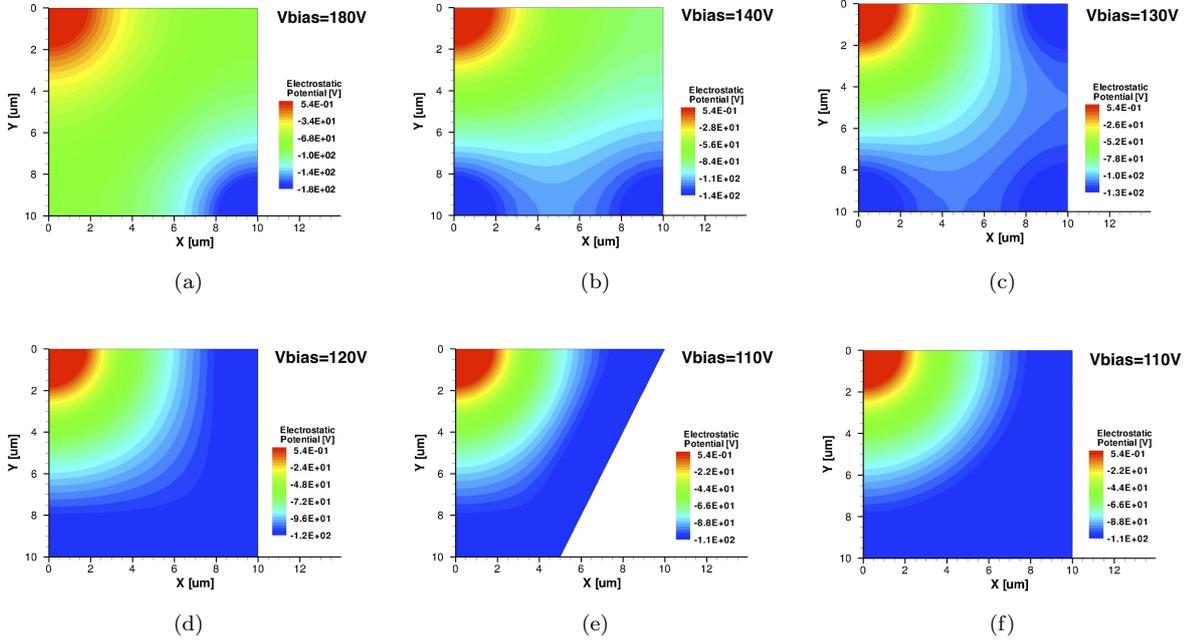


Figure 6.21: Electrostatic potential distribution close to breakdown for all the considered structures.

the voltage required for the onset of avalanche multiplication.

6.3.3 Charge multiplication results

Numerical simulations were performed on both un-irradiated and irradiated devices. A comprehensive description of the results is performed in the following paragraphs.

Un-irradiated devices

All the structures shown in Fig.6.15 were simulated in pre-irradiation conditions. The electrostatic characteristics of the devices were extracted from quasi-stationary simulations. Electrostatic potentials and electric fields for each of the considered structures are reported in Fig.6.21 and Fig.6.22, respectively. Data refer to bias conditions close to the breakdown voltage. Compared to the cylindrical structure of Fig.6.21(f) and Fig.6.22(f), used as a reference, the 2D distribution of the considered quantities is relatively uniform for the other structures featuring trench electrodes, whereas larger differences can be observed for structures featuring only columnar electrodes. In all cases the highest field peak is at the junction column and its magnitude is large enough to achieve multiplication at reasonably small bias voltages. From Fig.6.22(a) it can be noticed that a very high field is present also at the ohmic column only in the structure with one n^+ column and one p^+ column. This will be shown to affect the multiplication process.

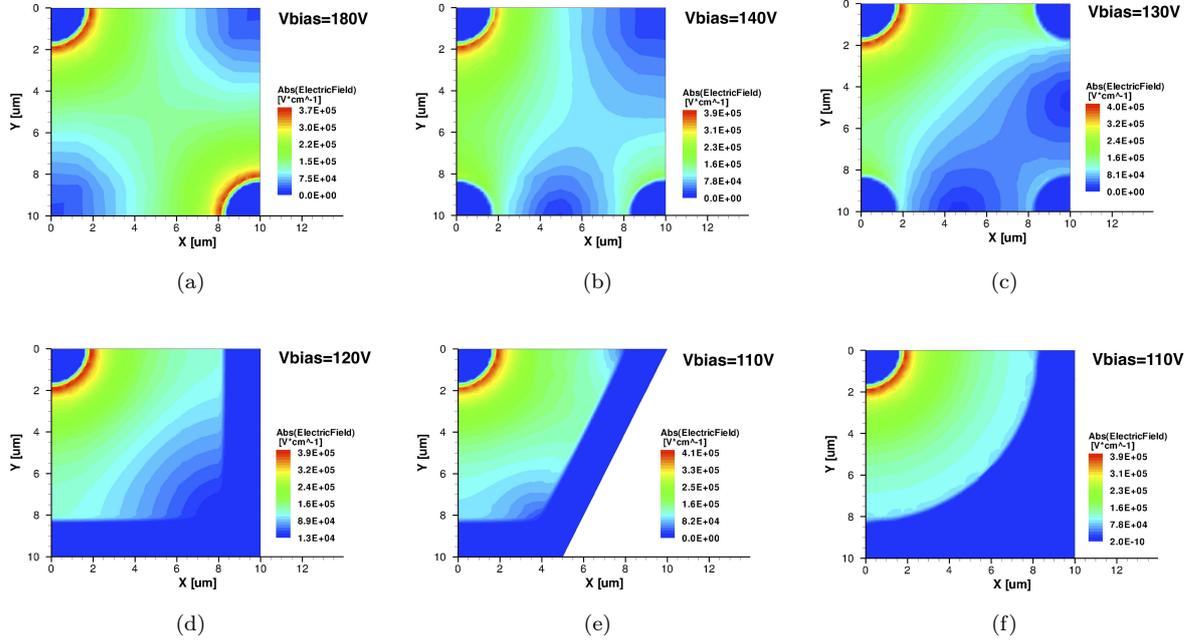


Figure 6.22: Electric field distribution close to breakdown for all the considered structures.

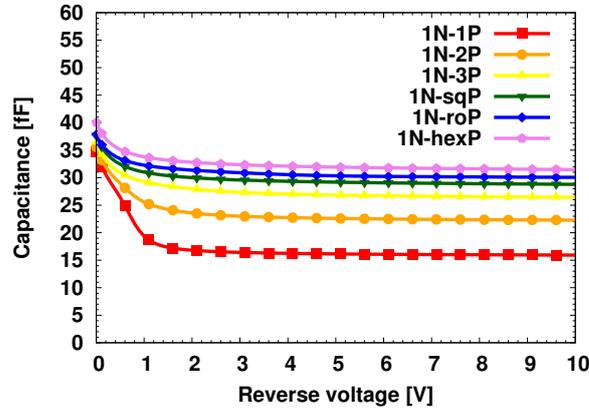
The structure identifiers and the breakdown voltages (defined as the voltage for which the ionization integral reaches 1) for all the considered structures are reported in Tab.6.2. Structure IDs are labelled according to the electrode configurations: all structures have one n^+ column (1N), whereas the p^+ electrodes can be columns (1P, 2P, 3P) or trenches (SqP, HexP, RoP). Breakdown occurs in the range between ~ 170 V for the 1N-1P structure and about ~ 110 V for the structures with trench ohmic electrodes.

In addition to current simulations, capacitance simulations were also performed in order to obtain an estimation of the effects of a reduced pixel size on the device capacitance. The results are reported in Fig.6.23, where the capacitance is shown to range between 15 and 35 fF (note that the surface contribution to the capacitance, not included in the simulation, is estimated to be negligible, ~ 1 fF, since the electrode perimeter is very small). These results, if compared to the ~ 100 fF/column estimated for the current FE-I4 3D pixels, show that the small inter-electrode distance is compensated by the reduction in sensor thickness and column diameter, so that the capacitance should affect the noise only to a minor extent. A summary of the capacitance values is also reported in Tab.6.2.

The avalanche gain for each considered bias was extracted from transient simulations in the following way: the leakage current was subtracted from the simulated output pulses and a numerical integration was later performed to obtain the total amount of collected charge. The gain was calculated by dividing the simulated collected charge by the known

Table 6.2: Structure identifiers and relative simulated breakdown voltages (V_{BD}), bias voltage required to reach a gain of 4 ($V_{bias}(G=4)$), and capacitances at 10V bias voltage ($C(@10\text{ V})$).

Structure ID	Ohmic electrode (p^+)	V_{bd} [V]	$V_{bias}(G=4)$ [V]	$C(@10\text{ V})$ [fF]
-	-			
1N-1P	1 Column	178	172	15.93
1N-2P	2 Columns	143	134	22.28
1N-3P	3 Columns	130	112	26.43
1N-SqP	Square trench	118	102	28.79
1N-HexP	Hexagonal trench	112	93	31.47
1N-RoP	Round trench	108	98	28.79

Figure 6.23: Simulated capacitance vs reverse voltage curves for all the considered structures. Values are scaled to a pixel size of $20 \times 20 \times 70 \mu\text{m}^3$.

charge released by the impinging MIP (80 electrons per micron). The obtained gain-voltage curves for each investigated structure for a particle hitting at the centre of the cell are reported in Fig.6.24. For low biases the gain is equal to 1, as expected due to the low electric field. By increasing the applied voltage, the gain starts increasing for all the structures, with the onset of avalanche multiplication ranging between about 60-80 V for the structures featuring trench electrodes and ~ 130 V for the 1N-1P structure. Gain magnitudes of up to 7 can be achieved at relatively low operating voltages, in agreement with the expectations. Simulations were repeated for several different particle hit positions in order to study the uniformity of the multiplication effects. As an example, Fig.6.25 shows the gain-voltage curves in a 1N-SqP structure for four different hit positions, also shown in the inset. The gain is largely independent on the particle hit position a part for those regions very close to the junction column, where it is smaller, in good agreement with the theoretical model [182], as will be discussed later.

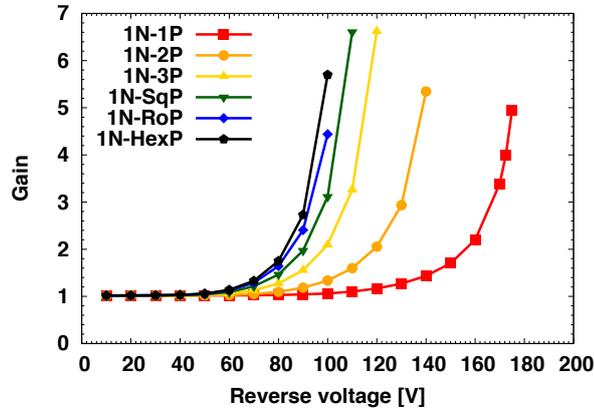


Figure 6.24: Simulated avalanche gain vs reverse voltage in all the considered structures in pre-irradiation conditions for a particle hitting at the centre of the cell.

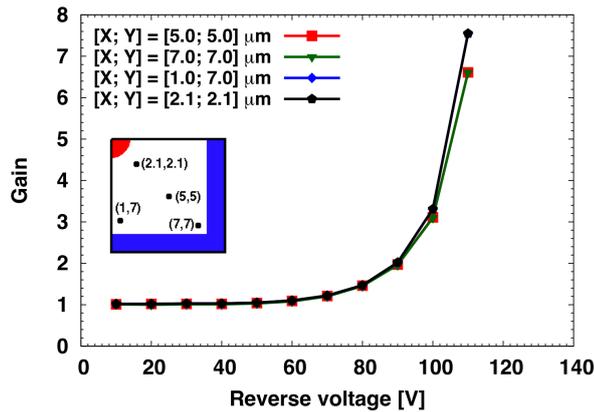


Figure 6.25: Simulated avalanche gain vs reverse voltage in a 1N-SqP structure in pre-irradiation conditions for different particle hit positions, shown in the inset.

Additional information about the dynamics of the devices can be extracted observing the shape of the output pulses. As an example, Fig.6.26(a) shows the output current pulses in response to a MIP hitting the centre of a 1N-SqP structure. The pulse rise times are in the order of 50 ps. The first signs of charge multiplication are visible at around 80 V; after that, the pulse amplitude starts increasing and the overall pulse duration increases, but the signal remains very fast for all voltages of practical interest. Similar behaviors are shown by all structures but the 1N-1P one (see Fig.6.26(b)), where a secondary peak is visible at about 150 ps. This is due to the fact that the electric field peak at the ohmic column is high enough to let also holes trigger avalanche multiplication (although with a lower efficiency with respect to electrons due to their lower ionizing coefficient [182]), so that a "ping pong" effect between charges multiplied at the two electrodes takes place. In

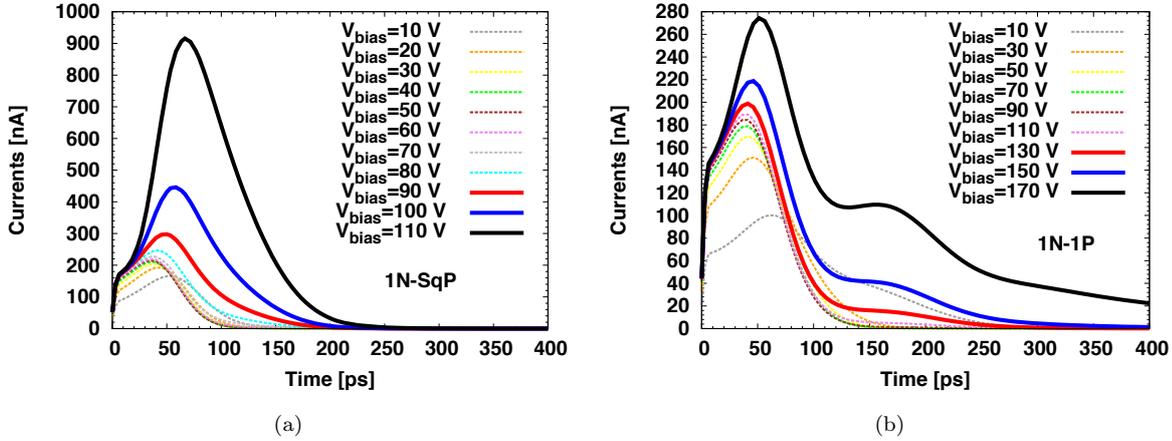


Figure 6.26: Simulated output current pulses in two of the considered structures at different bias voltages: 1N-SqP (a), and 1N-1P (b).

fact, the delay between the primary and secondary peaks in the current pulses is about 100 ps, i.e., the time needed by charge carriers to drift between the two electrodes. This effect is undesirable, since it causes a long tail in the signal shape and also worsens the excess noise factor, as will be shown in the next subsection.

Taking into account the simulation results in terms of gain-voltage curves, response speed, and area coverage, the 1N-SqP structure appears as the most promising one, so we will focus our analysis on it in the following.

Post-irradiation

The gain of all the structures was also simulated in post-irradiation conditions using the simplified structure in order to understand how the radiation damage would affect the sensor behavior. The trap concentrations of the 3-level bulk radiation damage model [91, 136] were gradually increased to account for different irradiation fluences up to $2 \times 10^{16} \text{ n}_{eq}/\text{cm}^2$.

Fig.6.27 shows the gain for the 1N-SqP structure as a function of the reverse voltage in different irradiation conditions. Data refer to a particle hit position at $X=7 \mu\text{m}$, $Y=7 \mu\text{m}$ (i.e., close to the ohmic trench corner, see also Fig.6.21(d) and Fig.6.22(d)) which was chosen as representative of a worst case condition. It is very important to notice how the onset of the multiplication effect is not affected by radiation at all, so that the proposed structures can be operated at the same voltage both before and after irradiation. The gain is lower than 1 at low voltage due to charge trapping effects, which are particularly important at the highest fluences, since the electric field is not very high in the considered particle hit position. However, the signal loss due to charge trapping can be recovered at

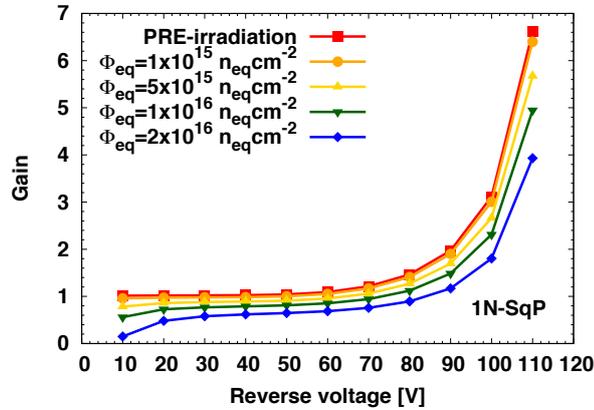


Figure 6.27: Simulated avalanche gain vs reverse voltage in a 1N-SqP structure at different irradiation fluences for a particle hit position at $X=7 \mu\text{m}$, $Y=7 \mu\text{m}$ (see also Fig.6.21(d) and Fig.6.22(d)).

larger voltages exploiting charge multiplication, so that the sensor is expected to be fully functional also after extreme irradiation fluences.

Simulation of a full 3D structure

The behavior of a non irradiated 1N-SqP structure was also investigated by using a full 3D simulation domain. This was particularly important to test if charge multiplication can be exploited also when the particle impinges inside the columns. Fig.6.28 shows the simulated gain vs reverse voltage for particles impinging in both electrode types and inside the silicon bulk. The poly-Si lifetimes were set to $1 \mu\text{s}$, as previously estimated. It can be observed that at low bias voltage results are in good agreement with those obtained

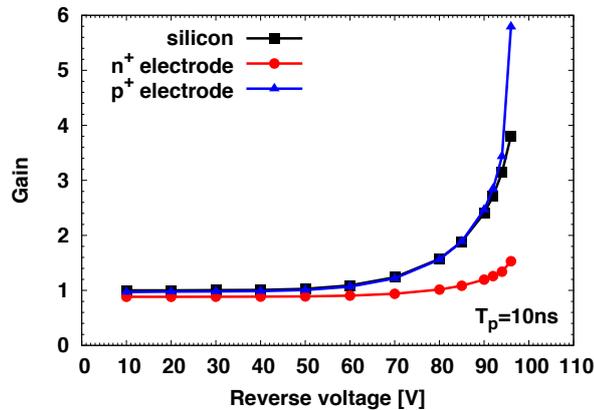


Figure 6.28: Simulated avalanche gain vs reverse voltage in a 1N-SqP full-3D structure in pre-irradiation conditions for three different particle hit positions: at the centre of the cell, and inside the n^+ and p^+ electrodes.

from the 2D simulation of Fig.6.17, i.e., the electrode efficiency is slightly lower for the n^+ electrode. At high voltage, the gain curve for the p^+ electrode is similar to that for the silicon bulk, because electrons are able to diffuse out in a few ns and later trigger the avalanche. On the contrary, a much lower gain is observed for the n^+ electrode, that is to be ascribed to charge multiplication at the column tip. In fact, holes that diffuse out of the n^+ electrode and drift to the p^+ electrode are not able to trigger an avalanche. Nevertheless, the weak gain obtained for the n^+ electrode is not a major concern, since for particles hitting in this region no charge sharing is expected to take place.

6.3.4 Noise considerations

The introduction of avalanche multiplication in the proposed detector inevitably leads to the presence of additional noise related to charge multiplication [185]. The increase in the charge signal enabled by avalanche multiplication is beneficial as long as the total output noise is dominated by electronic readout noise and the relative contribution of multiplication noise is comparatively small. It is therefore mandatory to perform an estimation of the avalanche noise, in order to evaluate the balance between benefits and drawbacks of the proposed 3D avalanche detectors.

Excess noise in avalanche photodiodes is described by a noise factor F , which quantifies the increase in the noise spectral density with respect to an ideal noiseless multiplication. The current noise spectral density S_I of an avalanche detector can be expressed as:

$$S_I = 2qI_{tot}M^2F \quad (6.1)$$

where I_{tot} is the total current flowing in the device and M is the average multiplication gain.

Starting from the first developments of avalanche photodiodes in the 1960s, several numerical models to estimate avalanche noise factor have been proposed. The first models were based on the assumption that avalanche is a local process and offers a good agreement with experimental data for avalanche diodes having a thick multiplication region [185, 186]. Later, more advanced models introduced the non-locality of avalanche multiplication [186, 187, 188], demonstrating that the local models yielded an over-estimation of noise factor in the presence of thin avalanche regions and high electric fields.

Although TCAD simulation tools include models for the simulation of avalanche multiplication effects, the modeling of avalanche noise is currently not implemented. However, if the central part of the columns is considered, the dimensionality of the problem can be reduced thanks to the radial symmetry of the simulation domain, enabling first-order avalanche noise estimation on a 1D simulation domain using the standard model proposed in [185]. The simplified 1D model can be preliminarily validated against TCAD simulations

by comparing the agreement with the predicted avalanche gain. The estimation obtained using this local model can be regarded as a worst-case, and can bring useful insight into the possibilities and limitations of avalanche multiplication in 3D detectors. In the future, the noise estimation accuracy could possibly be improved with the use of non-local avalanche models.

Noise factor calculation

The electric field map in the different structures analyzed in this work has been plotted in Fig.6.22. It can be observed that, except for device 1N-1P of Fig.6.22(a), the electric field peaks only in the region close to n^+ electrode. This region will therefore account for the observed avalanche multiplication. In addition, for almost all the structures, the electric field has a cylindrical symmetry in the proximity of the n^+ electrode. It is therefore reasonable to assume a simplified 1D model for a first estimation of avalanche multiplication and noise.

A 1D model for numerical evaluation of avalanche noise factor based on the cylindrical geometry was therefore developed. The avalanche gain obtained with the proposed model is first validated against TCAD simulation results with the cylindrical structure, and then used to calculate the avalanche noise factor.

In the model, the electric field was estimated analytically by considering a cylindrical electrode geometry. The equation for the electric field in a cylindrical capacitor is:

$$E(x) = \frac{V}{x \ln\left(\frac{r_d}{r_j}\right)} \quad (6.2)$$

where r_d is the depletion region radius, r_j is the junction radius and V is the applied voltage. The curve in Eq.6.2 is plotted in Fig.6.29 for $r_j=1.7 \mu\text{m}$, $r_d=8.2 \mu\text{m}$ and $V=110 \text{ V}$, and compared with the electric field of the cylindrical structure 1N-RoP. A good matching between analytical model and 3D TCAD simulation can be observed. Avalanche gain was evaluated numerically starting from the following expression [185]:

$$M(x) = \frac{\exp\left[-\int_x^w (\alpha_n - \alpha_p) dx'\right]}{1 - \int_0^w \alpha_n \exp\left[-\int_{x'}^w (\alpha_n - \alpha_p) dx''\right] dx'} \quad (6.3)$$

where the electron and hole ionization coefficients α_n and α_p were calculated numerically using Van Overstraeten and De Man models [182]. Multiplication gain as a function of the distance from the center of the N-type column is plotted in Fig.6.30 for three different bias voltages. It is worth noting that for $x \geq 4 \mu\text{m}$, corresponding to pure electron injection into the high field region, M is approximately constant. Since the cell geometry is cylindrical, this volume corresponds to more than 75% of the detector active volume.

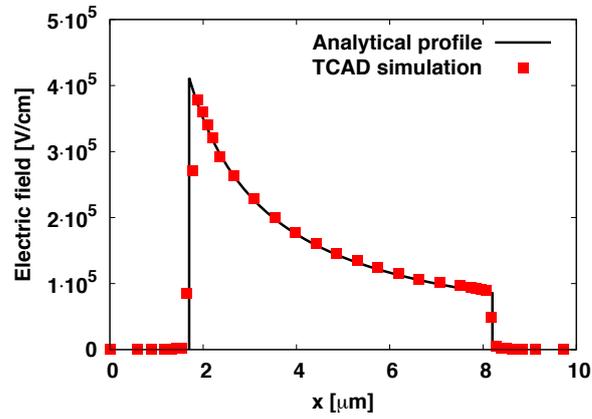


Figure 6.29: Electric field profile for TCAD simulation (cylindrical structure) and analytic solution.

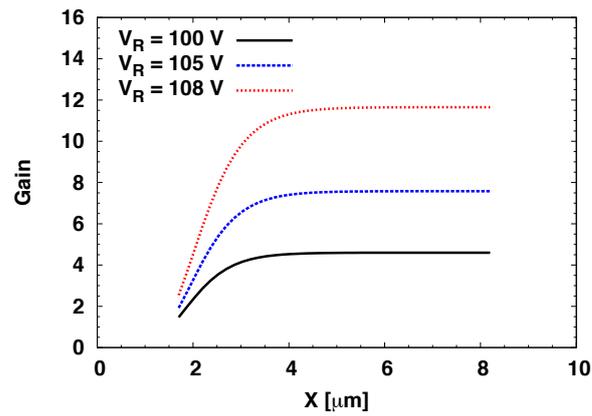


Figure 6.30: Position-dependent multiplication gain calculated with the 1D model.

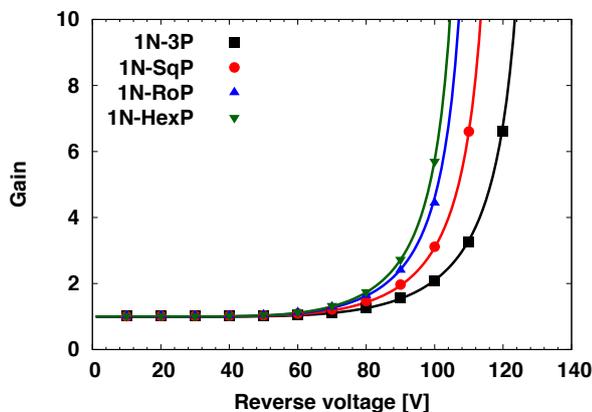


Figure 6.31: Gain-voltage curves simulated with the 1D model (continuous lines) and obtained from TCAD simulations (symbols).

The voltage dependence of gain was estimated using Eq.6.3 at different reverse voltages, giving an excellent agreement with TCAD simulation results, as shown in Fig.6.31. Since in the high-field region of structures 1N-3P (c), 1N-SqP (d) and 1N-HexP (f) the electric field has a rotational symmetry, the model developed for the cylindrical case was extended also for these devices. Even if the models do not match in the low-field regions of the devices, the good correspondence of the high-field region within 2-3 μm from the n^+ column ensures a reasonably accurate noise factor estimation. To account for the different device geometries, the external electrode radius r_d in Eq.6.2 was used as a fitting parameter, adjusting its value to match the avalanche gain simulated with the 1D model with the 3D TCAD simulation results. Gain-voltage curves obtained for these 3 structures are shown in Fig.6.31 together with the cylindrical reference structure (1N-RoP).

Differently from conventional commercial avalanche photodiodes, which feature pure electron injection in the avalanche region in order to minimize the noise factor, in the examined structures charge is generated also into the avalanche region. It is therefore necessary to estimate the noise factor as a function of position in which the electron-hole pair is generated. The position-dependent noise factor can be calculated with the following equation, adapted from [185]:

$$F(x) = 2 + \frac{1}{M(x)} \left[2 \int_0^w \alpha_n M^2(x') dx' - M^2(w) \right]. \quad (6.4)$$

$F(x)$ is plotted in Fig.6.32 for the cylindrical geometry at different bias voltages. In Fig.6.33, the noise factor F as a function of multiplication gain M is shown in the case of pure electron and pure hole injection (at the interface with the n^+ column). Although the data reported in Fig.6.33 were calculated for the cylindrical trench geometry, it was found

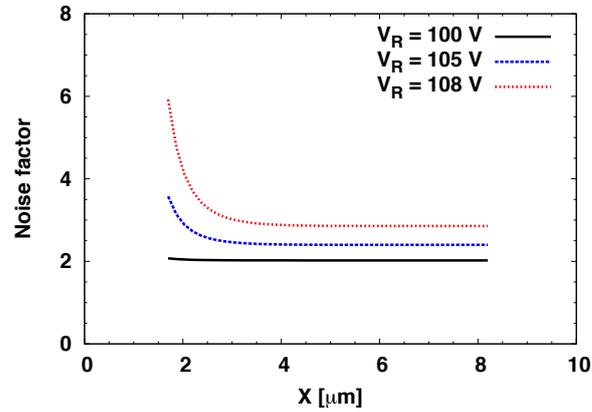


Figure 6.32: Position-dependent noise factor calculated with the 1D model.

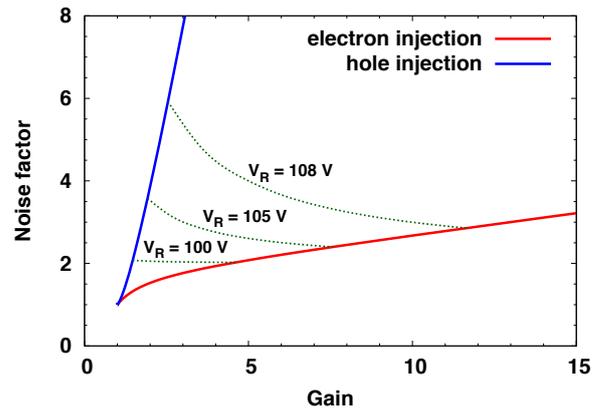


Figure 6.33: Noise factor as a function of gain for the two cases of pure electron and pure hole injection. Intermediate cases, representing generation inside the high-field region, are shown as dotted lines at 3 different voltages.

that for the other 3 device geometries the same curves are almost coincident, varying less than 3% at $M=10$. It can therefore be concluded that the noise factor vs. gain curves obtained for the cylindrical geometry are also representative of the devices (c), (d) and (f), although with different bias voltages.

In Fig.6.33, the curves of F as a function of M are also reported at different locations inside the device for three different reverse voltages. These data, also plotted in Fig.6.30 and Fig.6.32 as a function of X , appear in Fig.6.33 as lines joining the two extreme cases of pure electron and pure hole injection. It can be noticed that, if the gain obtained far from the n^+ column is maintained at moderate values, i.e. below 10, the corresponding worst-case noise factor in the high-field region does not exceed 6, and is therefore not harmful for the operation of the device.

Effect of avalanche gain and noise on particle tracking

An obvious drawback of avalanche multiplication in spectroscopic measurements is the dependence of generated signal charge on the position inside the detector, shown in Fig.6.30. On one hand, therefore, the presence of a non-uniform avalanche gain inside the detector would cause unwanted distortions in charge measurements, making the proposed detectors unsuitable for spectroscopy applications. On the other hand, this is not a severe limitation in particle tracking applications, since an accurate charge estimation is not required. In this paragraph we will discuss the introduction of avalanche multiplication to increase the detection robustness in tracking application.

In particle tracking, rough energy estimation is used to discriminate particle detection events from spurious noise events. The optimal threshold for event discrimination is limited on the lower level by the Equivalent Noise Charge (ENC) of the detector system, and on the higher level by the lower limit of the generated charge PDF, which follows a Landau distribution [27, 189]. In this paragraph, the effect of avalanche gain and noise on both ENC and charge distribution will be analyzed. In an electronic detector system, the ENC can be expressed as [35, 36]:

$$ENC^2 = A_w C_T^2 \frac{A_1}{\tau_p} + A_f C_T^2 A_2 + B_w A_3 \tau_p \quad (6.5)$$

where A_1 , A_2 and A_3 are constants depending on the type of shaping filter, τ_p is the signal peaking time after the shaping amplifier, C_T is the total capacitance at the input of the preamplifier, and A_w , A_f and B_w are terms accounting for white series noise, $1/f$ noise and white parallel noise, respectively. In particular, the detector leakage current noise spectral density $2qI_{det}$ enters in the B_w term. In the presence of avalanche multiplication, this last term is increased to $2qFM^2I_{det}$. It is worth noting that the factor FM^2 as a

function of position in the detector reaches the maximum in the case of pure electron injection, i.e. when the charge is generated far from the n^+ column.

In tracking applications, where the peaking time is very small, in the order of 20 ns, the parallel noise is typically negligible. However, the presence of avalanche gain increases its relative importance and it is necessary to keep M to a moderate value. A first-order estimation of the effect of avalanche can be done considering a typical situation with $A_3=0.92$ ($e^2/8$, for a RC-CR shaping), $\tau_p=20$ ns and $I_{det}=13$ nA. This last value was estimated from TCAD simulations, considering a detector pixel size of $250 \times 50 \mu\text{m}^2$, a thickness of $70 \mu\text{m}$, the radiation damage corresponding to 2×10^{16} n_{eq}/cm^2 and an operating temperature $T=-20$ °C.

For an applied bias voltage of 100 V ($M=4.6$ and $F=2$) the contribution of avalanche noise to ENC is 356 electrons rms, substantially larger than the leakage current shot noise in the absence of multiplication (55 electrons rms). Since in pixels for tracking applications the usual ENC is in the order of 200 electrons [190], the effect of avalanche on ENC becomes dominant also in the case of moderate gain. The first term in Eq.6.5 predicts a proportional contribution of the total input capacitance to the ENC. It is therefore necessary to estimate the possible impact of the increased capacitance of the proposed detector with respect to existing solutions. Considering a detector capacitance of 30 fF for a $20 \times 20 \mu\text{m}^2$ cell with $70 \mu\text{m}$ thickness, a projection to an area of $250 \times 50 \mu\text{m}^2$ yields a total capacitance of 900 fF. In the new ATLAS frond-end chip FE-I4A [113], the contribution of the capacitance to ENC is estimated as $0.15 e^-/\text{fF}$ [191], resulting in 135 electrons for 900 fF capacitance. Although this value would significantly increase the total ENC, its impact would be considerably reduced in the presence of avalanche multiplication. Moreover, reduction of pixel size and aggressive thinning can make its influence negligible in future developments.

In addition to the detector leakage current, avalanche noise also affects the charge signal delivered by the detector. The variance in the detector charge in the presence of avalanche multiplication can be modeled as [192]:

$$\sigma_D^2 = M^2 \sigma_L^2 + NM^2 (F - 1) \quad (6.6)$$

where σ_L^2 is the variance due to the Landau distribution, and N is the number of primary generated electrons. In the case of charge spectrum measurement, the energy resolution can be expressed as [193]:

$$\frac{\Delta E}{E} = \sqrt{\left(\frac{ENC}{MN}\right)^2 + \frac{F-1}{N} + \frac{\sigma_L^2}{N^2}} \quad (6.7)$$

where σ_L^2 takes the place of the variance in number of photons generated in the scintillator, originally referred to in [193]. The contributions of the Landau distribution width σ_L/N

and avalanche noise $\sqrt{(F-1)/N}$ to energy resolution $\Delta E/E$ can be estimated in a typical scenario. Let us consider a Minimum Ionizing Particle (MIP) incident on a $70\ \mu\text{m}$ thick detector and a worst-case value for $F=6$, obtained at $V_R=108\ \text{V}$ for pure hole injection (Fig.6.33). Accounting for a conversion factor of $80\ \text{e}^-/\mu\text{m}$, the MIP will generate on average $N=5600$ electrons and the contribution of noise factor to $\Delta E/E$ will be 7% FWHM. For the same detector thickness, the charge delivered to the detector has a spectral width of 56% FWHM [189], which would be mostly unaffected by the avalanche noise. For thinner detectors, both terms will increase, but their ratio will remain substantially unchanged. It can therefore be concluded that, in all the practical cases, a moderate gain will not increase the relative spectral width of the generated charge.

For particle tracking applications, the threshold upper limit is determined by the need of high detection efficiency. In the case of pixel detectors, a threshold setting at $N/6$ was experimentally demonstrated to yield acceptably low detection inefficiency around 1% [190]. It is worth noting that if the events are shared among different pixels, the generation takes place far from the n^+ column, and the most favorable gain obtained in the case of pure electron injection is exploited. On the contrary, the electron cloud generated by particles detected close to n^+ columns is absorbed by one single pixel, offering a more relaxed constraint for the high threshold setting.

The lower limit for the threshold is determined by the ENC of the readout channel. In order to avoid an excess of spurious detections, a threshold value around 10 ENC is typically applied in pixel detectors [190]. We can therefore estimate the lower limit (10 ENC) and the upper limit ($N/6$) for the threshold setting and find the minimum detector thickness for which both conditions of low spurious event number and low detection inefficiency are verified. This estimation is reported for the case of no avalanche multiplication in Fig.6.34(a) and moderate avalanche multiplication ($M=4.6$) in Fig.6.34(b), considering the simulation data in [189], a conversion factor of $80\ \text{e}^-/\mu\text{m}$ to estimate N , and an ENC value of 150 electrons for the pixel electronics, compatible with ATLAS FE-I4A readout chip [113]. As discussed before, the relative charge distribution broadening due to avalanche noise has been considered negligible, as well as the contribution of detector capacitance to the ENC. If no avalanche multiplication is present, the lower and upper threshold limit curves cross at a detector thickness of approximately $125\ \mu\text{m}$, which can be considered the minimum feasible detector thickness for optimal operation in the absence of multiplication.

The lower limit increases in the presence of avalanche gain due to the noise contribution associated to the multiplied detector leakage current. However, in this case the increase in the upper threshold limit is considerably more relevant, as shown in Fig.6.34(b), leading to a minimum thickness of $57\ \mu\text{m}$ for optimal operation.

This estimation shows that the introduction of avalanche multiplication could enable

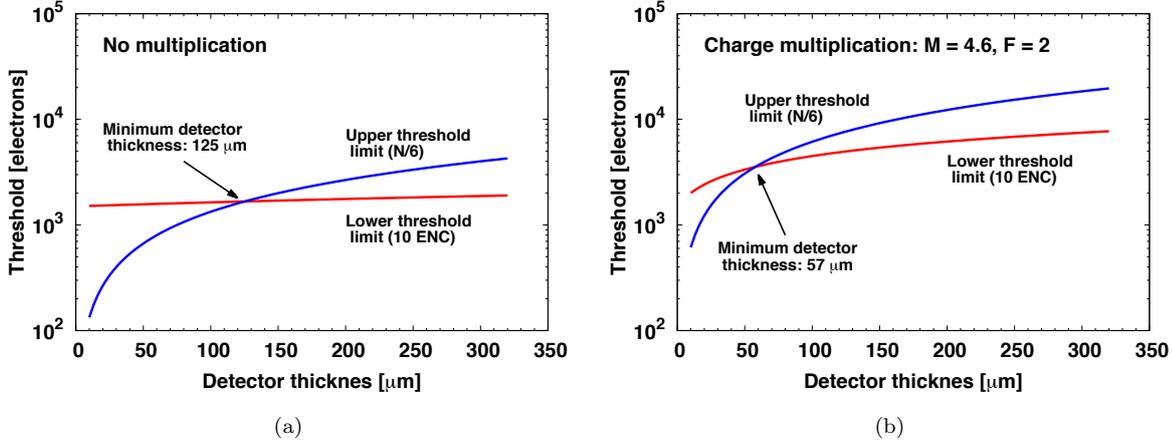


Figure 6.34: Upper and lower threshold in the absence of gain (a) and with moderate avalanche multiplication (b).

the thinning of detectors down to a few tens of micrometers. In this calculation, a detector size of $250 \times 50 \mu\text{m}^2$ was considered, but avalanche multiplication could be even more effective for smaller pixels, where the total current will reduce proportionally with the pixel area.

6.4 HYbrid DETectors for neutrons (HYDE)

Besides particle tracking applications, 3D technology can also be adapted to fulfill other purposes. In particular, a field currently drawing many attentions is the detection of neutrons with high spatial, energetic and timing resolution. Many fields require an accurate neutron detection, and among them are particle physics, nuclear physics, explosives detection, medical physics and many others [194, 195]. Because silicon is not itself able to detect neutrons, it must be coupled to scintillating materials that will convert the impinging particles in other kinds of radiation detectable by silicon. In particular, many devices aiming to detect thermal neutrons were made available in the past years, using silicon diodes featuring specifically designed cavities (similar to 3D detectors) that were covered/filled with inorganic materials based on ^6Li or ^{10}B [196, 197, 198, 199, 200, 201]. The advantage of realizing cavities filled by converting materials instead of just covering planar devices with the same compounds, lays in the increased probability of the reaction products (typically alpha particles and tritons) to interact with silicon. Being generated deeper inside the device, the solid angle available to particle to penetrate into silicon becomes larger, increasing the detection probability. Fig.6.35 shows the comparison between two reaction products generated inside a trench region or inside a surface material,

clearly demonstrating the highest detection probability of the former. These devices returned very promising results but with lower efficiencies with respect to theoretical expectations. This fact is to be ascribed to the range of the reaction products, that, if the cavity design is not properly tuned, might not be able to escape the converting material and penetrate into silicon or might exceed the available silicon width entering the neighboring converting cavity. In addition, the detection of the reaction products can be perturbed by the morphology of the interface between the converting materials and silicon, further reducing the total efficiency of the sensor.

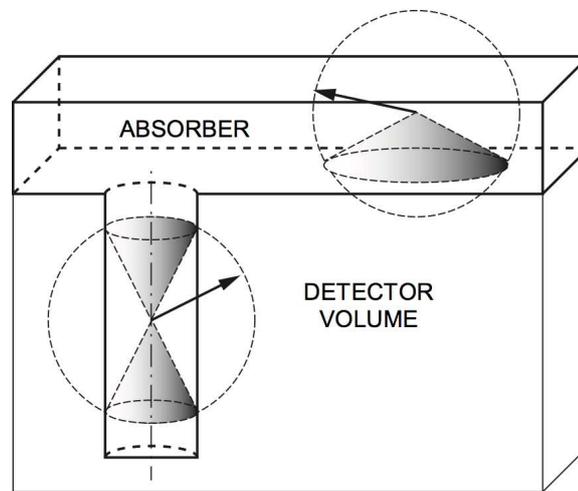


Figure 6.35: The solid angle available for the detection of a reaction product generated inside a trench is larger than the one for the same reaction product generated on the surface [198].

Currently, no similar systems are available for the detection of fast neutrons having energies of a few MeV. The easiest way to realize this, would be to detect and analyze the recoil protons from organic materials, but the efficiency of the systems proposed in literature would still be affected by the same problems.

In order to find a solution to the discussed issues, a collaboration between the INFN research groups of Trento and Legnaro (Padova, Italy) and FBK was formed. The main aim of this collaboration was to join the efforts and expertise related to 3D silicon detectors and organic scintillating materials, to design and realize a new hybrid and highly efficient kind of neutron detector.

The devices will be realized in the framework of the INFN project *HYDE* (HYbrid DETectors for neutrons). The main idea is to fabricate structures based on the insertion of organic scintillators inside the cavities of a specifically designed 3D detector, able to sense both the recoil protons and the scintillating light resulting from the neutron conversion in a newly designed scintillating material. This approach will allow to make the

neutron conversion volumes active as well, allowing to increase their size and, therefore, the detection efficiency of the system. This type of device would allow to perform spectroscopic or 2D analysis of the impinging neutrons.

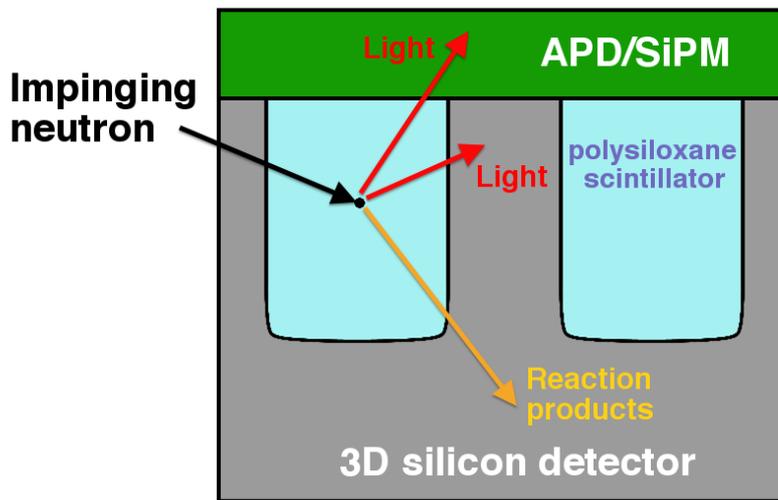


Figure 6.36: Conceptual sketch of the proposed 3D structure coupled to a polysiloxane scintillator and a multiplication silicon detector (APD/SiPM).

As already discussed in this work, 3D technology at FBK is now reliable and allows to plan the realization of modified structures. In order to ease the realization of the first prototypes, it was decided to investigate the possibility of realizing a 3D silicon detector in a Single Type Column (STC) configuration, with only one type of electrodes actually 3D and not passing through the entire bulk, while maintaining the other type of electrode planar [81]. The cavities, representing the junction electrodes in the proposed STC devices, are planned to be filled with modern polysiloxane organic scintillators, specifically designed to detect both thermal and fast neutrons [202, 203, 204, 206]. These materials proved to be very radiation tolerant and returned scintillation efficiencies in response to charged particles and gammas, between 50 and 70% with respect to the best commercial plastic scintillators. In addition, polysiloxane scintillators are very effective in detecting neutrons due to the possibility of inserting high quantities of boron compounds inside them [205] without drastically reducing the light transport inside the material. The greater advantage of these materials is the fact that, being synthesized using polysiloxane resins, they can easily be introduced inside complex structures such as the electrodes of the proposed 3D sensors. A sketch of the preliminary sensor structure is reported in Fig.6.36, where the large 3D cavities are filled with a polysiloxane scintillator. The reaction products and the scintillation light, will be detected by the bulk of the 3D sensor. In order to prevent

possible efficiency reduction related to the poor light transmission of the trench walls, the system can easily be coupled to a multiplication photodetector (APD/SiPM) on one of the surfaces to increase the light detection probability.

The results reported in this work are mainly related to the simulation, design and testing of the bare silicon detectors.

6.4.1 Computer aided design of the silicon detectors

In order to realize the desired 3D structures some issues have to be addressed. From the electrical point of view, it is known that STC devices feature rather low electric fields between columnar electrodes that cannot be enhanced by further increasing the bias voltage. In addition, in order to ease the deposition of the converting material, the 3D cavities must be made wider than standard columnar electrodes. As previously described in section 6.2, when trenches are etched into silicon, the following lithographic steps will become very complicated if the resulting structures are not filled to restore the wafer surface planarity. Since the converting material will be deposited after the devices are completely fabricated, the etched cavities will need to remain open during the entire fabrication, making the lithography of one side of the wafer impossible after the DRIE step. This will not allow for the metal deposition and patterning on the trench side thus forcing the following process steps to be performed in a single sided fashion. For this reason, the contact with the trenches needs to be performed from the other side of the wafer. The more convenient way of doing so, is by means of columnar holes penetrating the bulk up to the trench bottom edge and filled with doped polysilicon to assure the electrical contact. The planar electrode can instead be realized as a standard implant on the same wafer surface of the polysilicon pillars. A sketch of the intended detector design is reported in Fig.6.37(a). The bulk will be p-type, the large n^+ trench structures, in which the converting material will be deposited, are connected by polysilicon pillars reaching the front side of the wafer. On the same wafer side, the bulk contact is provided by means of planar p^+ implantations.

The structure used to perform the initial numerical simulation study is reported in Fig.6.37(b). In order to limit the computational time, 2D simulations were performed: the n^+ trenches and pillars, visible in red, were grounded while sweeping the p^+ implantation present at an x coordinate of $200 \mu\text{m}$ (in blue). The p-spray implantation is present between the trenches on the upper surface.

The first performed study was related to the depletion dynamics inside the device. Fig.6.38 shows the hole densities for different applied bias voltages: full depletion of the region between the trench bottom surface and the opposite wafer surface is reached already before 5 V due the short n^+ to p^+ distance, while higher voltages are required to achieve

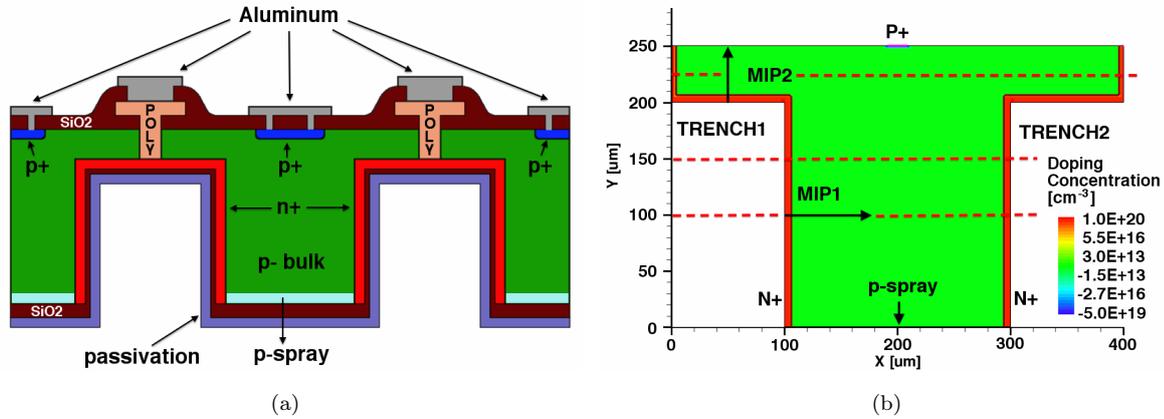


Figure 6.37: The conceptual sketch of the planned 3D structure is shown (not to scale) (a) together with the 2D structure used for the preliminary simulation process (b). The direction along which electrical quantities are extracted from simulated data are shown with dashed lines. The two investigated hit positions for the simulated impinging particles are also reported.

lateral depletion between the trenches (roughly 10 to 15 V). Because of the presence of the p-spray, required to assure isolation between the n⁺ trenches, the surface region between the cavities results to be more difficult to deplete (a reasonable depletion is obtained at roughly 50 V). This should not affect the operation of the devices and should become less evident when the oxide layers will be damaged by the gamma background radiation.

Another important information that can be extracted from numerical simulation results, is the distribution of the electric field inside the device. Fig.6.39 shows the 1D electric field profiles extracted from simulated data, for different y coordinates (100, 150 and 225 μm , see dashed lines in Fig.6.37(b)) as a function of the p⁺ implantation widths and for a bias voltage of 50 V. As expected from the previous experience with STC detectors, the field between the n⁺ electrodes is rather low (Fig.6.39(a) and 6.39(b)), and it is not possible to further increase it by applying higher biases. In the bottom part of the structure and underneath the trenches, the field is stronger and is largely affected by the width of the ohmic implantation, with larger implants yielding higher electric field peaks but less uniformity.

The second study performed by means of numerical simulations is related to the dynamics of charge collection in different regions of the device. Before proceeding with the device simulation, it was important to estimate the expected range of the reaction products in silicon. The interaction of neutrons with the polysiloxane scintillator is expected to return recoil protons with energies in the range from 100 keV to 5 MeV. The amount of released charge per micron in silicon was estimated using the SRIM software [207] and the returned profiles (shown in Fig.6.40) were fed to the device simulator. It is important to

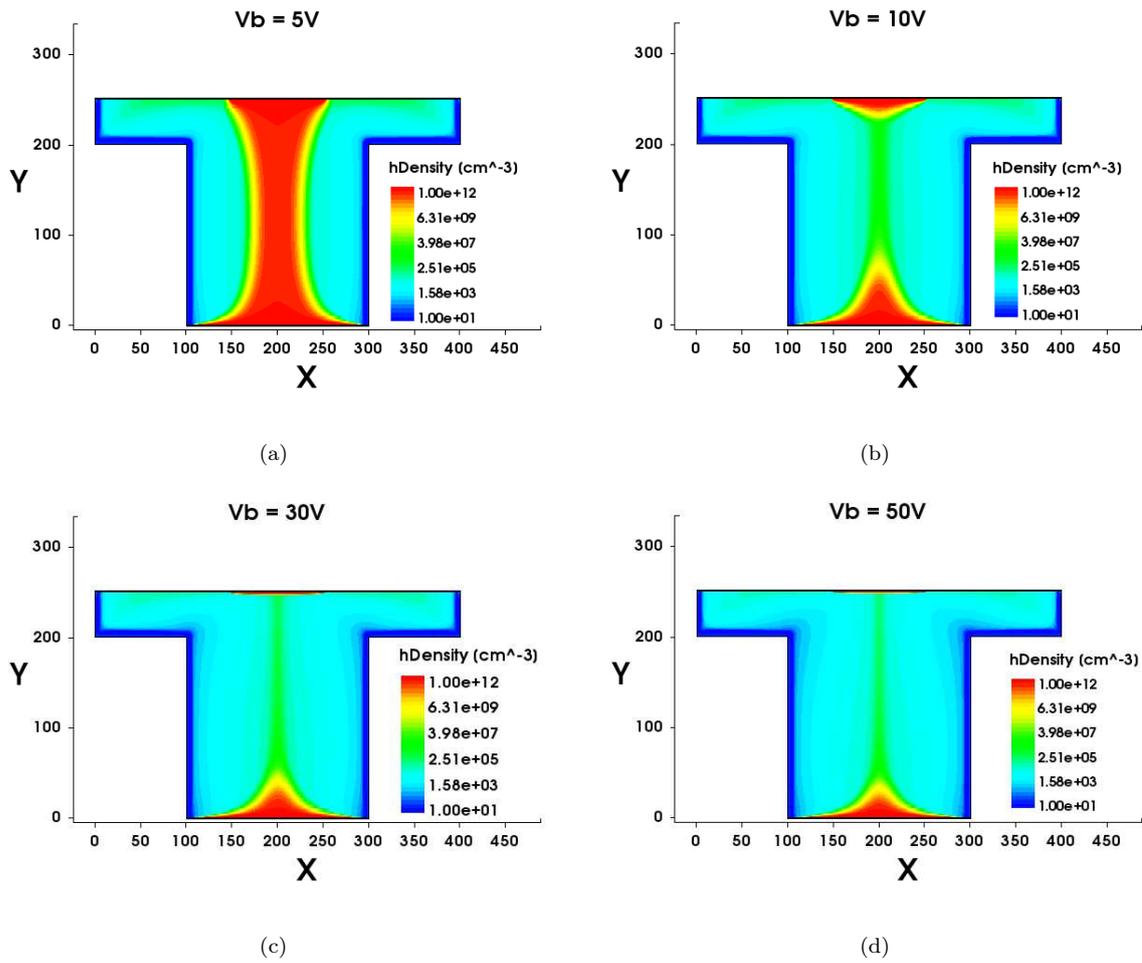


Figure 6.38: Simulated hole density for different bias voltages: 5 V (a), 10 V (b), 30 V (c) and 50 V (d).

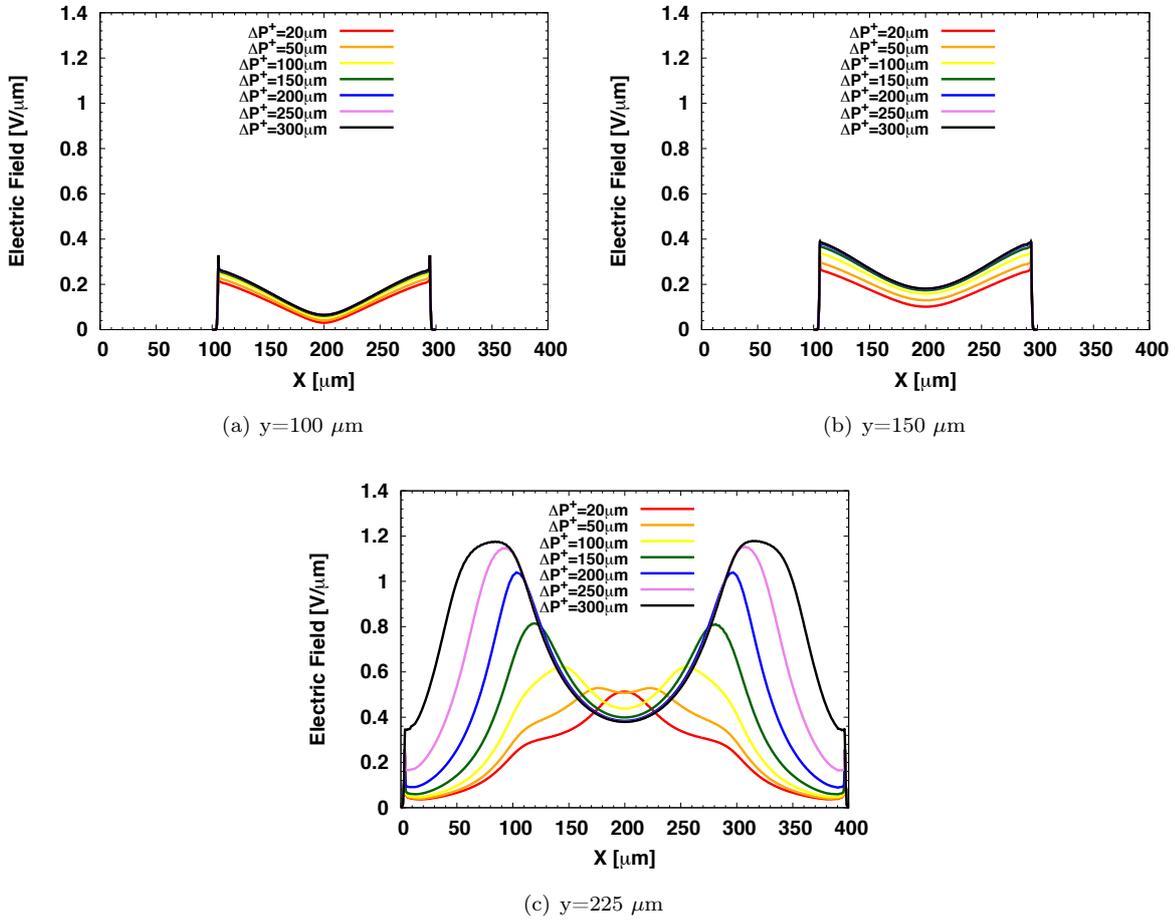


Figure 6.39: Simulated electric field distribution as a function of the p^+ width for three different y coordinates: 100 (a), 150 (b) and 225 μm .

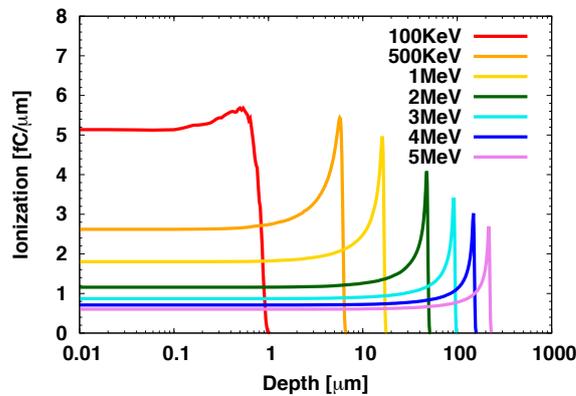


Figure 6.40: Released charge per micron for the expected recoil protons produced from the interaction between neutrons and polysiloxane materials. The expected energy range is between 100 keV and 5 MeV.

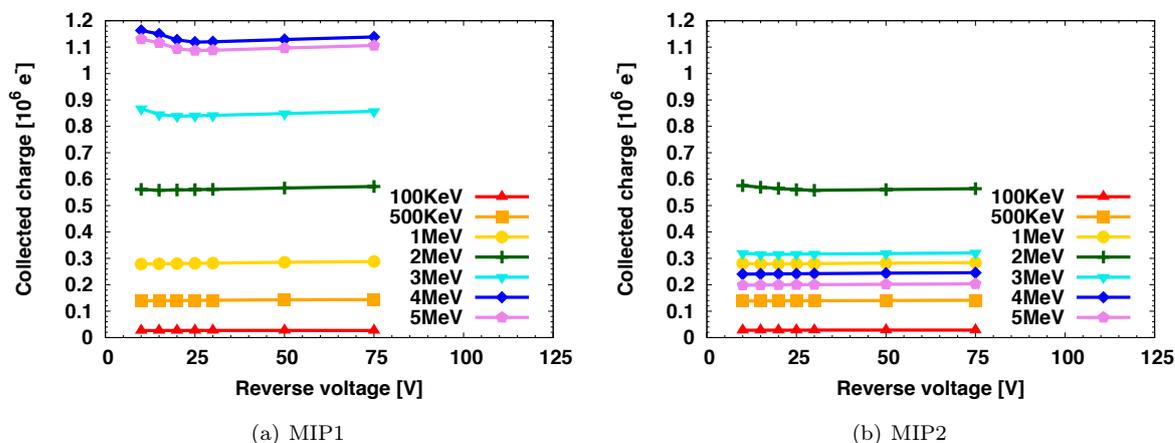


Figure 6.41: Collected charge as a function of the bias voltage for protons with different energies and for both investigated hit positions: horizontal (MIP1) (a) and vertical (MIP2) (b).

notice that these results suggest that the examined protons have a range between roughly $1 \mu\text{m}$ and $200 \mu\text{m}$. A transient simulation was performed for different bias voltages and considering two different particle hit positions and angles, one horizontal between the two trenches and the other one vertical, exiting from the bottom of one of the trenches (marked as MIP1 and MIP2 in Fig.6.37(b)). The two trenches are simultaneously readout in a diode-like mode. Charge collection as a function of the bias voltage for all the investigated proton energies and for both hit positions is reported in Fig.6.41. In both cases charge saturation is reached rather quickly (as expected from the previously discussed electrical simulations) and an obvious dependence of the amount of collected charge from the proton energy was found. The MIP1 hit position (horizontal, Fig.6.41(a)) shows an increasing amount of collected charge with respect to proton energies up to 4 MeV protons. For higher energies, the Bragg peak partially enters the neighboring trench, resulting in a slight charge loss. The MIP2 case (vertical, Fig.6.41(b)) returns lower charge values because of the lower amount of silicon available ($\sim 50 \mu\text{m}$). In this case the higher charge is generated by the 2 MeV proton (range of roughly $50 \mu\text{m}$ in silicon), while particles with higher energies are able to escape silicon because of the low thickness in this region of the detector. These simulations allowed to understand that, with the intended trench geometry, it should be possible to detect the reaction products in a rather efficient way, even for less fortunate events (e.g. vertical particles).

6.4.2 Wafer layout and fabrication

Although the final objective would be to realize pixelated detectors, the first batch only includes diode-like structures, in order to ease and speed up the electrical and functional

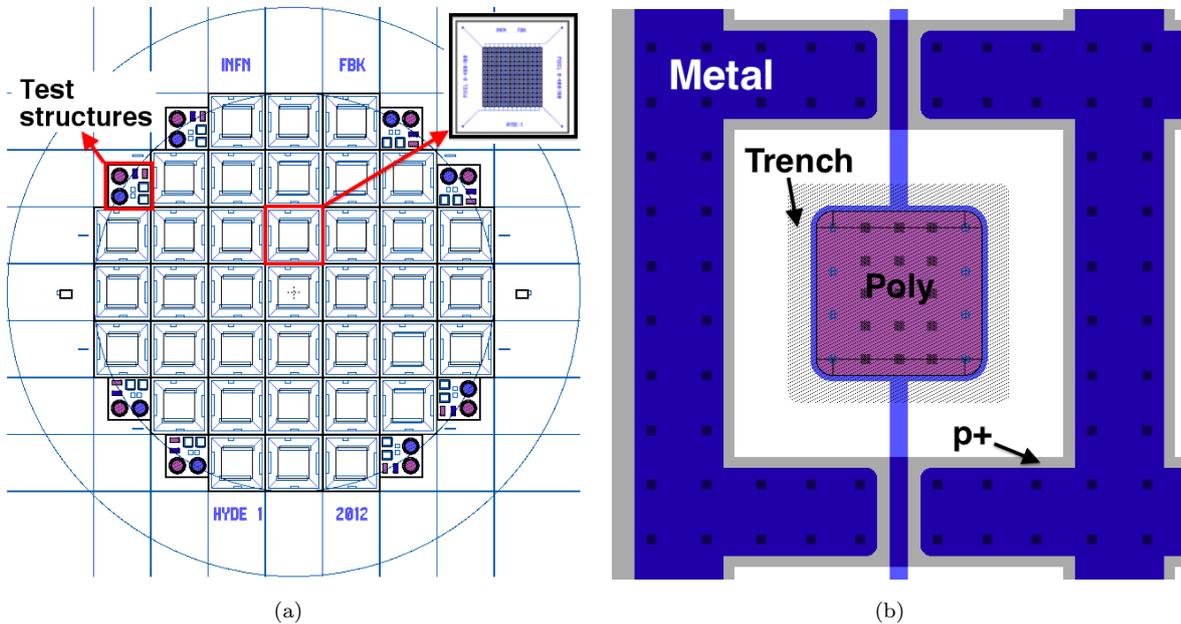


Figure 6.42: Wafer design of the first batch of devices (a) and elementary cell of one of the silicon sensors (b): the p^+ implantation is visible in grey while the metal is shown in blue, the dotted area corresponds to the trench while the red region is the polysilicon that penetrates inside the blue circles which are the pillars connecting to the cavity.

characterization. Once the neutron detection capabilities of the planned hybrid detectors will be demonstrated, a new layout will be designed, implementing more complicated structures. The wafer layout is shown in Fig.6.42(a). It includes a total of 37 devices having an active area of roughly $1 \times 1 \text{ cm}^2$ and with small differences in the geometrical implementation. The usual planar test structures are included as well. The basic cell of one of the sensors is reported in Fig.6.42(b). The standard cavity (dotted region) was designed trying to ease the deposition of the converter while leaving sufficient mechanical strength to the silicon wafers. The trenches have a square shape with sides of $200 \mu\text{m}$, depths of the same dimension and are doped (n^+) with a Phosphorus diffusion from solid source. The connection to the cavities is provided by means of eight polysilicon filled pillars etched from the opposite side of the wafer. The metal providing electrical connection to the pillars and therefore to the trenches, is deposited on top of the polyisilicon deposited on the wafer surface (in red in Fig.6.42(b)). On the same wafer side as the polysilicon deposition, a p^+ implantation is performed which is then covered by metal. The standard p^+ width was designed to be $100 \mu\text{m}$. Four pads are available in the device corners to perform the electrical connections to the readout system. The full device is realized by repeating the described basic cell in a matrix. Following the indications provided by numerical simulations, the standard device configuration has a $200 \mu\text{m}$ gap between the

Table 6.3: Different device geometrical variations implemented in the wafer layout.

Device name	Trench pitch (d) [μm]	Matrix size	p ⁺ width [μm]	Hole diameter [μm]
-	-	-	-	-
8-400-50	400	13×13	50	8
8-400-100	400	13×13	100	8
8-400-150	400	13×13	150	8
8-400-200	400	13×13	200	8
6-400-50	400	13×13	50	6
6-400-100	400	13×13	100	6
6-400-150	400	13×13	150	6
6-400-200	400	13×13	200	6
8-300-50	300	17×17	50	8
8-300-100	300	17×17	100	8
8-350-50	350	15×15	50	8
8-350-100	350	15×15	100	8

walls of two neighboring cavities, resulting in a pitch of 400 μm between their centers.

Some geometrical variation of the same structures were also implemented, by changing some of the basic layout parameters: the inter-cavity distance, the p⁺ width and the connecting column diameter. All the available configurations are reported in Tab.6.3.

The fabrication process of these devices shares many steps with the standard 3D process available at FBK. Devices were fabricated on the same wafers used in the IBL production, having a thickness of 230 μm , making the region underneath the cavities roughly 30 μm thick. Thanks to the well calibrated DRIE process, the etching and doping of the trenches resulted to be not critical, despite their large size. The most critical step was the realization of an electrical connection using columnar holes. Luckily, because of the small silicon thickness to be etched, this process did not cause any problems and the polysilicon filling of the holes resulted rather easy. The remaining process steps, were standard implantations, metal depositions and patterning, and were not cause of any worries. The mechanical yield of the batch was very good. A slight variation of the fabrication process was performed only on some wafers: instead of filling the pillars with polysilicon, they were doped with the same phosphorus diffusion of the cavities and they were connected by a surface n⁺ diffusion, in a 3D sensor fashion. The motivation for this process splitting was related to the fact that the polysilicon deposition inside columnar holes at FBK was not fully demonstrated yet, while the second method was already successfully tested on several 3D sensor batches.

Some pictures of the most interesting regions of the fabricated devices are reported

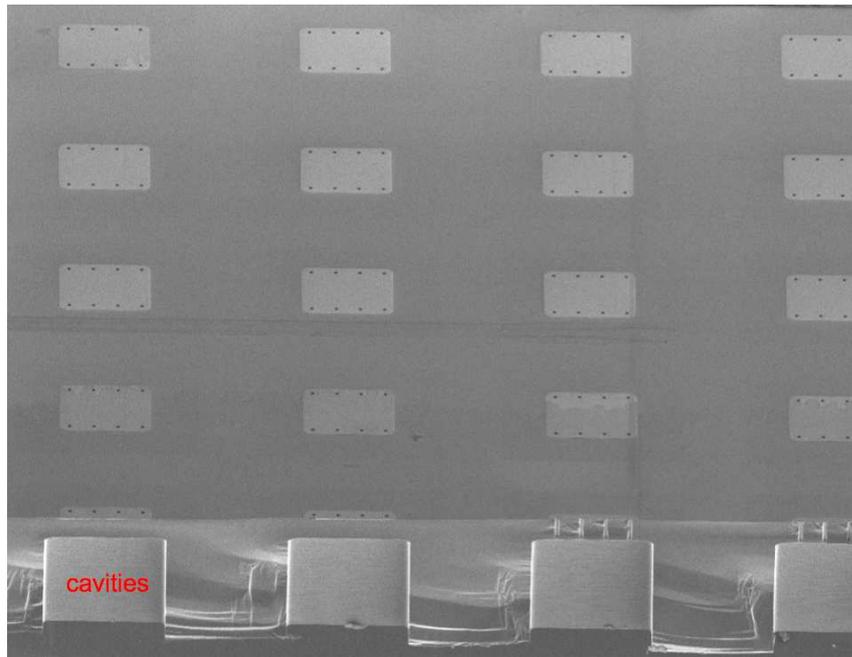
in Fig.6.43. The wafer was cleaved along a direction connecting several trenches in order to examine the outcome of the etching process. Some cavities are visible in Fig.6.43(a) featuring very uniform depths. An enlargement of one of the cavities is reported in Fig.6.43(b) where the connecting pillars are visible as well. The distance between the bottom of the trench and the opposite wafer surface was demonstrated to be in the order of $30\ \mu\text{m}$. Finally an enlargement of the pillars is reported in Fig.6.43(c) and shows how all of them reach the bottom of the trench to perform the desired electrical connection.

6.4.3 Electrical characterization

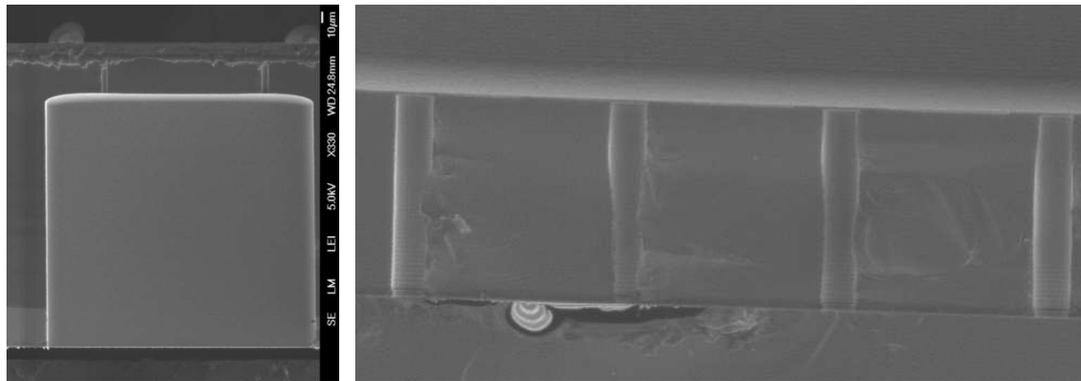
The first electrical tests were performed on wafer and were mainly focused on two aspects: verifying the goodness of the connections between the columnar electrodes and the trenches, and check the electrical yield of the process by means of I-V measurements on the fabricated devices. The first measurement was performed using a test structure specially designed to this purpose: multiple trenches were connected together only through the polysilicon pillars and not by surface layers, in this way it was possible to estimate the resistance across the entire series of cavities. The measurements proved this approach to be reliable and the connection resistances were found to be in the order of a few tens of ohms.

The second test, I-V measurement of the fabricated devices, were performed at the probe station by grounding all the cavities and by sweeping the potential of the p^+ contact. The results obtained from two different wafers, W2 and W10, are reported in Fig.6.44(a) and 6.44(b). The only difference between these two wafers is the fact that W2 features the polysilicon filling of the pillars while in W10 the connection was assured by using the dopant diffusion from solid source in the same way it is performed in FBK's 3D detectors. The current absolute value is very similar between the two wafers but the currents of devices from wafer W10 have a larger slope and the breakdown is anticipated, although the final discharge occurs at similar voltages in both wafers. In both cases the discharge is believed to occur at the trench to p-spray junction.

In order to study the dependence of layout parameters on the electrical characteristics, the I-V and C-V measurements for a specific subset of sensors were isolated and are reported in Fig.6.45. In particular, the chosen devices all feature an inter-cavity distance of $400\ \mu\text{m}$ and different p^+ widths. The currents reported in Fig.6.45(a) show a double knee effect, especially for lower p^+ widths. This effect might be attributed to the following phenomena: considering a square region containing four neighboring trenches, the $200\ \mu\text{m}$ of silicon between the sides of the cavities are depleted rather quickly, by applying roughly $5\ \text{V}$ (first knee at very low voltage). The situation is rather different along the diagonal between the trenches: the inter-cavity distance in this direction is in fact equal to $200\sqrt{2}\ \mu\text{m}$ (roughly $282\ \mu\text{m}$), requiring higher voltages to be fully depleted, thus the second knee in the I-V



(a)



(b)

(c)

Figure 6.43: Details of the etched cavities and pillars: cross-section of a large region of the devices (a), enlargement of one cavity showing also the columnar connections (b) and detail of the etched pillars (c).

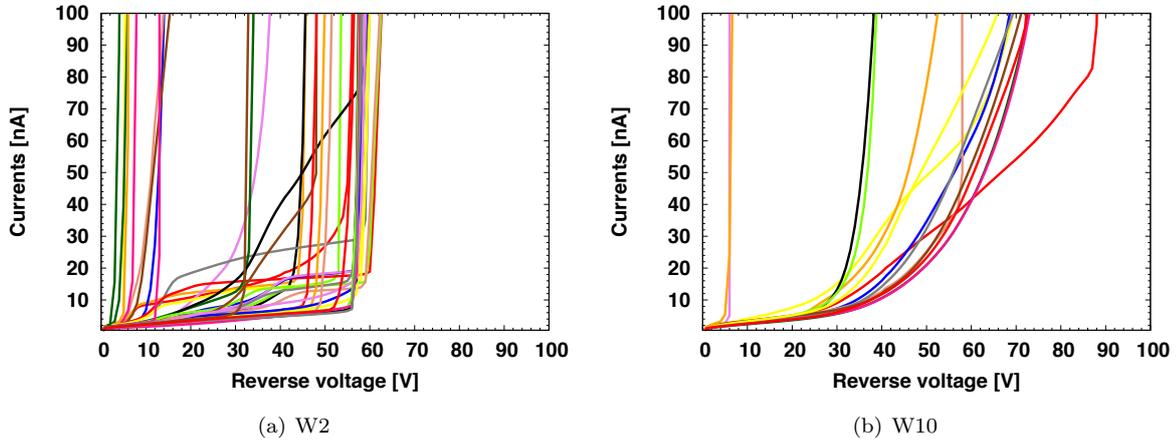


Figure 6.44: I-V curves of devices coming from two different wafers: W2 (a) featuring the polysilicon filling of the connecting pillars and W10 (b) without the polysilicon filling.

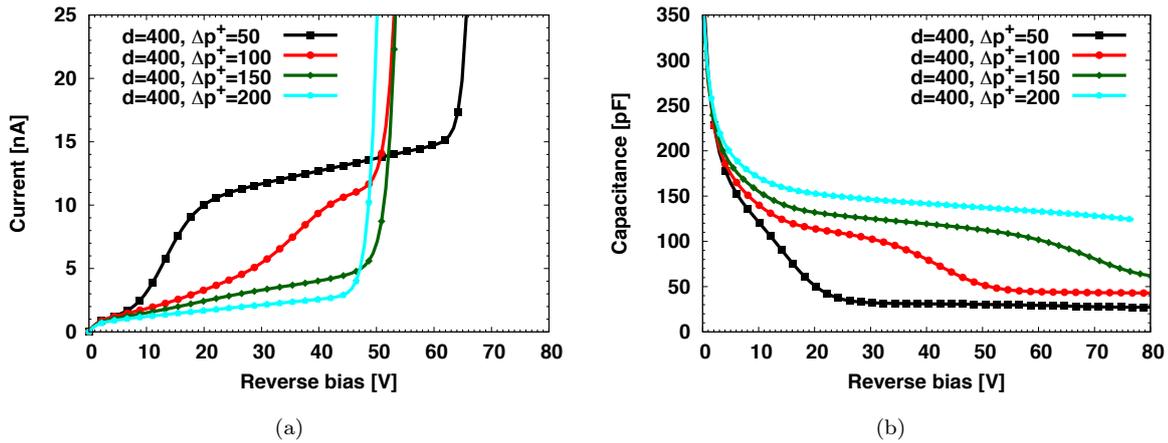


Figure 6.45: Measured electrical quantities as a function of the bias voltage and the p^+ width, I-V curves (a) and C-V curves (b) are reported.

curve. It is important to notice that devices having larger p^+ width show this effect at higher voltages, as can be observed for the device with Δp^+ equal to $100 \mu\text{m}$ in Fig.6.45(a) (the other two breakdown too early but is easy to understand that the second current knee is not reached yet). The cause of this effect can be attributed, in first approximation, to the fact that, by increasing the p^+ width, the electric field in the middle between two trenches, especially in the bottom of the trench, becomes lower, thus slowing down the depletion process (a similar effect can be seen in Fig.6.39(c) but for a different region of the device along the direction perpendicular to two neighboring trenches). Capacitance measurements reported in Fig.6.45(b) confirm the same double knee behavior found in I-V measurements. In addition, a slight offset in capacitance is found in devices with larger p^+ (this was expected because by increasing the area of an electrode, the total capacitance increases as well). The interpretation of this phenomenon appears to be sufficiently accurate but must be confirmed by means of numerical simulation that will need to be performed in three dimensions, in order to take into account all the critical aspects. Due to the very large dimension of the elementary cell, the structure to simulate is very large and requires a high number of grid points, considerably slowing the simulation process. The final results will require some time to be obtained.

6.4.4 Sensor assembly

The functional characterization of the devices will be performed in two different phases: tests on the bare sensors (without converting material) will be performed in laboratory at the University of Trento by means of radioactive source scans (β and α) and laser scans. Devices will then be shipped to Laboratori Nazionali di Legnaro (LNL) in order to fill the cavities with the polysiloxane converter and to test them with a neutron beam. In order to ease the testing and the deposition of the converting material a specific support PCB was designed. The board features a hole of roughly 7 mm in diameter able to contain the entire active area of the device. The silicon around the active-area will function as support and will be glued to the metal pad surrounding the hole. The hole will allow to pour the scintillator inside the cavities and will also function as containment for it. Several gold plated pads are available on the board front side to perform the wire bonding of the devices and provide connections to the readout system. A sketch of the final assembly of the sensor before deposition is reported in Fig.6.46(a). In addition, since the deposition process will be performed after the wire bonding, the wire bonds were realized in a redundant way (two wires per connection) and were encapsulated using an epossidic resin that will protect them during the deposition and later testing.

Two wafers were cut in December 2012 and the devices were remeasured in order to assure that no damage was suffered during the process. Three devices from wafer W2

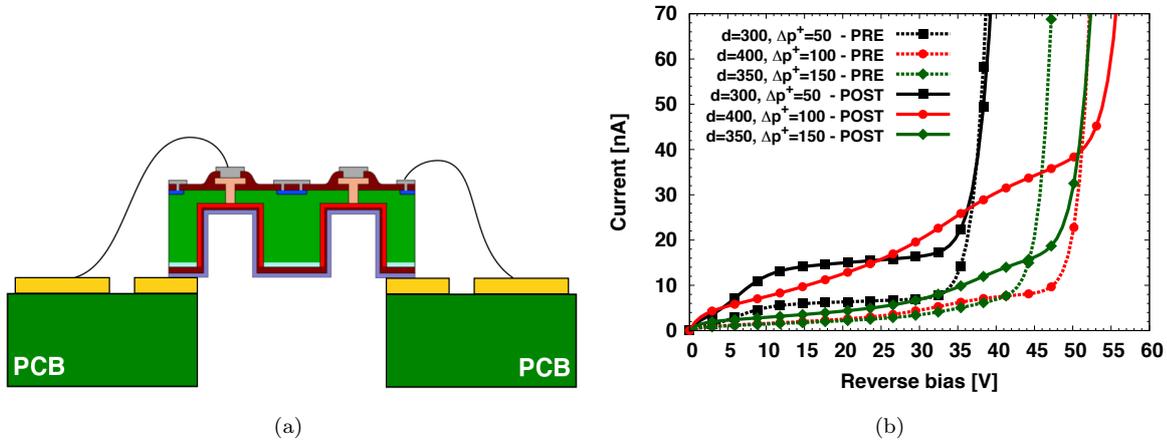


Figure 6.46: Sketch of a device assembled to the support PCB (a) and comparison between PRE and POST bonding I-V measurements (b).

were wire bonded to the mentioned supports for further electrical and functional testing. Fig.6.46(b) shows the comparison between pre-bonding I-V measurements (dashed lines) and the same data post wire bonding (solid lines). The general effect is a slight increase of the device leakage current (not expected to deteriorate the noise performances) and a small increase in breakdown voltage. After the final electrical characterization one of the devices was kept at University of Trento to test and optimize the readout system while two devices were sent to LNL for the trench filling in view of the upcoming neutron beam tests.

The cavities filling tests were first performed on bad devices from wafer W2 (exhibiting very low breakdown voltage). The converting material, initially in liquid form, was poured onto the etched surface of the sample and was let to solidify. Devices were then cut along a line passing through the trenches in order to investigate the outcome of the procedure. The first analysis was performed at the optical microscope and one of the images is reported in Fig.6.47(a). The first impression is in favor of an incredibly good filling of the cavity with the material adhering very well to the trench surfaces. To gather more informations, a Scanning Electron Microscope (SEM) analysis was performed on the same samples. A picture of two neighboring trenches is reported in Fig.6.47(b) while Fig.6.47(c) shows the enlargement of one single cavity. This analysis confirmed the very good conformity of the filling also in the bottom corners, regions that were thought to be more difficult to properly fill (see Fig.6.47(d)).

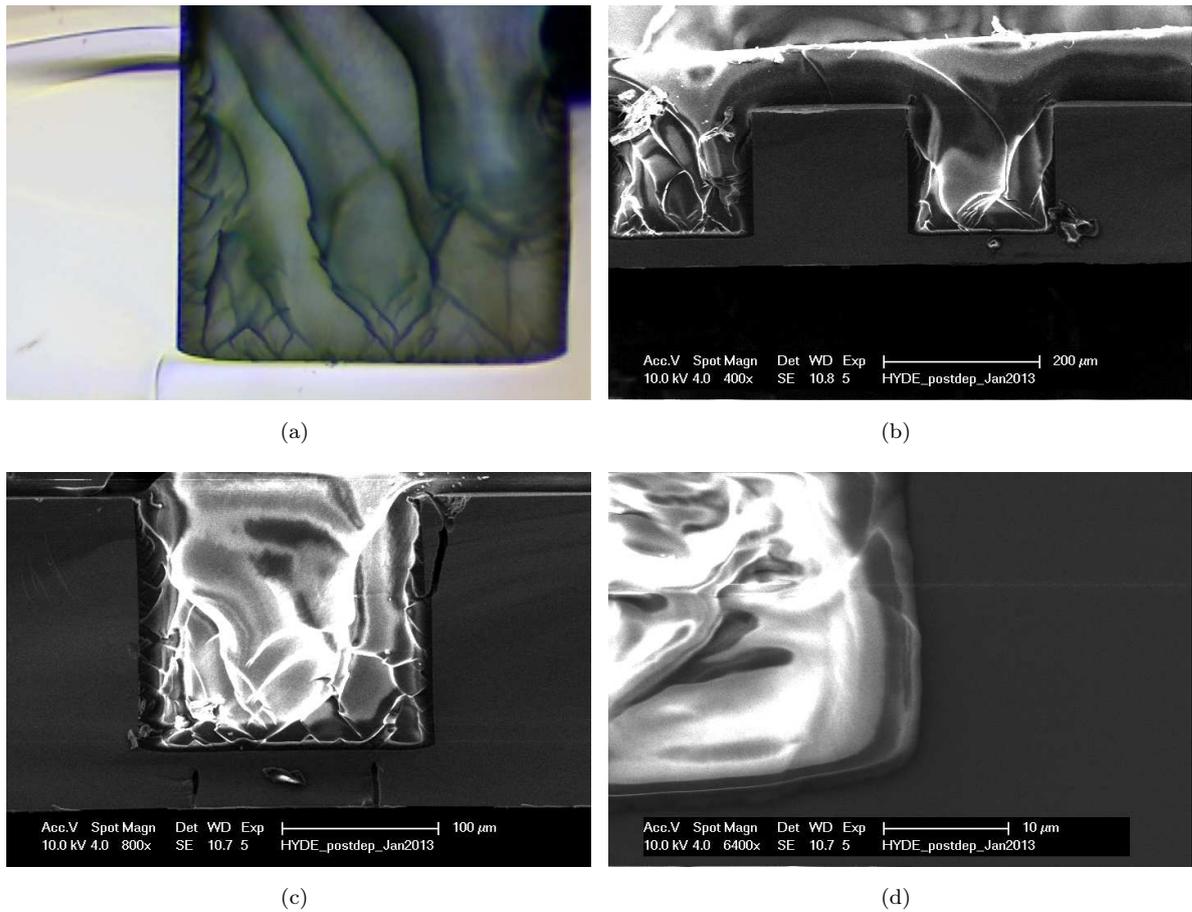


Figure 6.47: Pictures of the cavities filled with the converting material: optical microscope image (a), SEM images of a region including two trenches (b), the enlargement of a single trench (c) and detail of the bottom corner of the cavity (d) confirming the very good filling [courtesy of M. Dalla Palma, LNL].

6.4.5 Preliminary functional characterization

As already mentioned, the preliminary functional characterization will be performed on bare devices (without converting material) at the University of Trento laboratory using radioactive sources and laser scans. Experimental results will also be compared to numerical simulations (where possible) to gain a better insight into the devices behavior. Neutron beam tests on devices coupled to the converting material will instead be performed at "Laboratori Nazionali di Legnaro (LNL)", Legnaro, Padova, Italy, using the same setup developed and characterized in Trento.

The readout setup is essentially composed by an integration chain (CSA+shaper) realized using Cremat components. The CSA is the CR-110, featuring a feedback capacitor of ~ 1.4 pF which is discharged by means of a 100 M Ω resistor. The shaping is performed with a CR-200 gaussian shaping amplifier featuring a peaking time of 4 μ s. It is important to notice that signals in response to different types of radiations are expected to have different components (both fast and slow) thus a slow peaking time is forecasted. In addition, since the leakage current is not excessively high, this is expected to provide better noise performances. The acquisition of the output spectrum is performed by means of a multichannel analyzer from Amptek (MCA8000A), using the ADMCA acquisition software (also provided by Amptek). Notice that other readout configuration are being investigate like different shaping amplifiers/MCA (e.g. Amptek's DP4). Since additional informations on the nature of the reaction products might be extracted from the shape of the output signal, another readout option will also be considered using a wide-band amplifier from Phillips Scientific (model 6954, one or more depending on the needed gain) that should amplify the signals without distorting their shape. The laser scans will be performed using the same setup described in Chapter 4 subsection 4.6.1. Because of the rather asymmetric geometrical configuration between the upper and lower surfaces, different informations can be extracted by performing both the radioactive source and laser scans from both surfaces.

Very preliminary results were obtained using the device indicated with "d=400, $\Delta p^+ = 100$ " in Fig.6.46 (the other two were already sent to LNL for the converter deposition). Using an ^{241}Am α -source (AMR01032, nominal activity ~ 3 kBq, active diameter ~ 2 cm 2 , main energy ~ 5.5 MeV) impinging the device from opposite sides of the sensor (one at the time), it was possible to acquire the first preliminary energy spectra. The source was placed roughly 10 mm away from the sensor surface, and an energy loss of roughly 2-2.5 MeV was expected for α -particles traveling that distance in air [208]. Fig.6.48 shows the results obtained for a bias voltage of 40 V, for particles impinging the sensor from the top (metal contact side) and from the bottom (trench side). In both cases, a peak is observed in the spectrum at roughly 3.5 MeV, compatible with the residual energy of particles traveling 10 mm in air. These particles are believed to hit the detector in the

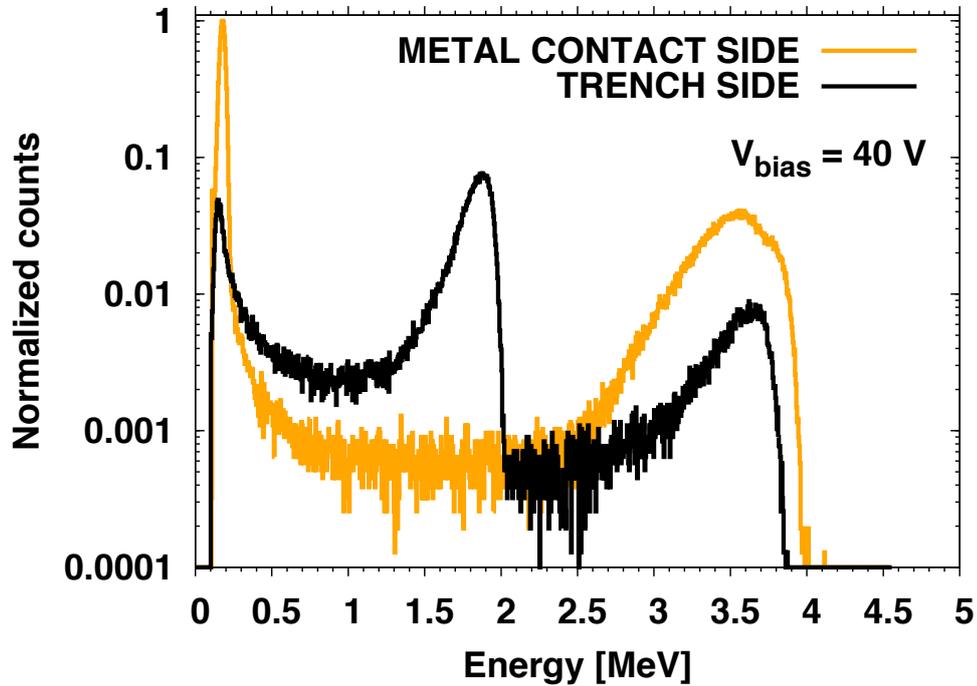


Figure 6.48: Spectra obtained from α -particles impinging the device from both sides for a fixed bias of 40 V.

regions where the electric field is higher, typically near the bottom corners of the trenches. Common to both measurements is also the very low peak situated at less 0.5 MeV: this peak is believed to be representative of the gamma component of the source spectrum, and further tests are being performed to confirm this hypothesis. The geometrical differences between the top and the bottom surfaces are clearly expressed by the peak situated at around 1.9 MeV, which is only present when particles impinge the device from the trench side. This peak is believed to be caused by particles impinging the device between two n^+ trenches, in a region where the field is rather low. Because of this, the charge collection becomes very slow and part of the event might be lost due to ballistic deficit. An additional effect that might play an important role in the formation of this lower energy peak, is an intrinsic property strictly related to this specific sensors configuration: it was already observed in single type column (STC) 3D strip detectors that, charge collected from one electrode can induce a signal of opposite polarity in the neighboring ones [209]. Since the investigated devices are readout in a "diode-like" mode, both the positive and the negative contributions are summed together resulting in a diminished amplitude of the output signal. This effect seems to be more relevant when full depletion between the trenches is reached and is currently being investigated by means of numerical simulations. It is important to note that this effect is not expected when particles hit the device from the

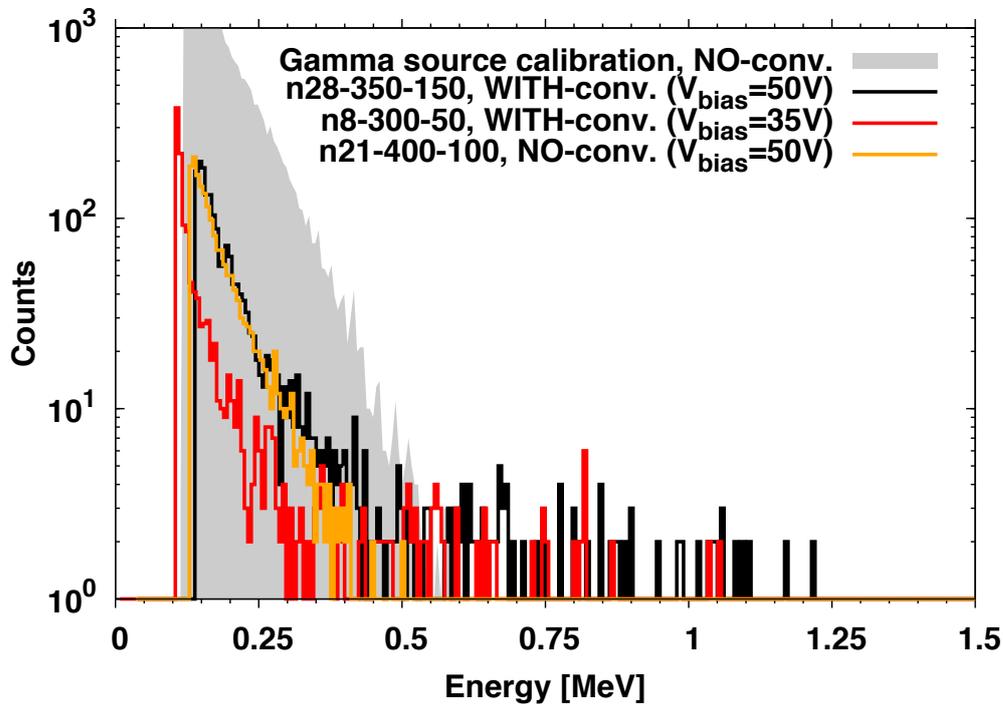


Figure 6.49: First preliminary results obtained with both bare silicon sensors and with devices coupled to the converting material in neutron beam test performed at LNL in January 2013.

metal side, because the range of α -particles in silicon is lower than $30 \mu\text{m}$ thus the charge will be generated in a higher field region. In addition, also β -particle and laser scans are being planned to have a clear understanding of the device behavior.

After confirming the correct operation of the bare silicon detectors and of the readout system, the first neutron beam tests were performed at "Laboratori Nazionali di Legnaro (LNL)" in January 2013. Neutrons were obtained from a proton beam hitting a lithium target. The readout system was placed downstream from the target and data were acquired both with and without the converting material inside the device trenches. Very preliminary results are reported in Fig.6.49. The first measurement performed was by means of a γ radioactive source, in order to verify that the system was performing as expected and to estimate how the forecasted γ background will influence the measurements performed with neutrons. The results of this first test are reported in Fig.6.49 in grey for a bare silicon sensor. In the same figure three different neutron measurement results are reported: in orange a measurement without the converting material confirms that the gamma background is compatible with the expectations and that no events are detected for energies higher than roughly 0.5 MeV. In black and red, the measurement obtained with the silicon devices coupled to the converting material show the presence of an increased amount

of counts in the region of the spectra between 0.5 and 1.25 MeV. This is to be attributed to the reaction products able to escape the converting material and to generate charge inside the silicon bulk. Due to the very short beam time available these measurements lasted only roughly one hour, thus it was not possible to accumulate additional statistics. Despite the low count rate, these results are encouraging and confirm that the investigated approach is feasible.

Building on the results so far obtained, greater understanding of the devices is being acquired with the help of numerical simulations and laser and source tests, in order to be fully prepared for an additional neutron beam test planned for mid March 2013.

Chapter 7

Conclusions and future plans

This work described the optimization of the 3D-DDTC sensor technology available at FBK in view of the ATLAS Insertable B-layer upgrade (IBL). Building on the experience gained with previous simplified technologies, it was decided to realize fully passing through columnar electrodes while maintaining a double-sided approach, thus limiting the process complication caused by the support wafer and assuring the accessibility of the backside of the sensor in order to ease the module assembly. The sensor layout was specifically designed with the IBL specifications in mind, in order to satisfy the required signal to noise ratio, the low power dissipation and the desired radiation hardness up to fluences in the order of $5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$.

Several batches of devices were fabricated at FBK between 2010 and 2012. The quality of the fabrication process was assessed by extracting the fundamental parameters from standard test structures and the basic aspects were found to be in good agreement with previous technologies. The electrical performances of 3D detectors were initially assessed by means of numerical simulations on 3D diodes. By properly reproducing the investigated devices in the simulation framework, the complete electrical properties of 3D sensors could be investigated, leading to a deep understanding of all the critical aspects. In particular, the most critical regions from the point of view of the breakdown voltage were found to be located near the sensor surfaces, where the highly doped p-spray layers are in contact with n^+ regions. It was also possible to demonstrate how different layout details, such as field-plates and/or floating-rings, could be successful in increasing the voltage handling capabilities of the investigated sensors.

The electrical characterization of fabricated 3D sensors were also performed on 3D diodes in pre irradiation conditions. The temperature dependence of both breakdown voltage and leakage currents were investigated for all available device geometries and were compared to theoretical expectations, finally demonstrating the proper operation of the considered sensors. In addition, the capacitance as a function of the reverse bias voltage

was studied. By comparing the performed measurements with incremental simulations, it was possible to understand how the different layout components affect the devices capacitance. The same study was also performed after heavy proton irradiation, up to IBL fluences. The theoretical dependence of currents, both with temperature and radiation fluence, was found to be in good agreement with measured values. Moreover, it was possible to demonstrate that, if the sensor behavior before irradiation is "intrinsic", the breakdown voltage after irradiation will reach values much larger than the estimated optimal operating condition.

Pixel detectors compatible with the FE-I4 readout chip were selected on wafer by means of current measurements using a temporary metal layer, in order to perform the bump-bonding only on good devices. Despite the large area of the FE-I4 pixel detectors, roughly $2 \times 2 \text{ cm}^2$, a large number of devices was found to be within the required IBL electrical specifications. The functional qualification of FBK technology was performed both in laboratory, by means of radioactive source scans, and in beam test at CERN SPS and DESY accelerators. The devices tracking efficiency was found to be higher than 98% in many different operating conditions and also after the maximum radiation fluences expected in IBL ($5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$). Due to the low operating voltages of 3D detectors (160 V in the worst IBL conditions), it was possible to demonstrate that the power dissipation of the investigated modules was lower than for standard planar devices.

The powerful simulation tools available also allowed to design a new edge termination, able to reduce the sensor dead area at the edge in the order of 100 to $200 \mu\text{m}$, without affecting the sensor operation and without causing premature reverse discharge. The signal efficiency of the edge region was confirmed with both laser and beam scans, and was found to be in very good agreement with numerical simulations.

All the IBL specifications and timings were respected and this finally led to the decision of installing 3D detectors in the forward regions of the IBL. Thanks to the large amount of testing performed during the IBL sensor qualification, 3D technology could be brought out of the R&D phase, proving to be a reliable and very radiation hard silicon detector technology for particle tracking in the future generations of experiments at sLHC.

The extensive simulation and measurement campaigns performed during the technology qualification for the IBL, led to the design of a new and improved batch of 3D detectors to be fabricated at FBK. The sensor layout was modified mostly relying on numerical simulations and results from the previous sensor batches. An additional reduction of the edge dead area was also performed thanks to the obtained simulation results and measurement results. New devices were fabricated at FBK and, despite major problems during fabrication, it was possible to partially demonstrate that numerical simulations were able to predict all the desired sensor improvements, leading to enhanced voltage

handling capabilities.

The great efforts made in the development of 3D technology for particle physics applications also translated into new ideas for the application of 3D sensors both in tracking applications and in other fields, such as the detection of neutrons, with very promising results.

The electrical and functional characterization of the fabricated devices is currently being completed and much higher irradiation fluences are also being investigated in view of the future LHC upgrades. In parallel, all the new ideas are being implemented, ranging from edge region reduction, passing through the mastering of avalanche multiplication and reaching the realization of hybrid neutron detectors.

A continuous development of 3D technology is planned at University of Trento and FBK. The clean room is currently being upgraded to handle six inches wafers. The 3D process will then be re-calibrated and the production will be restarted, possibly gaining additional advantages from the newly upgraded machines.

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