

Figure 8.2: Schematic overview of the Coincidence Chip (CC).

8.2 Implementation

8.2.1 The Coincidence Chip (CC)

The Coincidence Chip provides on-detector coincidences to reduce the trigger data sent to the counting room. It is used by the RP and T2 systems, but not by T1 where the more complex geometry made its use too difficult. Figure 8.2 shows a block diagram. The chip has 80 LVDS inputs which can be grouped in two ways:

- 16 groups of 5 inputs, for 5 detector planes (RP case).
- 8 groups of 10 inputs, for 10 detector planes (T2 case).

These groups correspond to detector sectors in a similar transverse position on different detector planes.

A synchronisation block is included to synchronise the pulses to the clock and to stretch the pulses over different clock cycles for detectors with an inherent timing spread larger than a single clock cycle. Asynchronous operation is also possible. For TOTEM only synchronised operation has been adopted.

Two types of coincidences can be performed:

- A coincidence on just one group: V hits on one track road through NP detector planes.
- A coincidence which takes into account a programmable number of neighbouring groups: W hits out of NP detector planes including X neighbouring groups.

The result of these coincidences can be logically combined in a programmable way (AND/OR with possible inversion). The possibility to include neighbouring sectors or not allows a certain programmable selectivity on the direction of incoming particles.

The total number of positive coincidence results is checked (Z out of 8 or 16) and can be logically combined with the coincidence results (AND/OR2). This can be used to impose certain occupancy limits, for instance to prevent the generation of a trigger if a detector is completely filled with artificial hits, e.g. due to noise or particle showers. Finally, signals can be grouped into a smaller number (OR2) to reduce overall signal count.

The parameters of the blocks on the Coincidence Chip can be fully configured through its I²C interface. The VFAT chip also includes counters on the fast trigger outputs to monitor hit rates. This is achieved by a 24 bit counter which records the number of sector hits within a given time window. The duration of the time window can be selected from a list of 4 possible options (6.4 μ s, 1.6 ms, 0.4 s, 107 s).

8.2.2 Trigger bit transmission to the counting-room

The trigger signals from all subdetectors are optically transmitted to the counting-room using the GOH optohybrid in the same way as the tracking data. However, the Roman Pot station RP220 is so far away from the counting-room that optically transmitted trigger data would not arrive within the latency allowed by the trigger of CMS. Therefore, in addition to optical transmission for TOTEM runs, electrical transmission with LVDS signals was implemented for commons runs with CMS. To maintain the electrical isolation between detector and counting room, optocouplers will be used to receive these electrically transmitted signals. At regular intervals of about 70 m along the total cable length of 270 m, repeaters based on a custom-designed LVDS repeater chip are inserted to preserve the electrical signal quality.

8.2.3 Trigger signal synchronisation

The large distances between the subdetectors — with RPs at up to 220 m from the interaction point — requires special attention to the synchronisation of the trigger information.

Since the trigger output from the RP220 station has the longest signal transmission time, the trigger signals from that station are the last to arrive in the counting-room. In order to minimise the latency of the combined trigger, the data from the trigger FEDs of the other subdetectors are transmitted via the VME back-plane to the trigger FED of the RP220 station where all the trigger information is merged. Thus the RP220 trigger FED acts as the master of the TOTEM trigger system, generating the global TOTEM L1 trigger decision and is also capable of sending 16 trigger bits to the CMS global trigger system [60] for common data taking with CMS in the future.

The synchronisation of the trigger generating bits is based on the BC0 signal (Beam Crossing Zero). This signal — related to the first bunch of a LHC beam revolution cycle — is issued every 3564 bunch crossings and broadcast by the TTC system. On the detector side, it is received via the control token ring and decoded by a VFAT Trigger Mezzanine (VTM) as shown in figure 7.7. It is then superimposed onto the trigger data stream transmitted to the counting-room. The trigger FEDs also receive the TTC signal including the BC0 signal. The trigger generating bits are then temporally aligned to the BCO signal. This scheme is also used for the 16 trigger bits sent to the CMS global trigger system.

Care also has to be taken in the synchronisation with respect to the transmission of the TOTEM first level trigger signal down to the “Local” and “On Detector” regions.

The level-1 trigger is transmitted to the detectors using the TTC system and the FEC card. The FEC card can adjust the phase of the fast commands and the clock. The latency of the VFAT can be adjusted to account for the differences in delay due to the spatial spread of the subdetectors and obtain synchronisation.

Chapter 9

DAQ

9.1 Requirements

The Data Acquisition of the TOTEM experiment will perform different tasks depending on the running conditions:

- Initialisation and calibration of the front-end hardware
- TOTEM stand-alone data taking at a rate ≈ 1 kHz;
- Data and Trigger quality monitoring;
- Data taking integrated in the CMS DAQ/Trigger system at a later stage.

9.1.1 Trigger and data rates

We consider that the upper limit of the total event size is ≈ 50 kB. This data size is fixed since no zero-suppression is applied to the data. This choice greatly simplifies the task of evaluating the data rates and the resources needed to cope with them.

The data rate is easily computed as $50 \text{ kB/event} \cdot \text{TriggerRate} = 50 \text{ MB/s} \cdot (\text{TriggerRate}/\text{kHz})$. We consider here that the standard trigger rate is 1 kHz, with an upper limit (on redundant resources) of 2 to 3 kHz.

Two operational conditions can be envisaged:

- **Calibration and Setup.** The VFAT chips and related front-devices need to be initialised and calibrated before a normal run can start. The parameter space of the VFAT chip is particularly large, and its calibration procedure delicate; many different parameters need to be scanned in order to compute the optimal setting in terms of threshold and latency adjustments, taking into account the specific properties of each detector in terms of signal shape and timing. In these operating conditions the rates are typically much lower than in standard running mode, the limiting factor being the time needed to re-configure all the VFAT chips at every step of the parameter scan. We assume that a typical trigger rate in this running mode will be ≈ 100 Hz, corresponding to ≈ 5 MB/s

- Once the system is properly calibrated and initialized with the computed parameters, the standard running mode can be started, and the data rate will solely be tuned by the trigger rate.

In both cases the data produced by the VFATs will flow through an infrastructure based on VME [56] and/or USB-2 (Universal Serial Bus) [61] links, independently from the one of the CMS experiment.

Irrespectively of the running mode (*standalone* or *CMS*) this *local DAQ* will always be used for setup and calibration.

9.1.2 CMS compatibility

In the special *CMS compatible* running mode, the raw data will flow through the CMS standard S-Link64 [58] lines, FRL boards and Myrinet infrastructure. The TOTEM FED boards (section 7.2.2) have been designed (as described in the relevant sections) to respect the CMS standard data format and control protocols when connected to the main CMS DAQ.

In this running mode, the *local* readout infrastructure will act as a parallel path, used for front-end initialization during the start-of-run procedures, and for data quality monitoring.

The TOTEM DAQ software is based on the same building blocks as the one of CMS. This will simplify the task of operating the TOTEM Run Control (and its end- and start-of-run procedures) system within the CMS one.

9.2 Implementation: readout chain and infrastructure

9.2.1 Readout link options

The TOTEM FED boards offer a large range of readout options.

- VME: We assume that the aggregated maximum data rate per VME crate is ≈ 40 MB/s. Readout load splitting over > 1 VME crates is possible.
VME is the standard communication link for hardware initialization. We decided to use a minimum 3 crates dedicated to readout FEDs to ease standalone operations of the 3 detectors during setting-up periods. One additional crate hosts the trigger FEDs. In these conditions, the minimal requirement of 1 kHz trigger is already largely satisfied.
- USB-2: Every FED carries 3 USB-2 links. If we assume the USB-2 standard to be capable of 10 MB/s, the maximum aggregated data rate over the 20 available raw-data links amounts to 200 MB/s, corresponding to a theoretical 4 to 5 kHz trigger rate. These numbers are challenging (although not impossible) at several levels of the DAQ system, from data transmission over the Ethernet network, to stress (and cost) of the storage system, to data mirroring in the Central Data Recording facilities. Full exploitation of these capabilities is out of the scope of the present activities, and therefore not foreseen for the moment. Suffice here to say that the TOTEM DAQ has abundant spare resources to accomodate the foreseen trigger rates.

- S-Link: This can be considered either an electrical connection to a front-end PC (useful for laboratory testing) or the entry point into the main CMS DAQ data transport via FRL boards and the Myrinet infrastructure. It is the default option for the integration of TOTEM into the CMS DAQ and Trigger system.

9.2.2 PC cluster and local data storage

The TOTEM DAQ cluster will consist of a set of a few PCs (presently 5) for raw data readout over VME (or optionally USB), and a set of event-building and storage nodes sized to the needed storage rate and capacity.

The minimum requirements for data storage is the ability to write data at the trigger rate of 1 to 2 kHz and the capacity to store data during one full day even in case of failure of data transfer to a central data recording system.

At the rate of 2 kHz, TOTEM will produce ≈ 360 GB / h, corresponding to ≈ 8.6 TB of data per day of running. These capacities and rates can be easily accommodated in present medium-level storage systems based on Fiber-Channel [62] or iSCSI [63] technology. To ensure that the required rate is attained and to provide redundancy, the data load will be shared between ≥ 2 storage systems.

Chapter 10

Detector Control System

10.1 Objectives

The Detector Control Systems (DCS) for LHC experiments are the evolution of slow control systems of the LEP era. Their aim is to permit the physicist on shift to operate and control various detector subsystems such as high and low voltage power supplies, gas circulation systems, cooling and so on, and monitor their performance as well as various relevant environmental parameters, for example temperature and radiation levels. All DCS systems of LHC experiments are built using the industrial PVSS control supervisory software running on networks of PCs (Windows and/or Linux), augmented with modules developed at CERN for typical HEP control functions and equipment, the JCOP framework. “Big.brother”, the TOTEM DCS system, also uses the same guidelines, technology, tools and components.

10.2 Constraints

The TOTEM detector is located at the CMS intersection of the CERN LHC accelerator, and CMS and TOTEM also have a common physics program, so that TOTEM must be able to operate independently, but also take data together with CMS. For this reason TOTEM adopted a number of technological and organisational solutions that will permit interoperability at the level of electronics, DAQ, run control, offline data processing and so on. In the same fashion, the TOTEM detector control system is developed in the framework of the CMS DCS. This implies following the CMS DCS integration rules [64], liaising with CMS central controls, through participation in the CMS DCS coordination board, and adopting the same model of rack-mounted PCs.

10.3 Equipment under control

The three TOTEM subdetectors, Roman Pot silicon detectors, T1 and T2, require the monitoring and control of the usual equipment found around particle physics experiments. All three use CAEN HV power supplies, Wiener Maraton LV units, Wiener VME crates, and environmental sensors connected to ELMBs or read from the DAQ through the DCU technology. T1 and T2 are cooled with cold water loops derived from CMS rack cooling, while the Roman Pot Si detectors use a

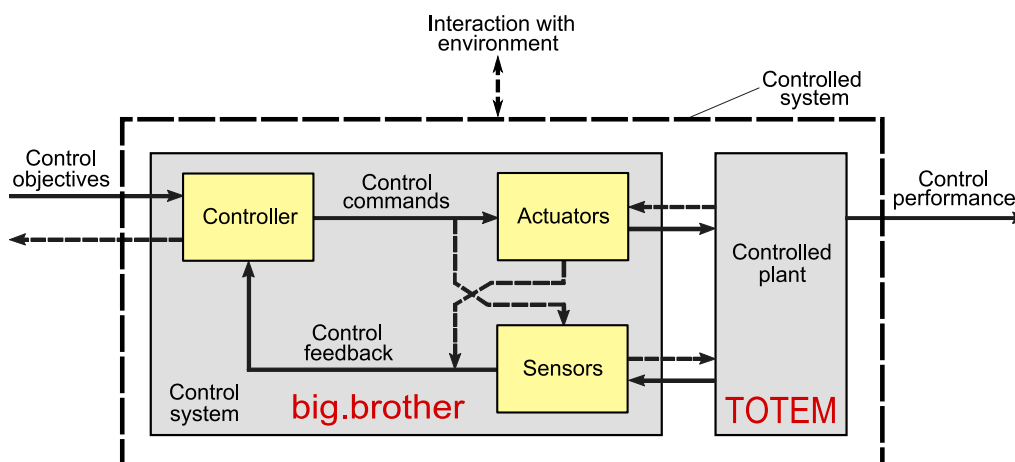


Figure 10.1: Generic control structure (adapted from [67], figure 1).

more sophisticated cooling plant. The T1 and T2 gas systems are subcontracted, including a PC running PVSS control software compliant with the GCS standard LHC gas control system [65].

The Roman Pot motor system is derived from the one of the LHC collimators, and so is the corresponding control system [66]. The front-end is based on National Instruments hardware and the Labview RealTime software, adapted to the selected sensors, and is subcontracted to PH/DT1. The high level control is also subcontracted, being derived from the Collimator Supervisory System, is integrated with the Central Collimation Application in the main control room, and sends status data and other relevant information to big.brother.

10.4 Engineering

Dealing with control, the system conforms to the standard control model of sensors, actuators and controllers depicted in figure 10.1.

The system consists of HW and SW components, therefore it requires comprehensive system engineering. As with any control system, the development process of big.brother is iterative vertically between system engineering and lower assembly engineering, and iterative horizontally between requirements engineering, design-configuration, verification-validation, and analysis (figure 10.2).

A number of HW and SW technologies have been defined already before the project started: sensors, front-end systems, the supervisory level based on PVSS and the JCOP Framework, the model of the PCs and their operating system.

The CMS DCS development model is federal, with independent subdetectors following their own engineering and project organisation, so far that as they use the agreed technology and obey the mandatory integration rules, dealing also with the definition and nesting of Finite States Machines (FSM) describing the state of the system. The situation is very different in ALICE, where the development model is centralised, and a number of engineering representations and software components have been developed centrally to be used by all subdetectors [68]. Big.brother has

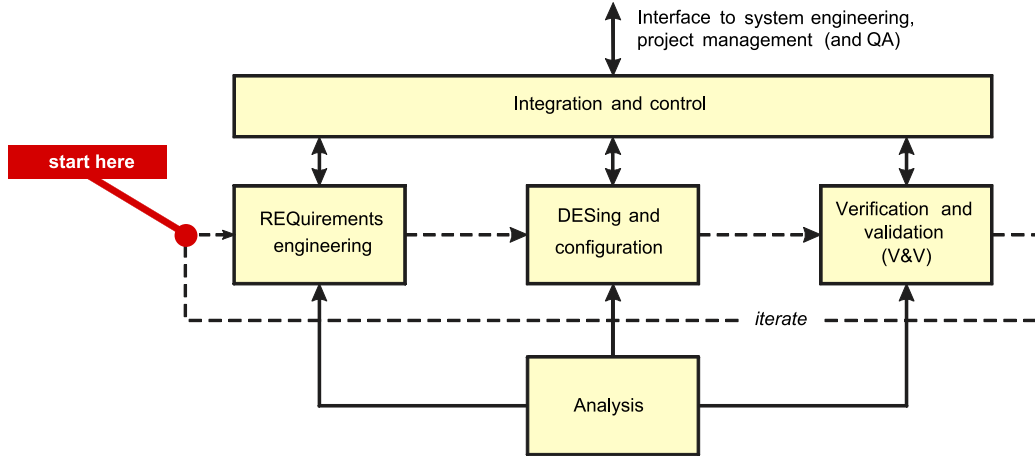


Figure 10.2: Horizontal development iteration.

adopted from ALICE DCS the requirements template, the format of the HW overview diagrams, and is considering to use some of the existing components, also for the user interface which is standardised across the three TOTEM subdetectors.

10.5 The Radiation Monitoring system — an example of environmental monitoring

The Roman Pot silicon detectors, T1 and T2 together with their related readout electronics, are located in LHC areas where high radiation levels are expected (see for example figure 5.1 and ref. [69]). For this reason, the Total Ionising Dose (TID) and the 1-MeV neutron equivalent particle fluence (Φ_{eq}) will be monitored during operation in various locations of the TOTEM experiment, and they will be available on-line in the TOTEM DCS [70].

Measurements of TID and Φ_{eq} are needed to understand the radiation-induced changes on the detector performances, to survey the radiation damage on electronic components, to verify the TOTEM radiation field simulated with Monte Carlo codes and to survey anomalous increases of radiation levels that may arise from accidental radiation burst such as beam losses or unstable beams. This set of information can finally be used to better plan the detector operation scenario.

The basic unit of the TOTEM Radiation Monitoring (RADMON) system is the Integrated Sensor Carrier (ISC) that hosts radiation sensors connected to the electronics via readout cables. TID measurements are performed with different types of Radiation-sensing Field Effect Transistors (RadFETs), while Φ_{eq} measurements are performed with forward biased *p-i-n* diodes [71]. In both cases the dosimetric parameter (voltage) is measured upon constant current injection through the sensors. Selection of sensors, assembly of the ISC, as well as calibration constants are provided by the TS-LEA and PH-DT2 groups at CERN [72]. In the case of TOTEM each ISC will host four radiation sensors and a temperature probe, leading to a total of five channels to be read out per monitoring location.

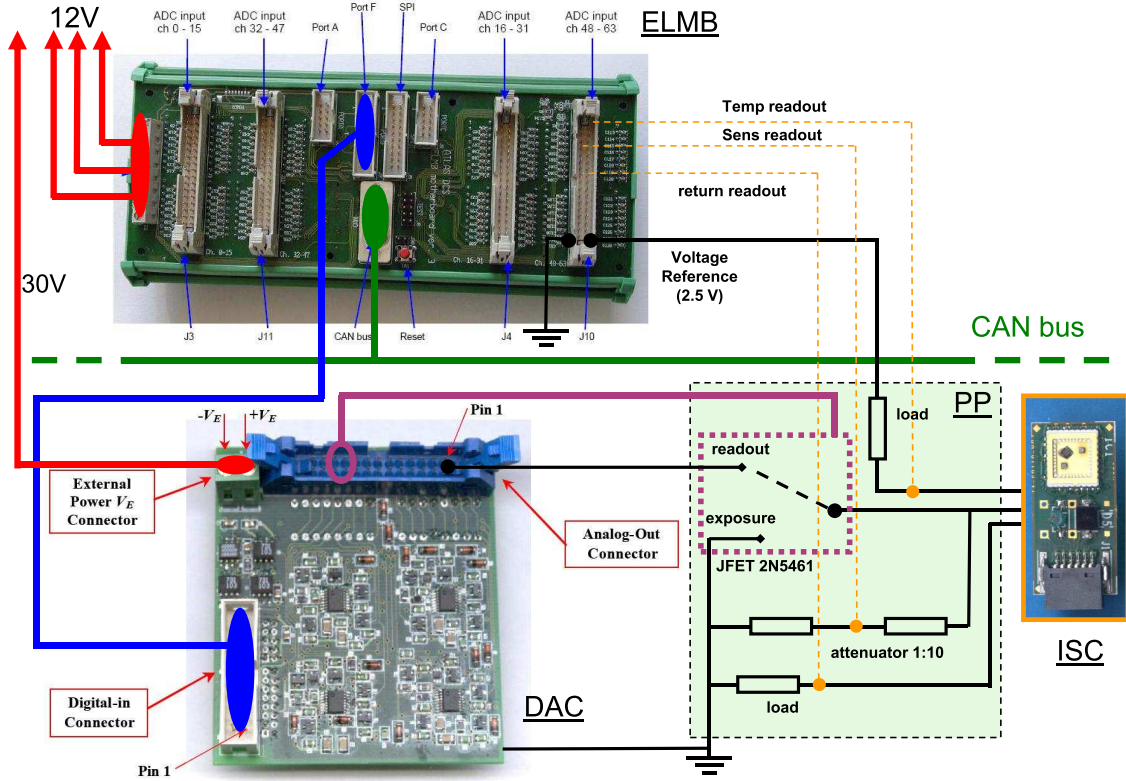


Figure 10.3: Schematic of the ELMB RADMON readout system used in TOTEM and based on the standard ATLAS electronics. This example of readout is referred to one ISC hosting 1 RADMON sensor and 1 temperature probe. On the right-hand side of the picture the ISC is visible. The readout current injected through each sensor is also monitored by measuring the voltage drop on a small resistor placed on the return line.

The design of the RADMON readout electronics in TOTEM follows the one developed by the ATLAS experiment where the sensor readout is based on Embedded Local Monitor Boards (ELMBs) [73]. As shown in figure 10.3, the readout of the ISC is based on an ELMB board, which communicate over the CAN bus with a PC running SCADA software (PVSSII) that is linked to the DCS. To drive currents through the sensors on the ISC during the readout sequence, ELMB-DAC boards are needed. The 16 channel, 12-bit DAC-module connects directly to the digital output of the ELMB motherboard. The ELMB and the ELMB-DAC finally interface with the ISC via patch panel (PP) boards. The PP host a series of JFET switches to short the sensor terminals to ground during radiation exposure and enable them for the readout. On the PP, voltage attenuators and loads to monitor the readout current sent to the radiation sensors are also present. One full readout chain consisting of 1 ELMB, 2 ELMB-DAC and 2 PP boards allows the readout of 6 ISCs in the TOTEM configuration. A total of 36 ISCs will be installed in the TOTEM experiment: one ISC will be integrated on each of the 24 RP motherboards, while 8 ISCs will be installed around T1 and 4 around T2 respectively.