

Chapter 7

The TOTEM electronics system

TOTEM has 3 separate and distinct detector technologies used within the three detector systems; RP, T1 and T2. Each detector system has its own physically separate electronics system however each system is made following one common system architecture. This has the obvious benefits of reducing design effort by using common electronic components, data formats and DAQ software.

The initial requirements for the electronics system are to be able to readout the charge of the three different detectors on one side and offer full compatibility with CMS on the other.

Table 7.1 gives an overview of the three detectors with their main properties and the number of front-end chips (VFAT) needed. The gas detectors generate more signal charge, distributed over several electrodes. The silicon strips generate positive charge, T2 negative, and T1 both polarities (anodes and cathodes). The T1 and T2 detectors have a large occupancy particularly in the regions close to the beam pipe. This is due to inelastic events with a large number of particles interacting in the beam pipe and thus creating particle showers at the detector edges.

The signal properties vary considerably between detectors. However, it was decided at an early stage to design one common front-end ASIC that would be capable to provide the charge readout for all detectors. This front-end ASIC is called VFAT and is key to providing a common data format and common control and readout needs in the electronic system for all 3 detectors.

Table 7.1: Overview of electronics requirements from the different detectors.

	RP	T1	T2
No. and type of detectors	240 Si strip detectors	60 Cathode Strip Chambers	40 Gas Electron Multipliers
No. of channels	122880	11124 anodes 15936 cathodes	62400 pads 20480 strips
No. of VFATs	960	480	680
Typical input charge	~ 4 fC	~ 50 fC	~ 50 fC
Occupancy	$< 1\%$	anodes: $< 10\%$ cathodes: $< 20\%$	pads: $< 5\%$ strips: $< 30\%$
Radiation Dose	< 10 Mrad	< 50 krad	< 50 Mrad

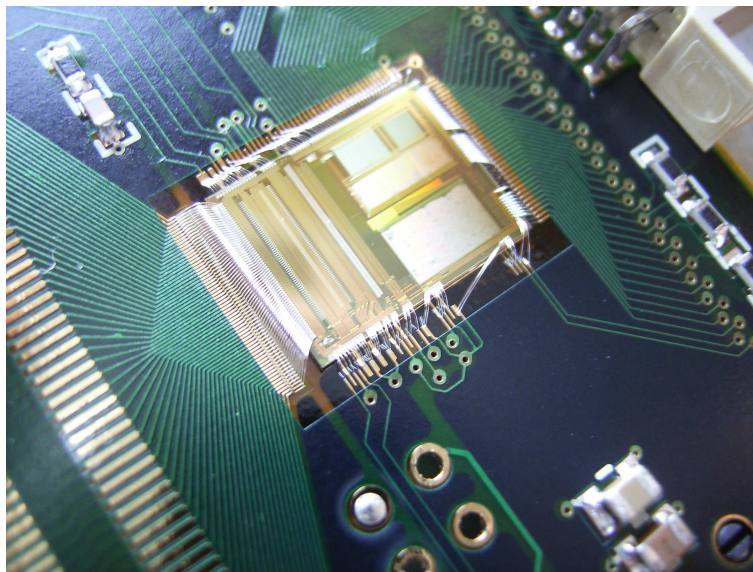


Figure 7.1: Photograph of the VFAT chip.

7.1 VFAT

The VFAT [52] (strictly “VFAT2”, being the second version) is a trigger and tracking front-end ASIC, designed specifically for the readout of sensors in the TOTEM experiment at the LHC. The VFAT chip (shown in figure 7.1) has been designed in quarter micron CMOS technology and measures 9.43 mm by 7.58 mm.

It has two main functions; the first (Tracking) is to provide precise spatial hit information for a given triggered event. The second function (Trigger) is to provide programmable “fast OR” information based on the region of the sensor hit. This can be used for the creation of a level-1 trigger.

Figure 7.2 shows the block diagram for the signal path through the VFAT. It has 128 analog input channels each of which are equipped with a very low noise pre-amplifier and a 22 ns shaping stage plus comparator. A calibration unit allows delivery of controlled test pulses to any channel for calibration purposes. Signal discrimination on a programmable threshold provides binary hit information which passes through a synchronisation and monostable stage before being stored within SRAMs until a trigger is received. The monostable has a variable length from 1 to 8 clock periods. This has the effect of recording the hit in more than one clock period (useful for gas detectors which have an uncertainty on the signal charge rise time). The SRAM storage capacity enables trigger latencies of up to $6.4 \mu\text{s}$ and the simultaneous storage of data for up to 128 triggered events. Dead time free operation with up to 100 kHz Poisson distributed trigger rates is ensured. Time and event tags are added to the triggered data which are then formatted and read from the chip in the form of digitized data packets at 40 Mbps. The data packet format is defined as in figure 7.3.

VFAT has many programmable functions controlled through an I²C interface. These include: internal biasing of analog blocks via 8 bit DACs, individual channel calibration via an internal test pulse with 8 bit programmable amplitude, calibration test pulse phase control, operate with positive

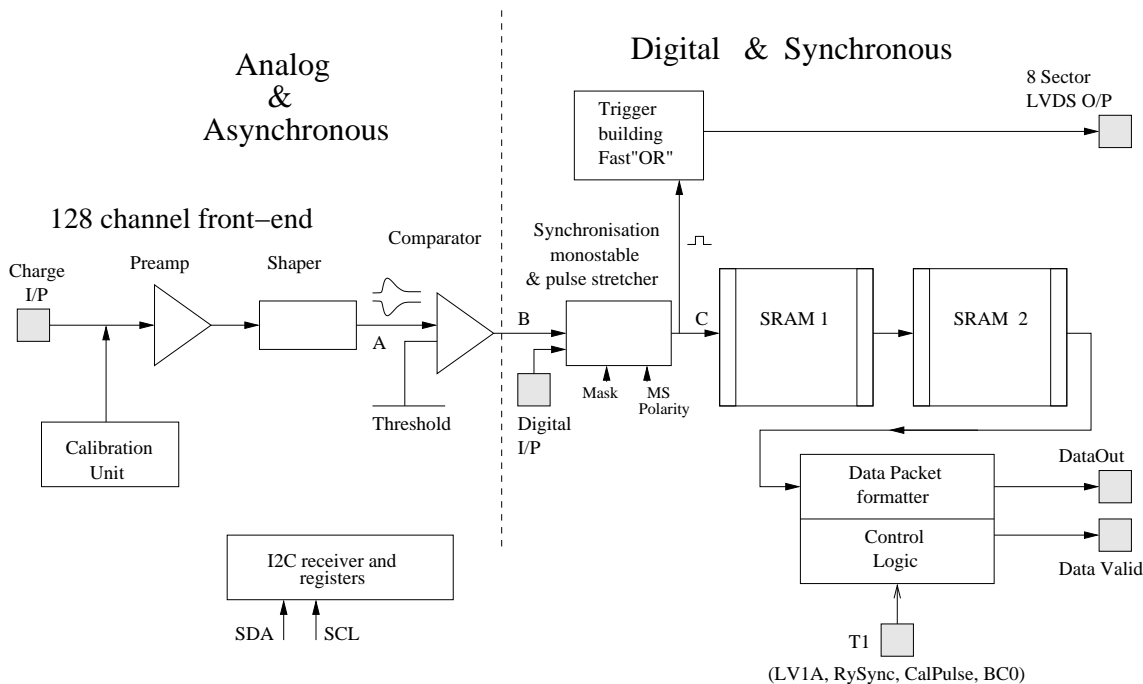


Figure 7.2: Block diagram of the signal path through the VFAT.

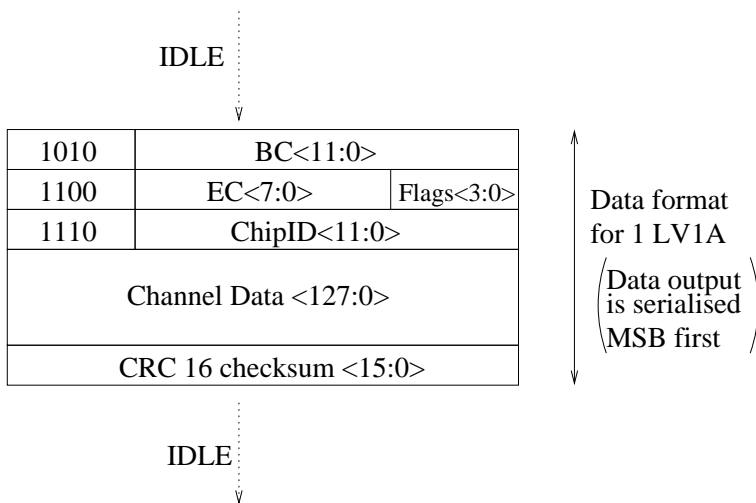


Figure 7.3: VFAT data packet format.

or negative detector charge, 8 bit global threshold plus a 5 bit trim DAC threshold adjust on each channel, multiple possibilities for channel grouping for the “Fast OR” outputs, variable latency, various test modes plus an automatic self test of the digital memories. Chip status information including occupancy and SEU rates can be read via I²C.

Fast synchronous commands are applied via an encoded LVDS signal (T1) which is then decoded to 4 synchronous commands via an internal command decoder.

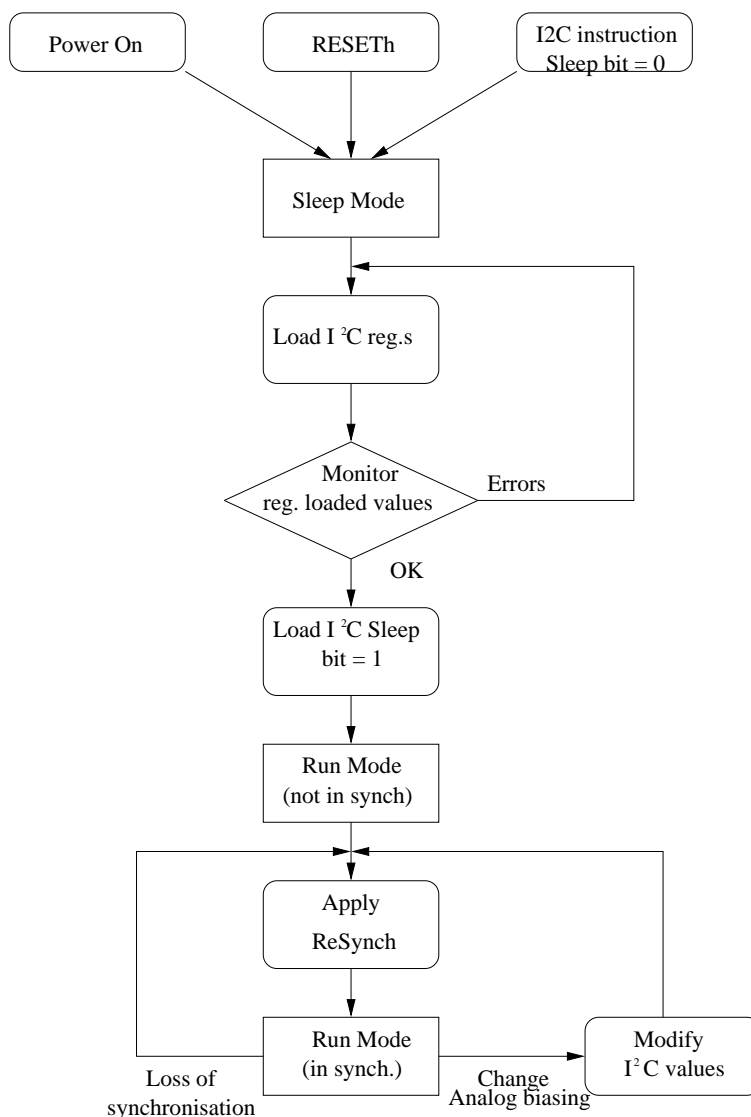


Figure 7.4: Flowchart of the operation cycle of VFAT.

For robustness against single event upsets (SEU), the digital parts of VFAT have been designed with hamming encoding for the SRAMs and triplication logic for the I²C interface and control logic. All analog circuitry employs layout techniques that reduce threshold voltage shifts under ionising radiation.

The operation flow of VFAT is shown in the flowchart of figure 7.4. On applying power to the chip VFAT performs an automatic power-on reset and goes directly into “Sleep Mode”. Sleep Mode sets all DACs to default values providing stable but minimum power consuming conditions to the entire chip. In Sleep Mode only the I²C is active and can respond to commands. The internal registers can then be loaded with data. This data can be read back to check if loading was successful. The values loaded are not applied to the active circuits until VFAT is put into Run Mode. When VFAT is put into Run Mode, biases are applied to the analog circuits and digital circuits come out of a reset condition bringing the power consumption up to the normal level. Since

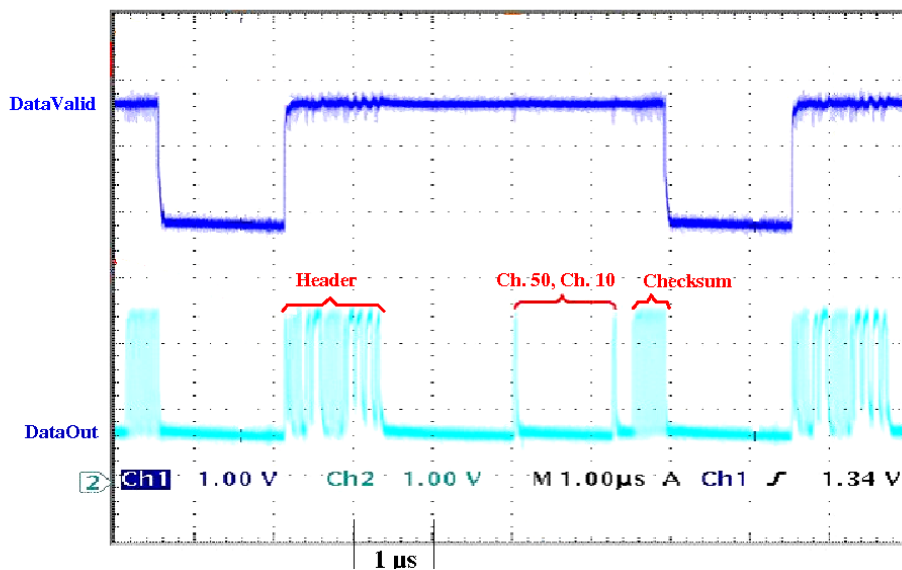


Figure 7.5: Oscilloscope view of the data packet and DataValid signal.

the I²C is a non-synchronous slow command VFAT still requires a synchronising signal. This is applied via a ReSync signal encoded within the T1 signal. VFAT is now in a synchronous Run mode and ready for taking data. Initial functional measurements showed all functions of VFAT to be fully operational.

Measurements of the Calibration units internal test pulse generator reveal a linear charge delivery range of -2 fC to 18.5 fC with LSB of 0.08 fC.

When triggered, Data packets appear on the DataOut output as shown in figure 7.5 together with a DataValid signal which goes high for the duration of a Data Packet. The figure shows two “hit” channels, these channels received a charge pulse from the Calibration unit.

Noise measurements have been made by choosing a random threshold and then ramping the magnitude of the signal charge using the internal test pulse generator controlled via DAC (digital-to-analog converter). The range is chosen such that the test pulse amplitude V_{Cal} passes through the threshold from 0% hits to 100%. The result is an S-curve as shown in figure 7.6. The mean of an error function fit to the S-curve gives the threshold and the sigma gives the noise expressed in ENC (Equivalent Noise Charge).

S-curves have been generated for all channels. The second and third plots of figure 7.6 show histograms of the extracted thresholds and noise of 128 channels. The results show for a mean threshold of 5952 electrons there is a threshold spread (before fine adjustment with the Trim DACs) of 335 electrons rms. The mean ENC is 539 electrons with a spread of 67 electrons rms.

A major design challenge was to integrate the multitude of digital functions without having a significant impact on the analog performance. Stringent design techniques to “deafen the listener” and “silence the talker” have been employed to all analog and digital modules.

Measurements from the chip show all modules to be 100 percent functionally correct. The expected front-end noise performance of approximately $600 e + 50 e/pF$ of detector capacitance is maintained. The total power consumption is 572 mW.

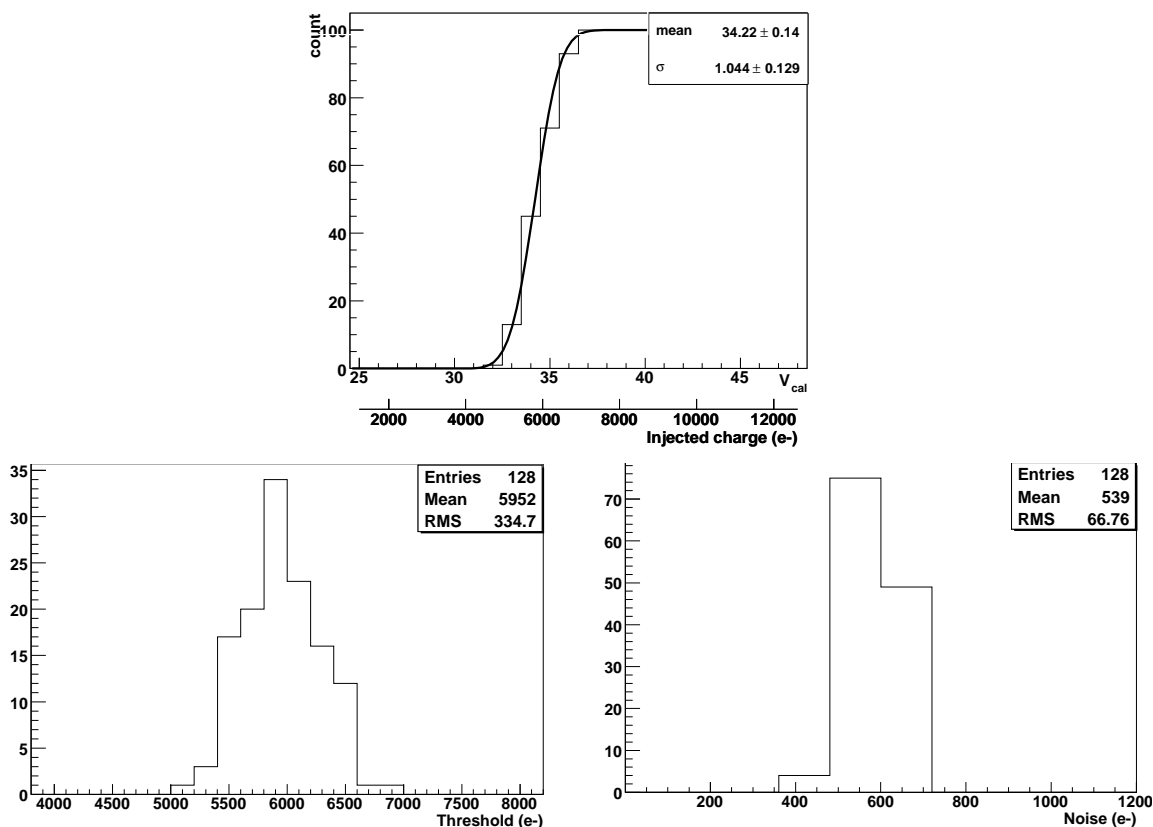


Figure 7.6: Top: S-curve (number of hits as a function of the test pulse amplitude for a fixed threshold) for one VFAT channel with a Gaussian error function fit superimposed. Bottom left: distribution of the mean thresholds (V_{cal} at 50% level of the Gaussian error function) of all 128 VFAT channels. Bottom right: distribution of the noise, i.e. the width of the fitted Gaussian error function, for all 128 channels.

VFAT has successfully integrated complex analog and digital functions into a single ASIC without compromising noise performance.

7.2 The TOTEM electronics control and readout system

The architecture of the TOTEM control and readout system is common to all 3 detector systems. This section describes the common electronics architecture and the components used.

Figure 7.7 shows a basic block diagram of the functional components used in the system. It is sub divided into physically separated regions and also data flow. The “On Detector regions” have the VFAT front-end ASIC located as close to the detector as physically possible. The “Local Detector regions” are for readout boards in the vicinity of the detector used for grouping and distributing control signals.

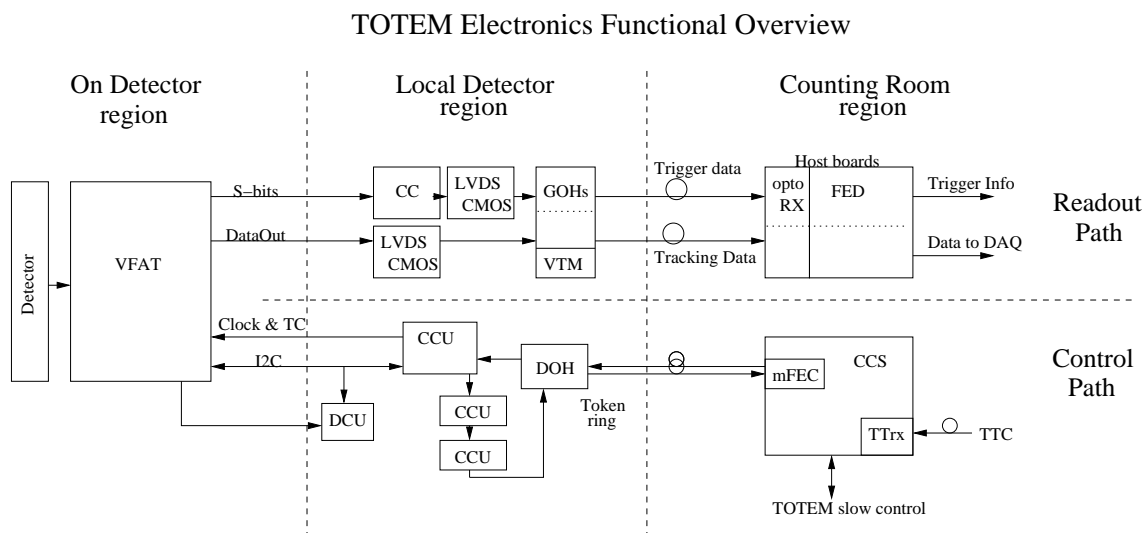


Figure 7.7: Functional block diagram of the TOTEM electronics system architecture.

7.2.1 The VFAT control path

The VFAT control path starts in the counting room with the arrival of Timing, Trigger and Control (TTC) signals [53] to the TTC receiver (TTCrx) on the Clock and Control System (CCS). The TTC signals are composed of the LHC machine clock and trigger commands (TC).

The CCS is equipped with Front End Controller (FEC) modules. TOTEM slow control instructions and TTC signals are transmitted onto a token ring via the FEC modules. The token ring starts with 40 Mb/s optical links from the FECs to the subsystems in the local detector regions. The optical signals of the token ring are converted to electrical signals in the local detector regions by a module known as the Digital Opto Hybrid Module (DOHM [54]). Communication and Control Units (CCU) sit in the token ring and are used to extract and distribute fast clock/TC signals and slow control information to and from the VFATs. The fast clock/TC signals are delivered to the VFATs via Low Voltage Differential Signals (LVDS). Slow control is achieved using the I²C protocol to be able to provide write/read access to registers inside the VFATs. The Detector Control Unit (DCU) contains analog to digital converters (ADCs) which are used to measure currents and voltages within VFAT and read back these values via I²C. The DCU is used during calibration of the VFATs.

The concept of the token ring and the design of the token ring ASICs ie. FEC, CCU, DCU plus associated PLLs [39] were designed by the CERN microelectronics group for use within CMS. The CMS tracker and Preshower use this concept for their control systems.

7.2.2 The VFAT readout path

VFAT produces both trigger and tracking data. These two types of data have very different timing requirements hence are treated separately.

Trigger data is used to aid the generation of the first level trigger hence has to be read out as fast as possible. The Sector outputs (S-bits) of the VFAT give the result of internal fast OR

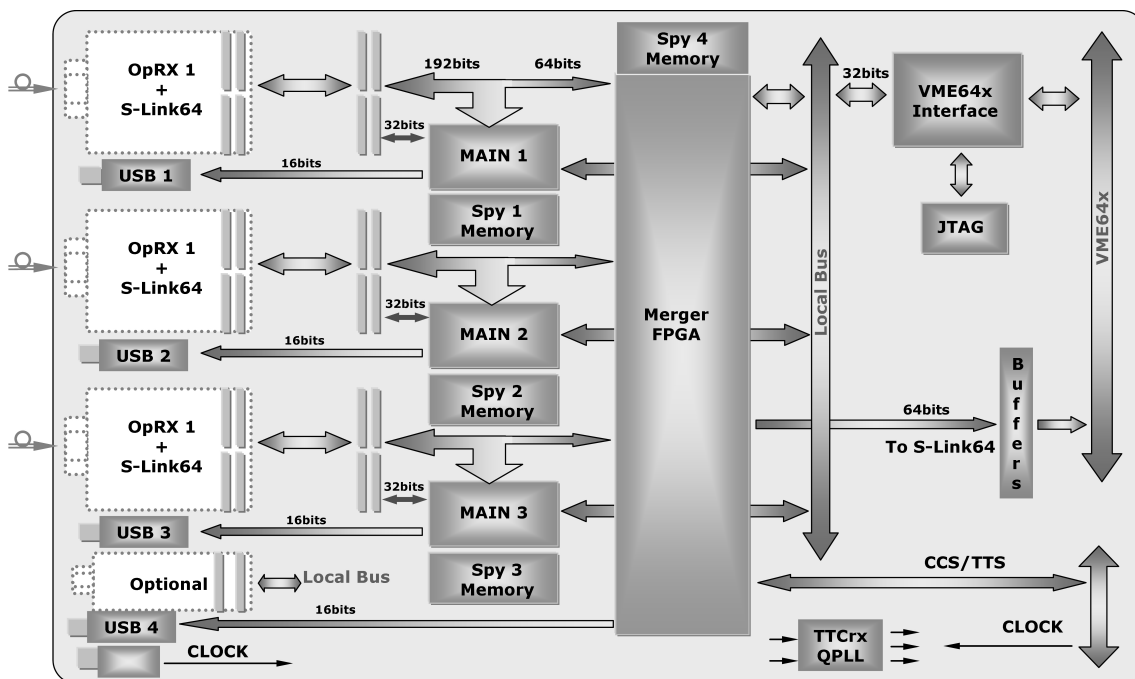


Figure 7.8: Block diagram of the TOTEM FED Host board.

operations within 1 clock cycle. These S-bits are in LVDS format. A Coincidence chip (CC, see section 8.2.1) then performs coincidence operations between VFAT sector outputs. The outputs from the CC chip (still in LVDS format) are then converted to CMOS levels by dedicated LVDS-to-CMOS converters. The trigger data are then serialised and transmitted by optical links at 800 Mb/s to the counting room. The module that performs the serialisation and optical transmission is called the Gigabit Optical Hybrid (GOH [34]).

Tracking data are data corresponding to triggered events and are buffered within VFAT for high trigger rates. Data packets are transmitted in serial LVDS form from the VFAT DataOut outputs at a bit rate of 40 Mb/s. Once again the LVDS to CMOS conversion is performed and the GOH serialises the data for transmission to the counting room via optical links. Up to 16 VFAT DataOut signals are multiplexed by one GOH into a serial stream for optical transmission. All VFATs operate synchronously, a VFAT Trigger Mezzanine (VTM) is used to control the timing of the GOH and maintain synchronisation.

Once in the counting room the optical fibres are connected to the 9U VME64x Host boards (developed by TOTEM) which contain the Front-End Drivers (FEDs [55]) used for trigger and event building. There are separate Host boards for the treatment of trigger data and tracking data. TOTEM uses 6 Host boards for the Trigger system and 8 Host Boards for the tracking data. A block diagram and photograph of the Host Board are shown in figures 7.8 and 7.9 respectively.

The incoming optical fibres (grouped in 3 bundles of 12 fibres) connect to optical receiver modules called optoRx-12. The OptoRx-12 is a plug-in module developed by the CMS preshower. It is based on a 12-channel optical receiver and a Field Programmable Gate Array (FPGA) Stratix™ GX from ALTERA. The FPGA has multiple gigabit blocks, each with four full duplex channels.

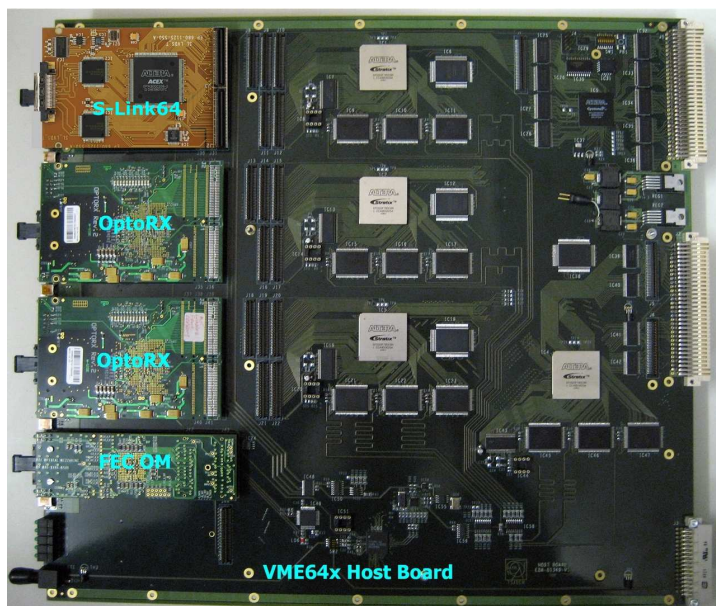


Figure 7.9: Photo of the TOTEM FED Host board.

Using clock data recovery technology, these channels can serialise or de-serialise data for transmission rates up to 3.125 Gbps. The module is compatible with the VME mechanical specification [56].

The first stage of FED data management is performed on the optoRX-12 with the de-serialisation of 32 input data streams per FPGA using the embedded high-speed deserialisers.

The second stage of data management is performed on the Host board. There are 3 Altera FPGAs Stratix™ labelled “Main-1”, “Main-2” and “Main-3”. Each Main controller bridge receives raw data from its associated OptoRX-12 module, stores it into its corresponding memory and transfers it to the VME64x bus or to the USB for slow spy readout.

For certain FED applications the de-serialised data are processed inside the OptoRX-12 module in order to reduce their volume. Then a fourth FPGA (also a Stratix™), labelled “Merger”, collects the reduced data through three associated 64-bit buses in order to build the event.

In the Trigger Host boards the incoming trigger data is sent to the FPGAs where coincidence logic functions and more complex algorithms can be performed in order to prepare trigger primitives for the global L1 TOTEM trigger. There are 2 Host Boards per detector used for the trigger.

Since the TOTEM Host boards are also used for data readout, all necessary hardware is available to include the trigger data into the data stream for monitoring purposes.

In the Tracking Host boards the incoming tracking data has a format defined by the data packets of VFAT. The format is defined in figure 7.3.

The data length is organised in 16 bit words consisting of: BC⟨11:0⟩ (bunch counter), EC⟨7:0⟩ (event counter), Flags⟨3:0⟩, Chip ID⟨11:0⟩, Data⟨127:0⟩, CRC 16 checksum⟨15:0⟩ and four control bits for the beginning of the frame. For multiple triggers the frames for each event follow one after another.

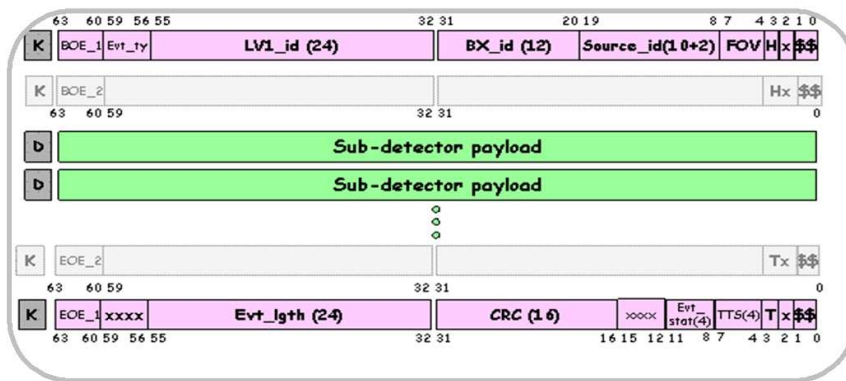


Figure 7.10: CMS FED data format.

When an event fragment is ready to be transmitted to the DAQ, the FED event builder encapsulates the data according to the common CMS FED data format [57] shown in figure 7.10.

The CMS format includes, in addition to the actual sub-detector payload, information such as event type (‘Evt_ty’), event number (‘LV1_id’), bunch crossing number (‘BX_id’), event length (‘Evt_lgth’), data source identifier (‘Source_id’) and CRC information.

There are 3 different possibilities implemented for sending data to the DAQ:

- VME interface: used for TOTEM operation;
- USB interface: alternative for TOTEM operation;
- S-Link64 [58] module: connection to the CMS Front-end Readout Links (FRLs) for common data taking, ensuring full compatibility with the CMS DAQ.

7.2.3 The low and high voltage power supplies

The on-detector electronics are electrically isolated from the counting room through the systematic use of floating power supplies and optical signal transmission or electrical transmission with opto-couplers. The low-voltage power supplies are located as close as possible to the detectors. The high-voltage power supplies are located in the counting-room.

7.3 Specific TOTEM detector electronics

Every effort has been made to standardise the use of components across all three detector systems. However, different geometries and segmentation have inevitably led to different board designs for the “on detector” regions and “local detector” regions.

This section aims to highlight the electronic boards used in the construction of the different detector systems.

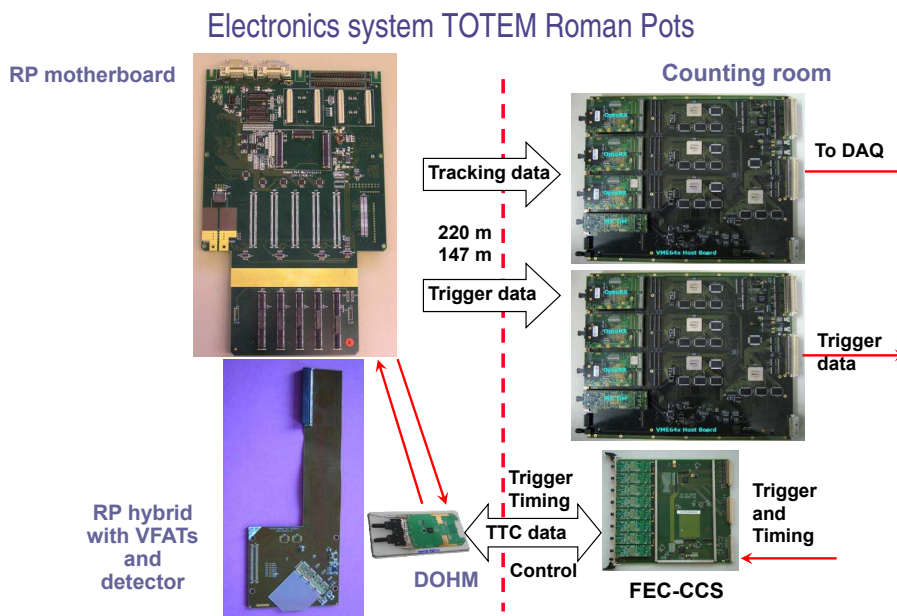


Figure 7.11: Overview of the RP electronics system.

7.3.1 TOTEM electronics boards for the Roman Pots

Figure 7.11 gives an overview of the electronics boards used for the Roman Pot system.

The Roman Pot hybrids contain one silicon detector sub-divided into 512 strips. Four VFATs are bonded directly to each strip with 128 channels per chip. There is one clock and LVDS bus on the hybrid to which each VFAT connects in parallel. In addition the clock is fed to the DCU chip which is also located on the hybrid. A single I²C bus is delivered to the hybrid which is connected to each VFAT and the DCU.

The RP hybrids (located in the “on detector region”) plug directly into the RP motherboard (located in the “near detector region”). The RP motherboard contains the components necessary for the token ring in the control path and the Trigger and Tracking data transmission components in the readout path. These components were described in section 7.2.

The low voltage power supplies are located approximately 70 m from the pots in the nearest alcove in the tunnel.

7.3.2 TOTEM electronics boards for T1

An overview of the electronic boards used in T1 is shown in figure 7.12.

The VFAT used for the gas detectors is a slightly different version than that used for the Roman Pots. The difference is that the VFAT inputs have internal overload protection circuits that help avoid destructive breakdown of the chip in the case of sparks (uncontrolled charge discharges) from the detector [59]. In all other respects however the VFATs are identical. T1 and T2 use also the same hybrid. This hybrid contains one VFAT chip.

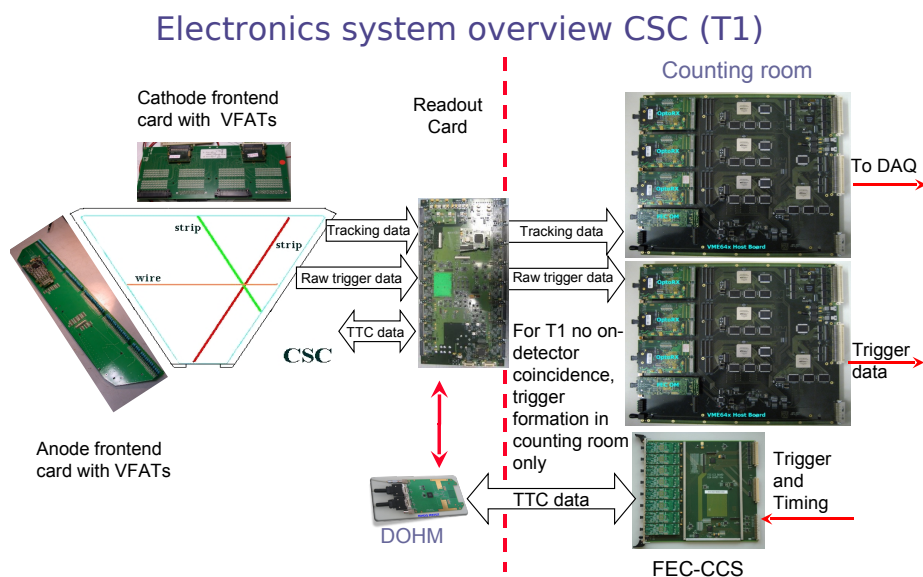


Figure 7.12: Overview of the T1 electronics system.

The connection to the T1 detector is made by plugging the hybrids into one of two readout cards adapted to the geometry of the T1 detector. One for the readout of the anodes (AFEC) and the other for the readout of cathodes (CFEC).

The “on detector region” is connected to the “local detector region” by cables. A T1 Read-Out Card (ROC) contains the components and functions shown in figure 7.7 for the local region with the exception of the CC chip. T1 will instead readout all VFAT S-bits without making any logical operations with respect to other VFATs in the system. One ROC can handle the readout of two cathode strip chambers, and can therefore be connected to up to two AFECs and up to 14 CFECs.

7.3.3 TOTEM electronics boards for T2

The electronics boards developed for the T2 system are shown in figure 7.13.

Similar to T1, the T2 detector also uses the VFATs designed for gas detectors which include the input protection circuits. The hybrids are also the same as the ones used for T1. The connection to the detector is made by plugging the hybrids into the horse-shoe card (so called because of its geometrical shape) which in turn is connected to the GEM strips and pads. The VFAT control and readout paths connect by a cable to a board known as the “11th Card”. The 11th card receives data from 10 Horse-shoe cards and also contains a CC chip for the coincidence logic function of the trigger path S-bits.

T2 has the most severe ionising radiation environment of the 3 detectors of up to 50 Mrads (see table 7.1). Whilst VFAT and the CC chip are expected to survive these radiation levels the optical links will not. Hence the electronics of the “near detector region” will be placed in a rack near the detectors but behind a radiation shield.

Electronics system overview GEM (T2)

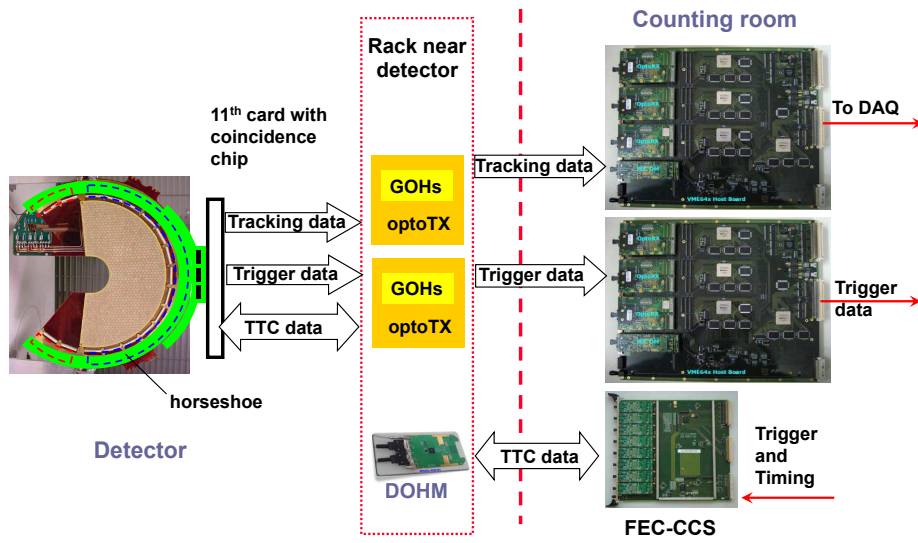


Figure 7.13: Overview of the T2 electronics system.