Chapter 3

Trigger and DAQ electronics

3.1 Global flow of trigger and DAQ

Data acquisition is carried out in the ATLAS counting room (USA15). All the sequences are optimized for 43 bunch operation. A timing diagram of trigger and data acquisition is shown in figure 3.1. Signals from the detectors reach the electronics in the counting room though 200 m cables. A first level trigger is generated when a bunch crossing (BX) occurs that can be identified using two BPTX signals generated by two Beam Position Monitors (BPMs) installed 175 m away from the interaction point. At every first level trigger, a 500 nsec gate signal is sent to the ADC for the plastic scintillators (CAEN V965). The particle flight time from the interaction point to our detectors is 466 nsec and the signal propagation time between the detector and USA15 is 860 nsec. The signals from plastic scintillators arriving at USA15 are split into ADCs and discriminators (CAEN V814B) by custom made NIM FANOUT modules with amplification factors of 1 and 4, respectively. The outputs of the discriminators are sent to VME FPGA boards (GND GPIO GN-

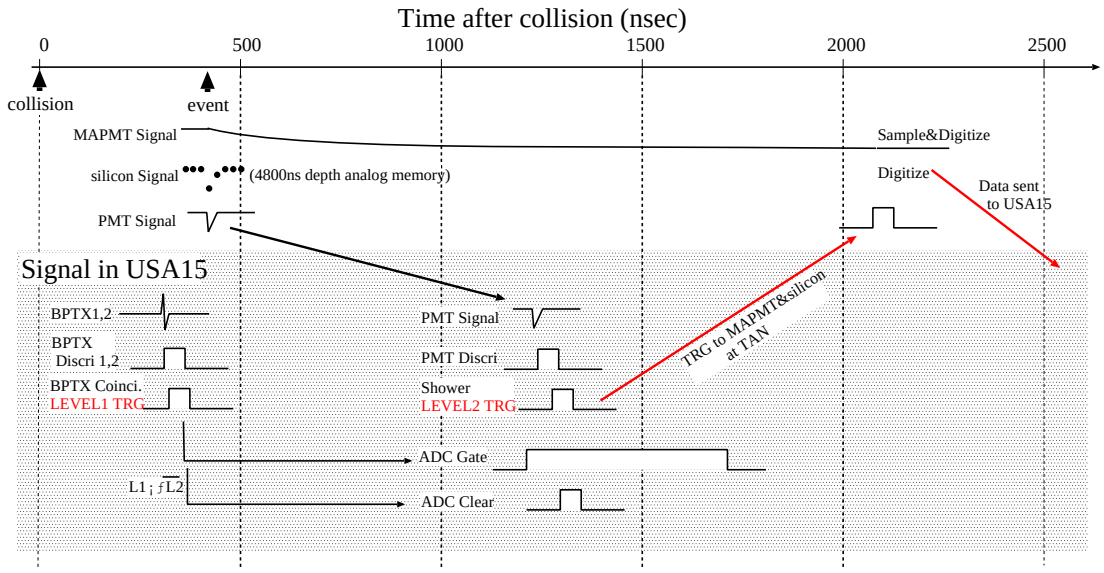

Figure 3.1: The timing chart for trigger and DAQ.

0324-3). Then the second level trigger is issued when more than 3 successive layers detect more than 300 particles corresponding to the energy threshold of about 100 GeV. Details of the trigger logic and energy threshold will be further optimized considering the actual beam conditions at the time of LHC operation. If the second level trigger is not generated within 1 μsec after the first level trigger, the ADC is cleared. At the second level trigger, if the acquisition PC is enabled to read data, a final signal to collect all the data is issued. For the SciFi in detector 1, the second level trigger is sent to the FECs to sample and digitize the MAPMT signal as described in section 3.2. For the silicon tracker in detector 2, the signal stored in the analog memory at the proper timing is digitized as described in section 3.3. Then digitized pulse height data is sent to the counting room and recorded together with the calorimeter data.

The data acquisition is carried out independently for the two arms. However in case of a high background counting rate, which can be expected if the residual gas in the beam pipe is far worse than expected, we can use a coincidence between the two arms to suppress this background. The FC with large acceptance coverage are expected to supply coincidence signals with the detector on the opposite side.

The data acquisition is carried out using the MIDAS package (Maximum Integration Data Acquisition System, [16]). One MIDAS server PC controls two front end PCs for detector 1 and detector 2. The raw data sizes of a single event for two arms are 1.2 kbytes and 14 kbytes in the MIDAS format. The MIDAS server PC also performs a RAID1 storage and can store up to 1.5 Tbytes of data, corresponding to about 10^8 events from both arms. Two other PCs, one for each arm, also communicate with the MIDAS server for a fast analysis during the run. The MIDAS format can be converted to the ROOT format by which fast on-line analysis will be made with the standard ROOT analysis tools [17]. Some basic results of the fast analysis (counting rate, event position, etc.) are distributed in the CERN network every second through the Data Interchange Protocol (DIP). Slow control data (electronics temperature, HV, LV values, manipulator position, etc) are also recorded. Some important machine conditions (luminosity, crossing angle, etc.) are also received through the DIP and recorded in our data base.

In order to synchronize with ATLAS events in possible further analysis, we count the number of the ATLAS level-1 (L1A) triggers and 40 MHz clock (Bunch Clock or BC) counts. These counts are reset roughly every second by the Event Counter Reset (ECR) signal that is also issued from ATLAS. These counts are latched and stored in FIFO when a L1A signal arrives and readout when a LHCf trigger is generated. Time synchronization of the acquisition PC with the CERN time server with one second accuracy can enable us to correlate LHCf and ATLAS events. The combination of the PC clock and the BC count gives the absolute time of each event with a precision of 25 nsec. Because the interval between bunch crossings will be 2 μsec during LHCf operation, we can easily identify the correlated events. These methods will also be used to identify the coincident events of detector 1 and detector 2.

3.2 Electronics and DAQ for the SciFi detector

The MAPMT signals are read out with the Front End Circuits (FECs) packed in the detector on which analog ASICs (VA32HDR14), ADCs and sequencers are mounted. Two VA32HDR14 chips, each of which contains 32 sets of preamplifier, shaping amplifier, sample and hold circuits,

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and one analog multiplexer, are used to read out the 64 channels for one MAPMT. Peaking time of the shaping amplifier is 1.9 μs. The peak voltages recorded by the sample and hold circuits are read out through an analog multiplexer. One ADC coupled to one VA32HDR14 performs the digital conversion of 32 channels in 64 μs. The digital data are transferred in a serial line from the detector via LVDS to an interface board installed on the VME bus. The processes after sampling are carried out when a trigger signal arrives at the FEC according to the level-2 trigger described in section 3.1. The trigger signal arriving 1.9 μs after the shower matches with the peaking time of the shaping amplifier.

3.3 Electronics and DAQ for the silicon tracking detector .

The DAQ used for the silicon part of detector 2 is mainly based on the fast electronics developed for the large LHC experiments, inserted in custom made boards and produced taking into account the LHCf requirements.

The analog preamplifier (PACE3) outputs are digitized by custom made ADC boards with 12 bit resolution. These boards are mounted, piggy-back, on a mother board which also takes care of the optical link communications and clock, level-2 trigger and slow control distribution to the PACE3 chips. Two silicon detectors are serviced by one mother board in such a way that a total of 4 mother boards are installed in the TAN area. The digitized data, along with other status information, are sent via optical fiber links to a VME receiver board in the Atlas USA15 counting room. The receiver board formats the data in an appropriate way for the common detector 2 DAQ to digest. The PACE3 chips receive the LHC 40 MHz clock and level-2 trigger through the TTCrx system developed at CERN for LHC [18]. The signals are coded through a Front End Controller (FEC) module (developed for the CMS experiment [19]) which also takes care of the I2C commands needed to properly set the PACE3 internal registers. From the FEC these fast control signals are sent through optical links down to the experiment in the tunnel. A custom receiver board then decodes the signals and sends them via an electrical token ring to the Clock and Control Unit Modules(CCUM) on the mother boards. These CCUM [19], developed for the CMS tracker, decode both clock, trigger and I2C commands for the PACE3 chips.