Chapter 2

The LHCb Detector

2.1 Detector layout

LHCb is a single-arm spectrometer with a forward angular coverage from approximately 10 mrad to 300 (250) mrad in the bending (non-bending) plane. The choice of the detector geometry is justified by the fact that at high energies both the b- and $\bar{\text{b}}$-hadrons are predominantly produced in the same forward or backward cone.

The layout of the LHCb spectrometer is shown in figure 2.1. The right-handed coordinate system adopted has the z axis along the beam, and the y axis along the vertical.

Intersection Point 8 of the LHC, previously used by the DELPHI experiment during the LEP

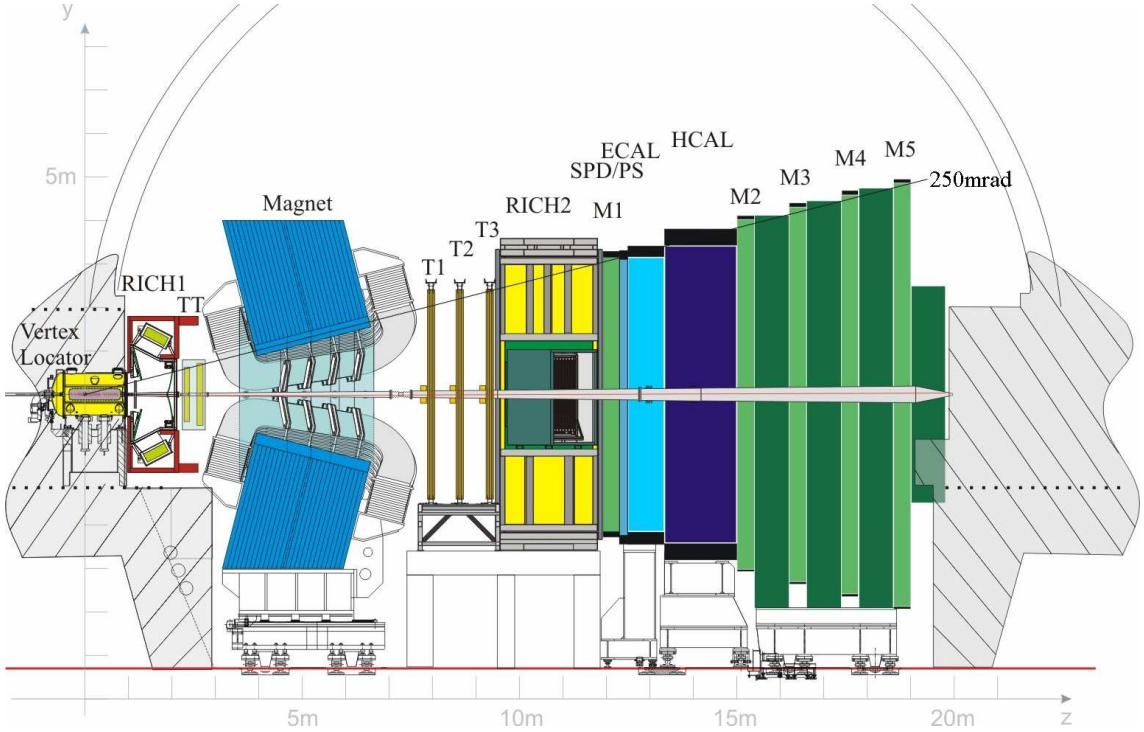

Figure 2.1: View of the LHCb detector.

time, has been allocated to the LHCb detector. A modification to the LHC optics, displacing the interaction point by 11.25 m from the centre, has permitted maximum use to be made of the existing cavern for the LHCb detector components.

The present paper describes the LHCb experiment, its interface to the machine, the spectrometer magnet, the tracking and the particle identification, as well as the trigger and online systems, including front-end electronics, the data acquisition and the experiment control system. Finally, taking into account the performance of the detectors as deduced from test beam studies, the expected global performance of LHCb, based on detailed MonteCarlo simulations, is summarized.

The interface with the LHC machine is described in section 3. The description of the detector components is made in the following sequence: the spectrometer magnet, a warm dipole magnet providing an integrated field of 4 Tm, is described in section 4; the vertex locator system (including a pile-up veto counter), called the VELO, is described in section 5.1; the tracking system made of a Trigger Tracker (a silicon microstrip detector, TT) in front of the spectrometer magnet, and three tracking stations behind the magnet, made of silicon microstrips in the inner parts (IT) and of Kapton/Al straws for the outer parts (OT) is described in sections 5.2 and 5.3; two Ring Imaging Cherencov counters (RICH1 and RICH2) using Aerogel, C_4F_{10} and CF_4 as radiators, to achieve excellent π-K separation in the momentum range from 2 to 100 GeV/c, and Hybrid Photon Detectors are described in section 6.1; the calorimeter system composed of a Scintillator Pad Detector and Preshower (SPD/PS), an electromagnetic (shashlik type) calorimeter (ECAL) and a hadronic (Fe and scintillator tiles) calorimeter (HCAL) is described in section 6.2; the muon detection system composed of MWPC (except in the highest rate region, where triple-GEM's are used) is described in section 6.3. The trigger, the online system, the computing resources and the expected performance of the detector are described in sections 7, 8, 9, and 10, respectively.

Most detector subsystems are assembled in two halves, which can be moved out separately horizontally for assembly and maintenance, as well as to provide access to the beampipe.

Interactions in the detector material reduce the detection efficiency for electrons and photons; multiple scattering of pions and kaons complicates the pattern recognition and degrades the momentum resolution. Therefore special attention was paid to the material budget up to the end of the tracking system. Estimations of the material budget of the detector [3] using realistic geometries for the vacuum chamber and all the sub-detectors show that at the end of the tracking, just before entering RICH2, a particle has seen, on average, about 60% of a radiation length and about 20% of an absorption length.

2.2 Architecture of the front-end electronics

The front-end architecture chosen for LHCb [4, 5] has to a very large extent been determined by the requirement of making a hardware-based short latency trigger, with an efficient event selection, for complicated B events. A fast first level trigger has been found capable of making an event rate reduction of the order of 1 in 10. This has for the chosen LHCb luminosity enforced the use of a front-end architecture with a first level trigger rate of up to 1 MHz. This was considered to be the highest rate affordable for the data acquisition system (DAQ) and required readout links. The general front-end electronics architecture and data flow in the DAQ interface are shown in figure 2.2. All sub-detectors store sampled detector signals at the 40 MHz bunch crossing rate in

2008 JINST 3 S08005

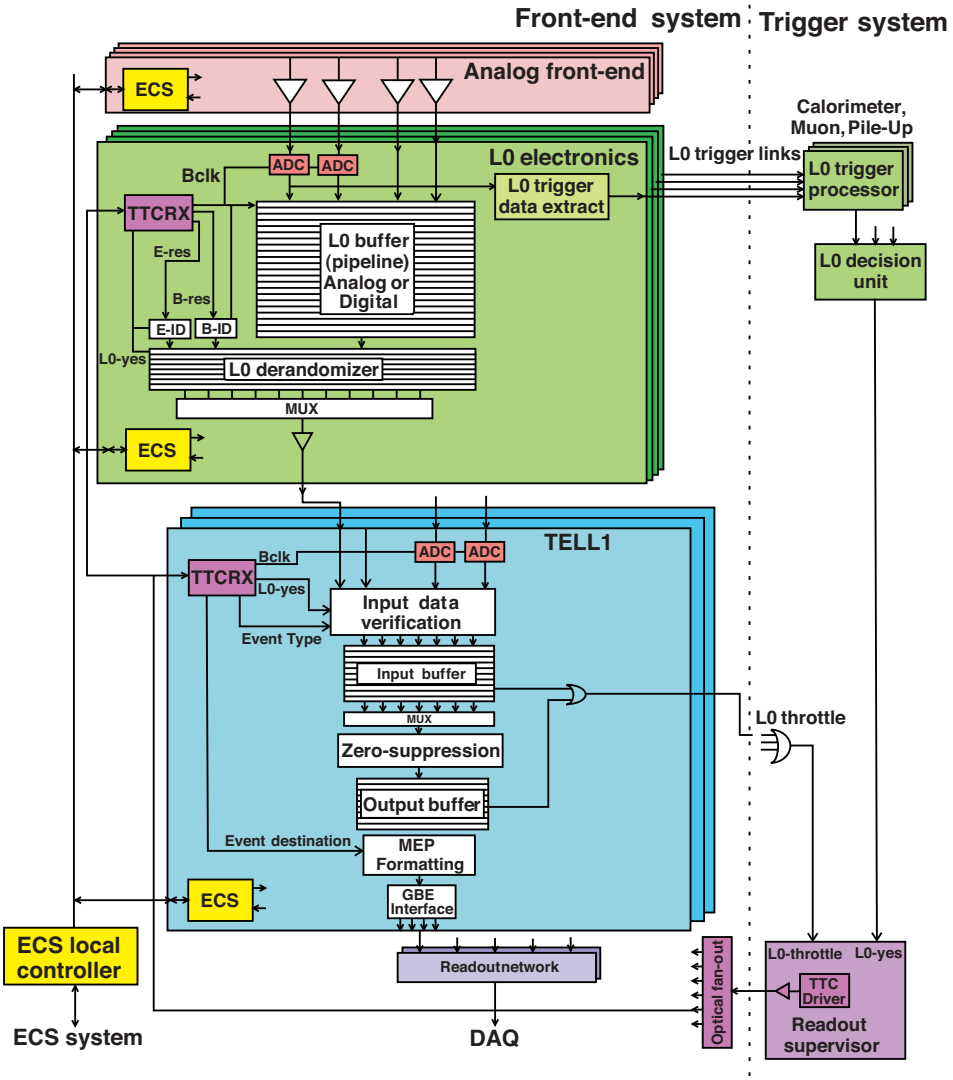

Figure 2.2: General front-end electronics architecture and data flow in the DAQ interface.

4 μs deep pipeline buffers, while the hardware-based first level trigger (hereafter called Level-0 or L0) makes the required trigger selection. The speed of the analog detector signal shaping is in general such that only a single sample from one bunch crossing within 25 ns is extracted from each detector channel when a positive trigger is given (with an exception for the OT with a drift time of up to two bunch crossings). After the first level trigger acceptance, event data are transferred to 16 event deep first level derandomizing buffers to enable a nearly constant data readout rate to the DAQ interface modules located in the counting house. The 16-deep derandomizer allows the front-end to handle closely spaced triggers efficiently. At the output of the derandomizer, data from 32 channels are transferred at a rate of 40MHz, giving a maximum rate of 1.1 MHz, and multiplexed into constant data rate links.

All sub-detectors, except the VELO, use optical links (6000 in LHCb) based on the radiation hard GOL (Gigabit Optical Link) serializer chip [6]. A centralized scheme, implemented in the readout supervisor module (see section 8.3), imposes global restrictions on the trigger accept rate

to prevent overflows of the derandomizer buffers and the following readout and data processing stages. Specific test and monitoring features are integrated into the different front-end systems to assure that thorough testing and monitoring can be made [7] as indicated in figure 2.2.

The Trigger, Timing and Control system (TTC) developed for the LHC experiments [8] is used to distribute clock and sampling phase, timing control (reset and synchronization signals), trigger (trigger accept and trigger types) and a set of dedicated test and calibration commands to all front-end and DAQ interface modules. Control and monitoring of the front-end electronics are based on either the LHCb specific *SPECS* control interface or the *ELMB* CAN bus module developed by ATLAS [9].

The reception of accepted event data from the sub-detectors is handled by 350 9U VME sized DAQ interface modules in the counting house. These *Field Programmable Gate Array* (FPGA) based modules receive front-end data, perform data and event synchronization verifications, appropriate zero-suppression and/or data compression, data buffering and finally send the event information to the DAQ system over up to four Gigabit-Ethernet links per module, as indicated in the lower part of figure 2. The DAQ interface module is in general based on a highly flexible and programmable module named TELL1 [10] with the exception of the RICH detector that has chosen to use a dedicated module[1] (c.f. section 6.1).

The electronics equipment is located in two different areas. Front-end electronics are installed on the subdetectors or in their close vicinity. Readout and trigger electronics as well as the Experiment Control System and the Data Acquisition system are located in a radiation protected *counting house*, composed of three levels of *electronic barracks* separated by a concrete shielding from the experimental area. The *control room* of the experiment in located on the ground floor.

The present paper does not contain a dedicated chapter with the detailed description of the electronics. The implementation of the specific front-end electronics is described in more detail in the chapters on the individual sub-detectors. Details of the readout supervisor, the Experiment Control System (ECS) and the DAQ system are described as part of the online system (section 8).

Radiation tolerance of the electronics

All detector components need to tolerate significant radiation doses. Parts of the trigger outside of the counting house are no exception.

The front-end electronics of each sub-detector are located either within the sub-detector itself or on its periphery. Sub-detector specific ASIC's and modules have been custom developed to handle the signal processing needed for the large channel counts in an environment with significant radiation levels. Radiation resistance requirements for all locations with electronics have been defined based on FLUKA simulations with appropriate safety factors [11] (e.g. 10 MRad and 10^{14} 1 MeV-neutron equivalent (n_{eq}) per cm^2 for the front-end chip used for the VELO and the Silicon Tracker; 4 kRad and 10^{12} n_{eq}/cm^2 for the ECAL/HCAL electronics, over 10 years of running). Extensive radiation tests have been made for all electronics components used in the front-end electronics, to verify their correct behaviour, after radiation (total dose and displacement damage), and during radiation exposure (single event upsets).

[1] Called UKL1 board.

2008 JINST 3 S08005